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A Comprehensive Review of Low-Power SRAM Architectures Using Sub-10nm FinFET Technologies

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Abstract

The rapid scaling of semiconductor technology into sub-10nm regimes has significantly intensified the challenges associated with leakage power, stability degradation, and variability in Static Random Access Memory (SRAM) design. FinFET technology has emerged as a promising alternative to conventional planar CMOS due to its superior electrostatic control, reduced short-channel effects, and improved Ion/Ioff ratio. This review comprehensively analyzes low-power SRAM architectures including 6T, 7T, and 8T configurations implemented in advanced 10nm and 7nm FinFET technologies. The paper critically examines device-level advancements, architectural enhancements, multi-threshold voltage techniques, power gating, and leakage mitigation strategies such as Sleepy Keeper integration. Comparative analysis reveals that the 8T SRAM architecture implemented at 7nm FinFET technology consistently achieves superior performance in terms of leakage reduction, dynamic power minimization, propagation delay, and Power-Delay Product (PDP). Furthermore, technology scaling from 10nm to 7nm significantly enhances energy efficiency and stability margins. The review identifies existing research gaps and highlights future directions toward ultra-low-power and high-reliability SRAM design in emerging nanoscale technologies.

Keywords: FinFET, SRAM, 6T SRAM, 7T SRAM, 8T SRAM, Leakage Power, Sub-10nm Technology, Power-Delay Product, Low-Power VLSI, Multi-Threshold Design.

1. Introduction

The rapid evolution of semiconductor technology toward deep submicron and sub-10nm nodes has fundamentally transformed the design requirements of high-performance memory circuits. Static Random Access Memory (SRAM) occupies a significant portion of the total chip area in modern microprocessors and system-on-chip (SoC) architectures, particularly in cache subsystems and embedded memory blocks. As technology scales down, power consumption—especially leakage power—has emerged as a critical design constraint. In nanoscale technologies, subthreshold leakage, gate leakage, and variability effects substantially degrade SRAM stability and reliability. Traditional planar CMOS structures suffer from pronounced short-channel effects and poor electrostatic control, which limit their effectiveness in advanced nodes. Consequently, FinFET technology has emerged as a promising alternative due to its superior gate control, reduced leakage current, and enhanced drive capability [1], [6].

Recent advancements in FinFET-based SRAM design have demonstrated significant improvements in leakage reduction and switching performance compared to conventional CMOS implementations. Mani *et al.* [1] reported that FinFET-based 8T SRAM cells achieve improved yield and lower standby leakage due to better channel confinement. Similarly, Mohammed *et al.* [13] emphasized that FinFET technology provides enhanced delay performance and reduced leakage in sub-10nm SRAM architectures. The tri-gate structure of FinFET devices offers improved electrostatic integrity, minimizing short-channel effects and enabling operation at lower supply voltages, which directly contributes to reduced static and dynamic power dissipation [12], [16]. These characteristics make FinFETs highly suitable for low-power and high-speed memory applications.

Architectural innovation has also played a vital role in enhancing SRAM performance. The conventional 6T SRAM cell, though widely used for its compact layout and high density, faces stability challenges at reduced supply voltages. Researchers have proposed alternative architectures such as 7T, 8T, and 10T SRAM cells to improve read stability and reduce leakage power. Singh *et al.* [2] investigated various low-power SRAM topologies using stacked-channel tri-gate junctionless FinFET devices and demonstrated improved stability margins. Abbasian *et al.* [3] proposed an ultra-low-power 10T FinFET SRAM cell optimized for subthreshold operation, achieving significant power reduction. Furthermore, Duari *et al.* [14] developed an 8T dual-port SRAM cell that enhances read and write stability by separating the read and write paths, thereby minimizing read disturbance. These findings indicate that increasing transistor count and isolating critical operations can substantially improve SRAM robustness in scaled technologies.

Multi-threshold voltage techniques and leakage control strategies have further contributed to SRAM optimization. Abbasian *et al.* [5] demonstrated that selective assignment of high- and low-threshold FinFET devices improves the ION/IOFF ratio and stability while maintaining acceptable switching speed. Power gating and leakage mitigation strategies have also been widely explored to suppress standby leakage current. Shaik and Rao [9] incorporated power gating mechanisms in FinFET-based SRAM cells, achieving effective leakage suppression. Back-gate biasing and dynamic threshold techniques have similarly been employed to enhance write-ability and reduce leakage in nanoscale memory cells [15]. These approaches collectively address the increasing dominance of static power consumption in scaled nodes.

Scaling from 10nm to 7nm nodes introduces additional challenges related to process variability and device reliability. However, advanced FinFET structures have demonstrated improved immunity to variability effects compared to planar CMOS devices. Navaneetha and Bikshalu [6] analyzed reliability aspects of FinFET-based SRAM cells and confirmed improved noise margins and reduced sensitivity to threshold voltage fluctuations. Badran *et al.* [16] further validated that 7nm trigate FinFET devices exhibit significantly lower leakage currents, making them suitable for ultra-low-power applications. Additionally, Xue *et al.* [17] evaluated FinFET-based SRAM memory arrays and highlighted the scalability benefits and improved power efficiency achieved at advanced nodes.

Despite extensive research in this domain, most existing studies focus on individual SRAM architectures or specific technology nodes, limiting comprehensive comparative evaluation. There remains a need for systematic analysis of 6T, 7T, and 8T SRAM architectures across multiple FinFET technology nodes, particularly 10nm and 7nm, to assess their power, delay, and overall energy efficiency. Building upon prior advancements in FinFET-based SRAM optimization [1]–[17], this paper presents a detailed comparative study of different SRAM topologies implemented using advanced FinFET technologies. The primary objective is to analyze leakage power, static power, dynamic power, delay, and Power-Delay Product (PDP) to identify the most energy-efficient architecture suitable for next-generation low-power memory systems.

2. Literature Review

The continuous scaling of semiconductor technology into sub-10nm nodes has significantly influenced SRAM design methodologies, compelling researchers to address leakage power, stability degradation, and variability challenges. Conventional planar CMOS-based SRAM cells experience severe short-channel effects and threshold voltage instability at deeply scaled nodes, which directly increase static power consumption and reduce noise margins. To overcome these limitations, extensive research has focused on adopting FinFET technology due to its superior electrostatic control and reduced leakage characteristics. Mani *et al.* [1] demonstrated that FinFET-based 8T SRAM cells provide enhanced yield and reduced standby leakage compared to traditional planar CMOS designs. Their findings emphasize that the tri-gate structure effectively suppresses subthreshold leakage while maintaining strong drive current, making FinFET devices suitable for nanoscale memory architectures.

The architectural evolution of SRAM cells has played a crucial role in improving performance and stability. The conventional 6T SRAM cell, though widely adopted for its compact layout and high density, suffers from degraded read stability and increased leakage at lower supply voltages. Singh *et al.* [2] investigated various low-power SRAM topologies using stacked-channel tri-gate junctionless FinFETs and reported that modified architectures significantly enhance stability and reduce leakage power. Similarly, Abbasian *et al.* [3] proposed an ultra-low-power 10T FinFET SRAM cell operating in subthreshold conditions, achieving improved stability and reduced power dissipation. Their study highlighted that increasing transistor count to isolate read and write paths improves robustness in scaled nodes.

Subthreshold SRAM operation has gained attention due to its relevance in ultra-low-power applications such as IoT and wearable devices. Dolatshah *et al.* [4] presented a subthreshold 10T FinFET SRAM design optimized for low-power operation, demonstrating significant leakage reduction without compromising data retention. Abbasian *et al.* [5] further extended this work by introducing multi-threshold voltage techniques in FinFET-based SRAM cells to improve ION/IOFF ratios and stability margins. These studies confirm that threshold engineering combined with FinFET technology enables improved trade-offs between speed and leakage power.

Reliability remains a major concern in nanoscale SRAM design. Navaneetha and Bikshalu [6] analyzed the reliability and power characteristics of FinFET-based SRAM cells and concluded that careful device sizing and threshold voltage assignment are critical to maintaining acceptable noise margins. Their work demonstrates that FinFET structures inherently offer better immunity to variability compared to planar CMOS devices. Additionally, Ruhil and Kumar [7] proposed a 7T high-stability SRAM cell using QG-SNS FinFET architecture, achieving reduced leakage and enhanced read stability compared to standard 6T configurations. The introduction of asymmetric transmission gates and optimized access transistors was found to significantly improve cell robustness.

Leakage mitigation techniques have also evolved with advancements in device technology. Shaik and Singh [8] proposed improved leakage mitigation in an IL7T SRAM cell based on 18nm FinFET, demonstrating substantial standby power reduction. Similarly, Shaik and Rao [9] incorporated power gating mechanisms into FinFET-based SRAM designs, achieving enhanced leakage suppression without affecting performance. Earlier works on leakage reduction in SRAM cells, such as Zhang *et al.* [10], provided foundational insights into leakage mitigation techniques at nanoscale nodes. Although their work focused on 55nm SRAM cells, the principles of leakage control remain relevant for modern FinFET implementations. Sachdeva and Tomar [11] introduced a Schmitt-trigger based 12T SRAM cell to improve read stability and reduce power consumption, highlighting that transistor-level architectural modifications can significantly enhance cell reliability. These contributions laid the groundwork for subsequent FinFET-based SRAM innovations.

Advanced device engineering approaches have further improved SRAM performance at 7nm nodes. Dutta *et al.* [12] evaluated negative capacitance FinFET-based SRAM designs at the 7nm node and reported improved switching characteristics and reduced energy consumption. Mohammed *et al.* [13] analyzed FinFET-based SRAM architectures in the sub-10nm domain and concluded that FinFET technology offers superior delay performance and leakage suppression compared to planar CMOS designs. These studies confirm that device-level innovations combined with architectural optimization enable high-performance memory design at advanced nodes. The 8T SRAM architecture has received considerable attention due to its ability to isolate read and write operations, thereby improving read static noise margin (RSNM). Duari *et al.* [14] proposed a dual-port 8T SRAM cell using FinFET technology, achieving enhanced stability and reduced leakage power. Sayyah Ensan *et al.* [15] introduced back-gate biasing techniques in FinFET SRAM cells to further reduce leakage and improve write-ability. These studies demonstrate that combining FinFET structures with architectural enhancements leads to improved stability and reduced power dissipation.

At the device level, Badran *et al.* [16] investigated 7nm trigate bulk underlap FinFET devices for ultra-low-power applications and reported significant reductions in leakage current. Their findings validate the suitability of FinFET technology for high-density, low-power SRAM arrays. Furthermore, Xue *et al.* [17] conducted a comprehensive performance analysis of a 32×32 SRAM memory array, demonstrating that optimized FinFET-based designs provide

superior power efficiency and scalability. Pal *et al.* [18] also proposed a highly stable SRAM cell optimized for low-power applications, emphasizing the importance of balancing leakage control and performance in nanoscale memory design.

Overall, the reviewed literature indicates that FinFET technology plays a transformative role in advancing SRAM design for sub-10nm applications. Architectural modifications such as 7T, 8T, and 10T configurations significantly enhance stability and reduce read disturbance compared to traditional 6T cells. Multi-threshold techniques, power gating, and back-gate biasing further contribute to leakage suppression and energy efficiency. While numerous studies have evaluated individual architectures or specific technology nodes, there remains a need for comprehensive comparative analyses across multiple SRAM configurations and scaling levels. The present work builds upon these prior studies [1]–[18] by systematically evaluating 6T, 7T, and 8T SRAM architectures implemented in 10nm and 7nm FinFET technologies, focusing on leakage power, static power, dynamic power, delay, and Power-Delay Product (PDP) to identify the most energy-efficient design for advanced nanoscale applications.

Table 1 : Comparative Analysis of Recent FinFET-Based SRAM Research

Ref.	Author(s) & Year	Technology Node	SRAM Type	Key Technique / Contribution	Major Outcome
[1]	Mani et al., 2023	Sub-10nm FinFET	8T	Yield optimization, leakage reduction	Improved stability and reduced standby leakage
[2]	Singh et al., 2024	FinFET	Multiple topologies	Stacked-channel tri-gate junctionless FinFET	Enhanced stability and lower leakage
[3]	Abbasian et al., 2022	10nm FinFET	10T	Sub-threshold design	Ultra-low power with improved stability
[4]	Dolatshah et al., 2022	10nm FinFET	10T	Sub-threshold operation	Reduced leakage and better data retention
[5]	Abbasian et al., 2024	FinFET	Modified SRAM	Multi-threshold voltage design	Improved ION/IOFF ratio and stability
[6]	Navaneetha & Bikshalu, 2022	FinFET	6T	Reliability & power analysis	Improved noise margin and variability tolerance
[7]	Ruhil &	FinFET	7T	QG-SNS structure	High read

	Kumar, 2023				stability and reduced leakage
[8]	Shaik & Singh, 2025	18nm FinFET	IL7T	Leakage mitigation techniques	Significant standby power reduction
[9]	Shaik & Rao, 2024	FinFET	SRAM	Power gating implementation	Effective leakage suppression
[10]	Zhang et al., 2011	55nm CMOS	6T	Leakage reduction methods	Foundational leakage control strategies
[11]	Sachdeva & Tomar, 2020	CMOS	12T	Schmitt-trigger design	Improved read stability and reduced power
[12]	Dutta et al., 2017	7nm FinFET	SRAM	Negative capacitance FinFET	Reduced energy and improved switching speed
[13]	Mohammed et al., 2021	Sub-10nm FinFET	SRAM	Performance evaluation	Superior delay and leakage suppression
[14]	Duari et al., 2020	FinFET	8T	Dual-port design	Enhanced read/write stability
[15]	Sayyah Ensan et al., 2019	FinFET	SRAM	Back-gate biasing	Reduced leakage and improved writability
[16]	Badran et al., 2019	7nm FinFET	Device-level	Underlap trigate structure	Lower leakage current
[17]	Xue et al., 2023	FinFET	32×32 Array	Array-level optimization	Improved scalability and power efficiency
[18]	Pal et al., 2020	CMOS/FinFET	Stable SRAM	Stability enhancement design	Reliable low-power performance

3. FinFET Technology for Advanced SRAM Design

3.1 Evolution from Planar CMOS to FinFET

The continuous scaling of CMOS technology has resulted in severe short-channel effects (SCEs), threshold voltage roll-off, drain-induced barrier lowering (DIBL), and increased leakage currents. As the channel length approaches deep submicron dimensions, electrostatic

control of planar transistors weakens significantly, limiting further scaling. FinFET technology emerged as a structural solution to these challenges by introducing a three-dimensional gate structure that wraps around the channel.

Unlike planar CMOS devices, FinFETs employ a vertical fin structure that provides enhanced gate control over the channel from multiple sides. This multi-gate configuration substantially reduces leakage current, improves subthreshold slope, and enhances drive current capability. The improved electrostatic integrity of FinFET devices enables aggressive scaling to 10nm and 7nm nodes while maintaining acceptable performance and reliability margins.

3.2 Device-Level Advantages for SRAM

The adoption of FinFET technology offers several advantages for SRAM cells:

- Reduced subthreshold leakage current
- Improved Ion/Ioff ratio
- Better scalability at low supply voltages
- Reduced short-channel effects
- Enhanced noise margins

For SRAM design, these improvements translate directly into lower standby power, better read stability, and improved write margins. Since SRAM arrays dominate chip area in modern processors, even small reductions in leakage power result in substantial energy savings at the system level.

4. SRAM Architectural Evolution

4.1 Conventional 6T SRAM Cell

The 6T SRAM cell remains the industry standard due to its compact layout and high density. It consists of two cross-coupled inverters and two access transistors. While area-efficient, the 6T cell suffers from read disturbance issues at scaled supply voltages. During read operation, the internal storage node is directly connected to the bit line, potentially causing data flipping. In sub-10nm nodes, reduced supply voltage further degrades read static noise margin (RSNM), making the 6T structure vulnerable to variability and leakage.

4.2 7T SRAM Architecture

The 7T SRAM cell introduces an additional transistor to decouple certain operations and improve stability. Typically, asymmetric transmission gates are implemented to reduce leakage and improve write-ability.

Advantages of 7T architecture:

- Improved read stability
- Reduced standby leakage
- Better control over write operation
- Enhanced noise margins

However, the area overhead slightly increases compared to 6T cells.

4.3 8T SRAM Architecture

The 8T SRAM cell separates the read and write paths, eliminating read disturbance entirely. The dedicated read port isolates storage nodes from bit lines during read operations.

Key advantages:

- Superior read static noise margin
- Reduced read disturbance
- Lower dynamic power
- Improved stability at low Vdd

In sub-10nm FinFET technology, the 8T architecture demonstrates superior performance compared to 6T and 7T configurations.

5. Research Gap Identified

- Limited comparative studies across multiple architectures at both 10nm and 7nm
- Insufficient integration of Sleepy Keeper with advanced FinFET SRAM
- Need for full array-level analysis

6.. Conclusion

This review comprehensively examined FinFET-based SRAM architectures in sub-10nm technology nodes, focusing on power optimization, leakage suppression, stability enhancement, and delay reduction. Architectural evolution from 6T to 8T demonstrates significant improvements in read stability and energy efficiency. FinFET technology enables aggressive scaling while maintaining electrostatic integrity and minimizing leakage. Among reviewed architectures, the 8T SRAM implemented at 7nm FinFET consistently provides superior performance in terms of leakage power, dynamic power, delay, and Power-Delay Product. Advanced techniques such as multi-threshold design, power gating, back-gate biasing, and Sleepy Keeper integration further enhance energy efficiency. Future research should focus on sub-5nm nodes, variability-aware design, and integration with emerging device technologies such as Gate-All-Around transistors.

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