Design & Simulation of Second Stage & Three Stage OP-AMP Using 0.35μm CMOS Technology

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Abstract:- **A method is presented in this paper for the design of high speed CMOS Operational Amplifiers (Op-Amp).This paper is to design a Second Stage and Three Stage CMOS Operational amplifier and analyze the results of various aspect ratios on the characteristics of this Op-Amp, which operates at 3V to 5V power supply using TSMC 0.35μm CMOS technology. They have acceptable resolution and high speed of operation and can be placed in relatively small area. The design is implemented in 0.18u M CMOS process. The design includes folded cascade op-amp with a unity gain frequency of 200MHz at 88° deg. The complete design topology of high gain-high bandwidth Op-Amp is presented between all characteristics such as Gain, Phase margin, CMRR etc. It also comprehensive improvements are seen in case of CMRR, PSRR, Offset Voltage and Transient performance at the expense of power and output resistance. Besides, for low power-low bandwidth application an optimum noise performance is achieved in this design. A Second stage Op-Amp the DC gain of the amplifier is 70 dB. The unity gain frequency and phase margin of the amplifier are 65 GHz and 43° and total power consumption of the Op-Amp is 0.070 mw. A Three stage OP-AMP the DC gain of the amplifier is 69 dB. The unity gain frequency and phase margin of the amplifier are 74 GHz and 43.5° and total power consumption of the Op-Amp is 0.062 mw. for a parallel combination of 2 pF and 1 kΩ load. I used AWR (microwave office) software for implement this work.**

Keywords: **CMOS Analog Circuit, Second Stage CMOS Operational amplifier,Stability, Device Design, Scaling, Differential Amp, Three stage CMOS Operational amplifier.**

I. INTRODUCTION

With developments in deep sub micrometer CMOS processes, the available dynamic range in Operational Amplifiers (Op-Amps) is reduced due to lower power supply voltages [1].The design of analog circuits such as operational amplifiers (Op-Amps) in CMOS technology becomes more critical. Many authors have noted the disproportionately large design time devoted to the analog circuitry in mixed mode integrated circuits. In this paper we introduce a new method for determining the component values and transistor dimensions for CMOS Op-Amps. The method handles a very wide variety of specifications and constraints, is extremely fast, and results in globally optimal designs[15]. Designing high performance analog integrated circuits is becoming increasingly exigent with the relentless trend toward reduced supply voltages and transistor channel length. A large part of the success of the MOS transistor is due to the fact that it can be scaled to increasingly smaller dimensions, which results in higher performance. As the scale of integration improves, more transistors, faster and smaller than their predecessors, are being packed into a chip. This leads to the steady growth of the operating frequency and processing capacity per chip. The design of Op-Amps continues to pose a challenge as the supply voltage and transistor channel lengths scale down with each generation of CMOS technologies. In order to meet the gain requirements of op-amp in nano scale CMOS processes and low supply voltage, three or higher stage op-amp topologies have become important. In this paper, we present a systematic design methodology for split-length compensated low-voltage three-stage Op-Amps.

II. PSPICE FUNDAMENTALS

P Spice was initially developed by MicroSim and is used in electronic design automation. The company was bought by Or CAD, which was subsequently purchased by Cadence Design Systems. P Spice was the first version of UC Berkeley SPICE available on a PC, having been released in January 1984 to run on the original IBM PC.

This initial version ran from two 360 KB floppy disks and later included a waveform viewer and analyzer program called Probe. Subsequent versions improved on performanc e and moved to DEC/VAX Minicomputer Sun workstations, Apple Macintosh, and Microsoft Windows. During its development, P Spice has evolved into an analog mixed signal simulator.

III. CMOS TECHNOLOGY

In CMOS (Complementary Metal-Oxide Semiconductor) technology, both N-type and P-type transistors are used to realize logic functions. Today, CMOS technology is the dominant semiconductor technology for microprocessors, memories and application specific integrated circuits (ASICs). The main advantage of CMOS over NMOS and bipolar technology is the much smaller power dissipation. Unlike[2] NMOS or bipolar circuits[4], a CMOS circuit has almost no static power dissipation. Power is only dissipated in case the circuit actually switches. This allows to integrate many more CMOS gates on an IC than in NMOS or bipolar technology, resulting in much better performance. An n-type MOS (NMOS) and a p-type MOS (PMOS) device are fabricated on the same p-doped wafer, with the PMOS device embedded in an n-doped well.

IV. DESIGN OF SECOND STAGE OPAMP AND RESULTS

At first un buffered Second -Stage Op Amp is considered with CMOS based Op-Amp Fig. 1. The considering Gain bandwidth Product (GB), power and noise. But it has a low -3 dB frequency and its open loop response exhibits a sudden spike in gain vs. frequency curve when cascaded with second stage op amp. At this point a cascade op amp is designed in such a way that the 1st and 2nd pole shifts to the right of frequency axis increasing the -3 dB frequency along with increased GB and stability at the expense of relative power, noise and gain [6].

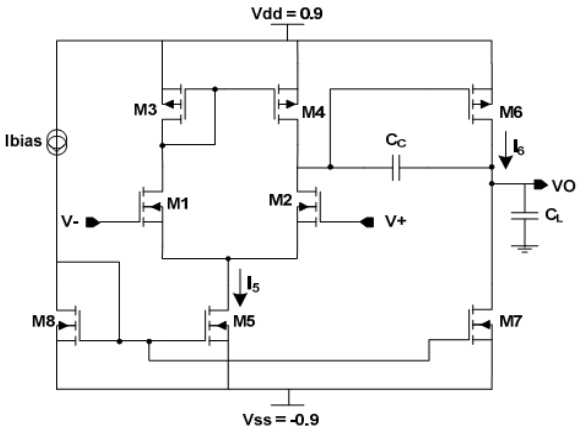

Figure 1: CMOS Design of Second Stage Op-Amp

In addition, Cc is added to increase the phase margin (45°) and hence the stability.[11] Because of cascading in the second stage, the circuit will be stable for large capacitive loading. It also doesn't need any level shifter [6].

Parameter	Two stage op amp
Gain (dB)	70
-3 dB frequency (MHz)	8.8
Phase Margin (°)	43
Unity gain frequency (GHz)	65
Power (mW)	0.062

Table 1:Parameters of Second Stage Op-Amp

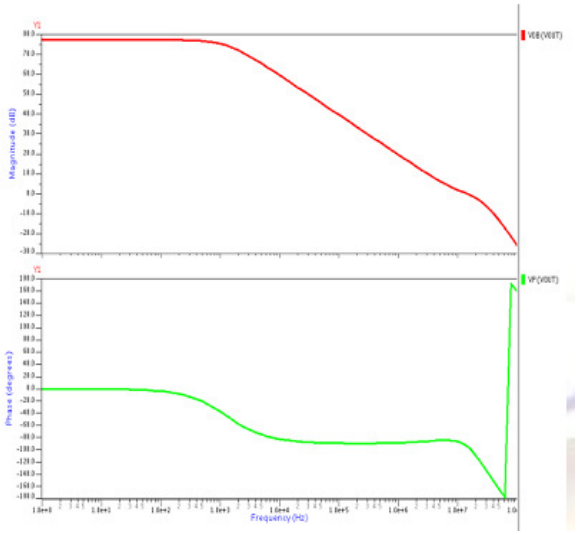

Figure 2. Output of Second Stage Op-Amp AC Analysis

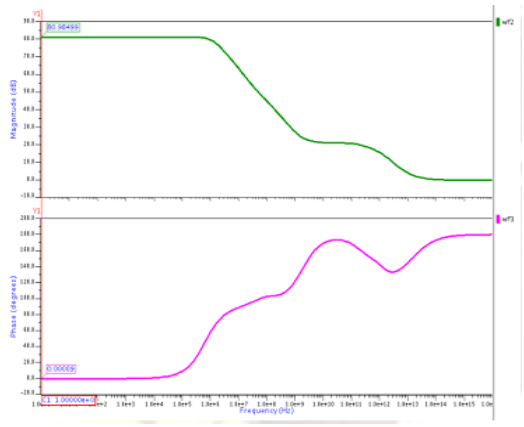

Figure 3. CMRR Result of Second Stage Op-Amp

V. DESIGN OF THREE STAGE OPAMP AND RESULTS

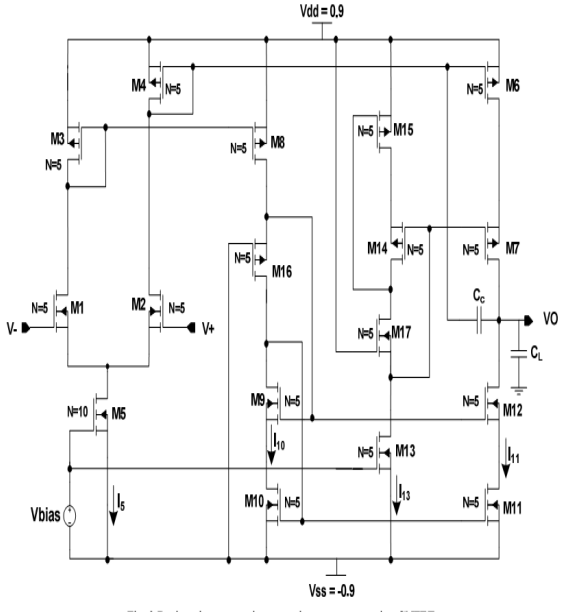

Figure 4: CMOS Design of Three Stage OP-AMP

Parameter	Three stage op amp
Gain (dB)	70
-3 dB frequency (MHz)	7.9
Phase Margin (°)	43.5
Unity gain frequency (GHz)	67
Power (mW)	0.070

Table 2:Parameters of Three Stage Op-Amp

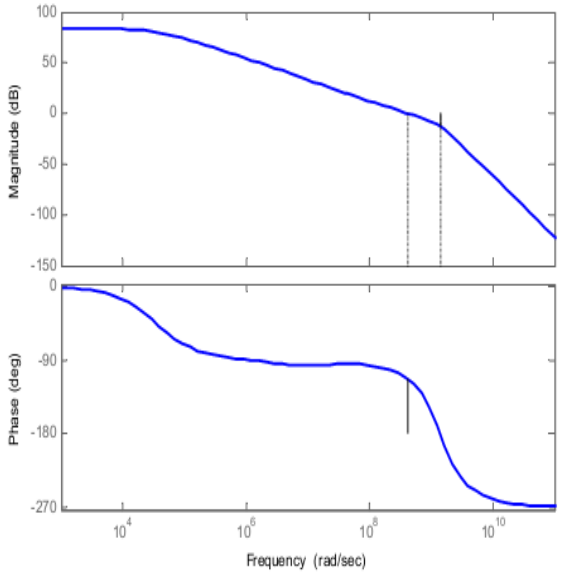

Figure 5. Output of Three Stage Op-Amp AC Analysis

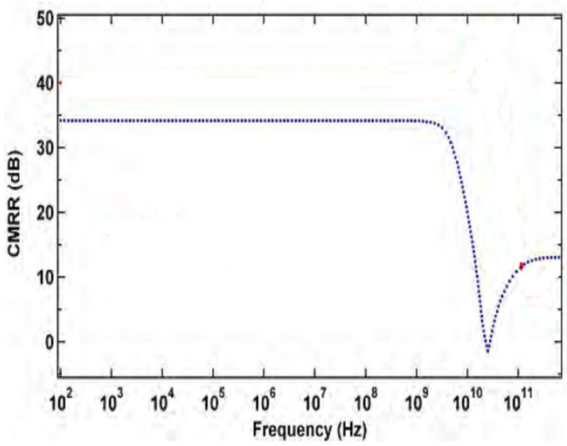

Figure 6. CMRR Result of Three Stage Op-Amp

VI. CONCLUSION AND FUTURE WORK

A fully-differential Op-Amp is designed in a TSMC 0.35µm standard digital CMOS process using the proposed compensation scheme. A Second stage OP-AMP the DC gain of the amplifier is 69 dB. The unity gain frequency and phase margin of the amplifier are 69 GHz and 43°,respectively. The total power consumption of the Op-Amp is 0.072 mw. A Three stage OP-AMP the DC gain of the amplifier is 72 dB. The unity gain frequency and

phase margin of the amplifier are 78 GHz and 43°,respectively. The total power consumption of the Op-Amp is 0.172 mw. We can also this parameters by using tuning NMOS CMOS parameters.

REFERENCES

[1] J. Appenzeller, Y. Lin, J. Knoch, Z. Chen, Ph. Avouris, "1/f Noise in Carbon Nanotube Devices-On the Impact of Contact and Device Geometry" IEEE Transactions on Nanotechnology, vol. 6, no. 3 pp 368–373, 2007.

[2] J. M. Marulanda and A. Srivastava, "Carrier Density and Effective Mass Calculations for Carbon Nanotubes" in ICICDT '07 IEEE, 2007, pp 1-4.

[3] M. Nayebi and B. A. Wooley, "A 10-bit video BiCMOS track-and-hold amplifier," IEEE J. Solid-State Circuits , vol. 24, pp.1507–1516, Dec.1989.

[4] P. J. Lim and B. A. Wooley, "A high speed sample and hold technique using a miller hold capacitance," IEEE J. Solid-State Circuits, vol. 26,pp. 643–651, Apr. 1991.

[5] G. C. Temes, Y. Huang, and P. F. Ferguson Jr., "A high-frequency track and hold stage with offset and gain compensation, "IEEE Trans. circuits Syst. II, vol. 42, pp. 559–560, Aug. 1995.

[6] S. Brigati, F. Maloberti, and G. Torelli, "A CMOS sample and hold for high-speed ADC's," inProc. IEEE Int. Symp. Circuits and Systems Circuits and Systems Connecting the World , vol.1, May 1996, pp. 163–166.

[7] J. H. Shieh, M. Patil, and B. J. Sheu, "Measurement and analysis of charge injection in MOS switches," IEEE J. Solid State Circuits , vol.SC-22, pp. 277–281, Apr. 1986.

[8] G. Wegmann, E. A. Vittoz, and F. Rahali, "Charge injection in analog MOS switches," IEEE J. Solid-State Circuits , vol. SC- 22, pp.1091–1097, Dec. 1987.

[9] G. Xu and S. Embabi, "A systematic approach in constructing fully differential amplifiers, "IEEE Tran. Circuits and Systems II: Analog and Digital Signal Processing, vol. 47, no. 11, pp.1343–1347, 2000.

[10] M. Shen, L. Hung, and P. Huang, "A 1.2 V fully differential amplifier with buffered reverse nested Miller and feed forward compensations," in IEEE Asian Solid-State Circuits Conf (ASSCC), 2006, pp. 171–174.

[11] S. Pavan, N. Krishnapura, R. Pandarinathan, and P.Sankar, "A power optimized continuous ime ADC for audio applications," IEEE J.Solid - State Circuits, vol. 43, no. 2, pp.351–360, 2008.

[12] X. Peng and W. Sansen, "Transconductance with capacitances feedback compensation for multistage amplifiers,"IEEE J. Solid-State Circuits,vol. 40, no. 7, pp. 1514–1520, 2005.

[13] V. Saxena and R. Baker, "Indirect compensation techniques for three-stage CMOS Op-Amps," in 52nd IEEE Int.Midwest Symp. Circuits and Systems (MWSCAS), 2009, pp.9–12.

[14] A. Younis and M. Hassoun, "A High Speed Fully Differential CMOS Opamp," Proceedings of the IEEE Midwest Symposium on Circuits and Systems , Vol. 2, pp.780-783,August 2000.

[15]P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design . Oxford University Press, 2002.

[16]R. J. Baker, H. W. Li, and D. E. Boyce, CMOS Circuit Design, Layout, and Simulation . IEEE Press, 1998.

[17] D. Johns and K. Martin, Analog Integrated Circuit Design .John Wiley & Sons, 1997.

[18] B. Razavi, Design of Analog CMOS Integrated Circuits. McGraw-Hill, 2001.

[19] TSMC 0.18-Micron Technology , Taiwan Semiconductor Manufacturing Company Ltd., Taiwan, April 2003.

[20] L. Trontelj, J. Trontelj, T. Slivnik, R. Sosic, and D. Strle, "Analog silicon compiler for switched capacitor filters," in Proc. IEEE Int. Conf. Computer-Aided Design , 1987, pp.506–509.

[21] P. J. Mvan Laarhoven and E. H. L. Aarts, Simulated Annealing: Theory and Applications Amsterdam, The Netherlands: Reidel, 1987.

[22] L. Vandenberghe, S. Boyd, and A. El Gamal, "Optimal wire and transistor sizing for circuits with non tree topology," in Proc. 1997 IEEE/ACM Int. Conf. Computer Aided Design ,pp. 252–259.

[23] L. Vandenberghe, S. Boyd, and A. El Gamal, "Optimizing dominant time constant in RC circuits," IEEE Trans.Computer-Aided Design, vol. 2,pp. 110–125, Feb. 1998.

[24] R J. Vanderbei, Linear Programming: Foundations and Extensions. Norwell, MA: Academic, 1997.

[25] F. Wang and R. Harjani, "Optimal design of op amps for oversampled converters," in Proc. IEEE Custom Integrated Circuit Conf. , 1996, pp.15.5.1–15.5.4.

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