Study of QSD Addition / Subtraction using Bidirectional Reversible Logic Gate

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Abstract- The researchers in VLSI Technology have been engaged in Multi-valued logic circuits (Quaternary) for the past few years, the intention behind the statement that some synonymous with multiple-valued logic is the of theory and application of logic, where the traditional truth values "true" and "false" are switched by several values. Because of carry propagation, complexity and delay gets introduced in the adder circuit due to which addition, subtraction and multiplication obtains delay in the Arithmetic Logic unit. In order to reduce the delay, carry-free addition is introduced by QSD (Quaternary Signed Digit) Numbers. In this paper, a study of QSD Addition and Subtraction circuit and Reversible Logic Gates.

Keywords:- Multi-valued Logic Circuit, Quaternary Signed Digit (QSD), Addition, Subtractor

I. INTRODUCTION

Integrated Circuit (IC) design has been developing from small scale integration‖ (SSI), which contains tens of transistors, to the current days of very Large Scale Integration‖ (VLSI) that includes millions of transistors on a single chip. Numerous different circuit technologies have been used in this path of IC design evolvement as presented [1, 2]. Metal Oxide Semiconductor (MOS) technology offered several fundamental benefits along with an easy fabrication of basic transistor switch and allowed the scaling resulting in IC size-reduction periodically. Complementary Metal Oxide Semiconductor (CMOS) technology conveyed the low power consumption advantage which developed semiconductor design applications. Whereas Analog designs deeply depend on the continuous signal response of transistors, digital designs rely on discrete logic levels of the signals. The overview of microprocessor designs along with their adjacent applications significantly increased the understanding of complex real-world applications using digital ICs for the past two decades is presented [3, 4]. Two-level logic specifically ―binary logic‖ is the decoding method used heavily. This logic basically involves only two logic levels: 0 and 1. Another improvement in logic decoding is the use of multiple levels namely more than two discrete levels signifying the signals.

Logically, in theory, higher radix will be better to represent as many numbers as possible. But, in the real-world, the restrictions of usability and availability of suitable devices limit the usage of higher radix-based MVL circuits is presented [5, 6]. The following four factors internment the trade-offs in choosing appropriate radix. Area: Increased data density of multiple valued logic circuits ensures that to reduce the area when compared to equivalent binary circuits. Every circuit stores additional information per bit. The remaining result is that a large number of data sets can be combined and implemented in a lesser area. Even though, at smaller circuits, the additional overhead of supplementary logic increases the area when compared to their equivalent binary gates. Therefore, the area advantages can only be found in larger circuits. Logic replication due to binary logic spread is avoided in MVL circuits. Also, higher radices would tolerate the increased number of functions that can be implemented, making it easier for larger and more complex functions implementation is presented. An additional advantage is the reduction of signal wires. The reduced wires would shrink the size of the chip and also recover the routability of the design. One of the serious challenges in the Deep Sub-Micron technologies is the routing bottleneck and also the fabrication of the proximity of the wires is illustrated [7, 8]. The restrictions of the current fabrication equipment would create several manufacturing defects like shorting of the wires, opening of the wires, etc. producing a lot of part defects and yield loss. So, reducing the number of wires would considerably improve the device manufacturability and area improvement.

II. LITERATURE SURVEY

B Devika Rani et al. [1], the worst-case delay is the primary drawback of the array multiplier that was initially developed for use in area optimizations. Many methods were developed to overcome this disadvantage, and the Vedic methodology has gained prominence due to its

rapid computations. It has been discovered that the Urdhva Tiryagbhyam-based Vedic multiplier is one of the most efficient multipliers with the shortest delay for multiplying any size of number. Despite this multiplier's high speed, area occupancy is higher. In order to reduce area, the Binary to Excess-one Converter (BEC) method is used in this multiplier. A 16 16 Vedic multiplier made with BEC adders and modified logic gates is developed to further enhance performance. Because the sum is directly generated in binary using the novel concept of an adjusting bit, the design does not require a radix conversion module. The Vedic multiplier that incorporates a QSD adder with a conversion module for quaternary to binary conversion, the Vedic multiplier that makes use of the Carry Select Adder, and a fast multiplication mechanism that is commonly used, such as the Booth multiplier, are contrasted with the design of the proposed multiplier. This large number of plans have been created utilizing Verilog HDL and blended by Synopsys Plan Compiler.

Mohammed A. Al-Ibadi et al. [2], based on the QSD number system and FPGA hardware, a fast parallel 2D-array computation has been implemented in this paper. In order to be processed by the digital hardware, the QSD numbers are encoded in binary bit streams. When adding binary-codded QSD numbers, the two-step parallel addition algorithm that is used to add two QSD numbers has been successfully implemented in an FPGA chip. The blends and execution of the equipment equal snake shows that the proposed equal viper has an elite presentation than the product variant, and the size of information clusters relies upon the quantity of rationale components of the FPGA chip.

K. Deepak et al. [3], this current work manages a reversible Vedic sort multiplier utilizing the earliest Urdhva Tiryagbhyam sutras of Vedic kind math consolidate with the QSD viper (Quaternary Marked digit number snake). Duplication halfway items age, fractional items decrease, and expansion are the three intrinsic activities. This greatly speeds up the overall process thanks to the quick snake design. A give free numerical task have the option to be developed utilize a top radix number arrangement, for example, QSD viper. In QSD, every one number can be address by a digit starting around 3 to 3. With consistent deferment and less multifaceted nature, pass on complimentary development as well as distinct exercises on incalculable, such as 64, 128, or more, can be carried out. A reversible Vedic multiplier combines a QSD Quaternary Signed digit number adder viper with a transformation section for quaternary to paired change in the proposed multiplier configuration. The recommendation shows a most outrageous speed upgrade.

P. Dalmia et al. [4], a novel adder based on the Quaternary Signed digit number system is included in the high-speed Vedic multiplier that is presented in this paper. It is based on the Urdhva Tiryagbhyam sutra of Vedic mathematics. Multiplication has three inherent operations: partial products generation, reduction, and addition of partial products. As a result, a fast adder architecture significantly speeds up the process as a whole. An architecture for a quaternary logic adder that works with both binary and quaternary number systems is proposed. A given double string is first separated into quaternary digits of 2 pieces each followed by equal expansion decreasing the convey spread delay. Because the sum is directly generated in binary using the novel concept of an adjusting bit, the design does not require a radix conversion module. The Vedic multiplier that incorporates a QSD adder with a conversion module for quaternary to binary conversion, the Vedic multiplier that makes use of the Carry Select Adder, and a fast multiplication mechanism that is commonly used, such as the Booth multiplier, are contrasted with the design of the proposed multiplier. Synopsys Design Compiler synthesized each of these designs, which were developed using Verilog HDL. They have been acknowledged utilizing the open source NAN door 15nm innovation library. The proposition shows a limit of 88.75% speed improvement as for Multi Worth rationale based 128x128 Vedic multiplier while the least is 17.47%.

Simranjeet Singh Sudan et al. [5], the Arithmetic Logic Unit is an essential component of the computer system's central processing unit. The ALU is thought to be primarily composed of addition. Power and speed are the significant boundaries to be remembered for planning a snake. Addition, subtraction, and multiplication all experience delays in the Arithmetic Logic unit as a result of carry propagation, which introduces complexity and delay into the adder circuit. To diminish the postponement, convey free expansion is presented by QSD (Quaternary Marked Digit) Numbers. Using MIG and COG Reversible Logic Gates, a quick QSD Addition and Subtraction circuit is created in this paper. We can imagine from the outcomes meeting that Postponement gets decreased up to 83% for the QSD expansion and up to 90% for the QSD deduction.

Radhika Thakur et al. [6], data processing, control systems, and computation are the most common

applications for digital systems. They are having numberof benefits over simple framework: One advantage is the speed with which math is done. A number of different methods, including Wallace, Booth, and Binary Signed Digit (BSD) multiplication, are available for carrying out arithmetic operations. When doing arithmetic, the use of a binary number system results in carry, which slows down the process and causes delay. We are employing a higher radix number system, such as Quaternary Signed Digit (QSD), to solve this issue. The base 4 number system is the QSD system. Using decimal numbers, QSD can be expressed as: 0, 1, 2 and 3. It is in charge of carry-free math operations. In this paper we proposed a fast, low power QSD multiplier which can do convey free activity. Without any additional delay, this circuit can multiply signed and unsigned numbers. Additionally, this circuit is simpler and operates at a faster rate. The circuit is recreated on XilinxSPARTAN 3E-100or250 field programmable entryway cluster (FPGA) board utilizing Verilog HDL.

I. Simranjeet Singh et al. [7], as portable multimedia and communication become integrated into information processing and computing, the requirement for rapid speed digital circuits has increased. In terms of delay, carry propagation, high power consumption, and extensive circuitry complications, the primary flaw of current computers demonstrates a decline in the presentation of fundamental arithmetic calculations and operations—such as addition, subtraction, division, and multiplication. Because the carry propagation delay is crucial to the speed of any digital system, this system defines the addition and subtraction of the carry-free n digits. In this paper, we are giving the fundamental audit of papers for the QSD Viper/Subtractor.

Purva Agarwal et al. [8], different kinds of adders are used in modern computers to perform ALU (Arithmetic Logic Unit) operations like addition and subtraction with low delay and rapid output. QSD numbers are used to provide carry-free addition so that modern computers can perform ALU operations with less delay and increase speed. Subtraction can be performed using QSD numbers in the contemporary digital system's fast adder. The QSD numbers range from -3 to +3. We use a Reversible Logic Gate-based Full adder to perform 4 Bit QSD addition and subtraction in this paper. For performing quick activity, we are likewise presenting Pipelining so that deferral can be additionally diminished during the time spent option and deduction. We can see from the session's results that using a Reversible Logic Gate-based full adder with Pipelining reduced the delay by up to 92%.

III. PROBLEM STATEMENT

Moore law states that, the power required for processing just doubles in every 18 months. Irreversible technologies will dissipate a lot of heat and can reduce the life of the circuit. The reversible logic operations do not erase information and dissipate very less heat. As the technology shirking, tradeoff between performance and delay is very essential. The significant interest in delay reduction is consideration of high-performance circuits. Existing design minimizes the delay but at the cost of design metrics. The goal of this thesis is to design various components of a processor with tightly constraints design parameters, which are advantageous than the existing techniques. Reversible logic is a very prospective approach of logic synthesis for delay reduction in future computing technologies.

IV. REVERSIBLE GATE

Reversible rationale is picking up significance in zones of CMOS configuration on account of its low power dissemination. The customary entryways like AND, OR, XOR are all irreversible doors. Consider the instance of conventional AND entryway. It comprises of two inputs and one yield. Thus, one piece is lost every time a calculation is completed Hence it is impractical to decide a remarkable information that brought about the yield zero. With a specific end goal to make an entryway reversible extra information and yield lines are added so that a coordinated mapping exists between the info and yield. This keeps the loss of data that is fundamental driver of force dispersal in irreversible circuits. The information that is added to a m x n capacity to make it reversible is known as steady information (CI). Every one of the yields of a reversible circuit need not be utilized as a part of the circuit. Those yields that are not utilized as a part of the circuit is called as junk yield (GO). The quantity of trash yield for a specific reversible door is not altered.

The two main constraints of reversible logic circuit is

- Fan out not allowed
- Feedbacks or loops not allowed.

Several 4x4 gates have been described in the literature targeting low cost and delay which may be implemented in a programmable manner to produce a high number of logical calculations. The DPG gate produces the following logical output calculations:

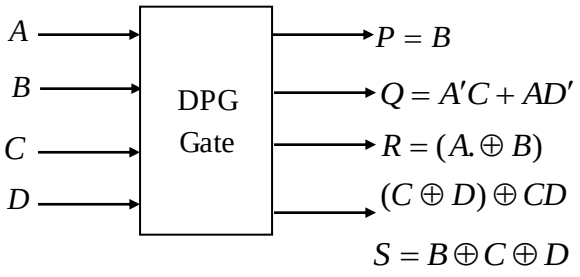

Figure 1: DKG Gate

$$P = B \tag{1}$$

$$Q = A'C + AD' \tag{2}$$

$$R = (A. \oplus B)(C \oplus D) \oplus CD \tag{3}$$

$$S = B \oplus C \oplus D \tag{4}$$

V. EVALUTION PARAMETERS

Garbage Output
Unused output or extra output is not used to circuit is called garbage output.

Constant Input
The constant inputs either '0' or '1' defined in the input are known as ancilla input or constant input.

Number 4-input LUTs
LUT stands for look up table that reduces the complex mathematics calculations and provide the reduced processing time.

Number of Slices
How many areas are used in this circuit is called number of slices.

Number of IOBs
All input output port used in this circuit are combined called number of input output buffer switch.

Maximum Combinational Path Delay
Maximum delay for signal propagation is called the maximum combinational path delay.

VI. CONCLUSION

Therefore lowpower addition design has become a significant part of VLSI system design. Day by day new approach is being established to design low-power addition at technological, physical, circuit, and logic levels. Meanwhile, the addition is normally the slowest element in a system; the system's performance is analyzed by the performance of the multiplier. Additionally, multipliers are the most area-consuming unit in a design. So, optimizing the speed and area of a multiplier is a major design issue. Though, area and speed are usually contradictory restrictions so improving speed results in larger areas and viceversa. Similarly, the area and power consumption of a circuit is linearly interconnected. So a negotiation has to be done in the speed of the circuit for a superior improvement in reduction of area and power.

REFERENCES

[1] B Devika Rani and Dr S Govindarajulu, "Implementation of Modified Vedic Multiplier using on Quaternary Signed Digit Number System", Journal of Engineering Sciences, Vol 13 Issue 12,2022.

[2] Mohammed A. Al-Ibadi, "Hardware Implementation for High-Speed Parallel Adder for QSD 2D Data Arrays", International Conference on Electrical, Communication, and Computer Engineering (ICECCE), IEEE 2020.

[3] K. Deepak "Design and Analysis of High Speed and Low Power Reversible Vedic Multiplier Incorporating with QSDN Adder" International Journal of Innovative Technology and Exploring Engineering (IJITEE) vol. 8 no. 4 pp. 273-279 February 2019.

[4] P. Dalmia V. Vikas A. Parashar A. Tomar and N. Pandey "Novel High speed Vedic Multiplier proposal incorporating Adder based on Quaternary Signed Digit number system" 31th International Conference on VLSI Design IEEE computer society 2017 pp. 289-294 2018.

[5] Simranjeet Singh Sudan and Manish Singhal, "MIG and COG Reversible Logic gate Based QSD Addition / Subtraction", International Conference on Computing, Communication and Automation (ICCCA2017).

[6] Radhika Thakur, Shruti Jain and Meenakshi Sood, FPGA Implementation of Unsiged Multiplier Circuit based on Quaternary Signed Digit Number System", IEEE Conference on Signal Processing, Computing and Control, IEEE 2017.

[7] I. Simranjeet Singh Sudan and Manish Singhal, "A review on basics of QSD number addition & subtraction", International Conference on Computing and Communication Technologies for Smart Nation (IC3TSN), IEEE 2017.

[8] Purva Agarwal and Pawan Whig, "Low Delay Based 4 Bit QSD Adder / Subtraction Number System By Reversible Logic Gate", 2016 8th

International Conference on Computational Intelligence and Communication Networks.

[9] Ameya N. Bankar, Shweta Hajare, "Design of Arithmetic Circuit Using Quaternary Signed Digit Number System", International Conference on Communication and Signal Processing, April 3-5, 2014, India.

[10] Tanay Chattopadhyay and Tamal Sarkar, "Logical Design of Quaternary Signed Digit Conversion Circuit and its Effectuation using Operational Amplifier", Bonfring International Journal of Power Systems and Integrated Circuits, Vol. 2, No. 3, December 2012.

[11] Krishna Murthy, Gayatri G, Manoj Kumar "Design of Efficient Adder Circuits Using Proposed Parity Preserving Gate" VLSICS Vol.3, No.3, June 2012.

[12] M. D. Saiful Islam and Z. Begum, Reversible Logic Synthesis Of Fault Tolerant Carry Skip BCD Adder, Journal of Bangladesh Academy of Sciences, Vol. 32, No. 2, 193-200, 2008.

[13] M. K. Thomsen, R. Gluck, H. B. Axelsen, 2010, Reversible arithmetic logic unit for quantum arithmetic, Journal of physics A: Mathematical and Theoretical, 43 (2010) 382002 (10pp), doi: 10.1088/1751- 8113/43/38/382002.

[14] M. Haghparast, K. Navi, 2008: A Novel Fault Tolerant Reversible Gate For Nanotechnology Based Systems, Am. J. Applied Sci., 5(5), 519-523.

[15] B. Parhami, Fault Tolerant Reversible Circuits, Proc. Asilomar Conf. Signals, Systems, and Computers, Pacific Grove, CA,Oct.2006.

[16] Haghparast, M. and K. Navi, " A novel fault tolerant reversible gate for nanotechnology based systems". Am. J. Appl. Sci., 5(5).2008.

[17] Jayashree H V and Ashwin S, "Berger Check and Fault Tolerant Reversible Arithmetic Component Design", 978-1- 4799 - 8364-3/ 15/ $31.00 @ 2015 IEEE.

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