VLSI Architecture for Bidirectional Logic Gate Based on Higher Bit QSD Addition / Subtraction

Kanu Priya Singh[1], Prof. Satyarth Tiwari[2]

M. Tech. Scholar, Department of Electronics and Communication, Bhabha Engineering Research Institute, Bhopal[1]

Guide, Department of Electronics and Communication, Bhabha Engineering Research Institute, Bhopal[2]

Abstract- With the exponential increase of data processing and storage needs, there is a strong momentum to move to a higher radix logic/number system that can exterminate many limitations of the binary system is presented. Awaited saturation of Moore's law and the necessity to increase information density and processing speed in the future micro and nanoelectronic circuits and systems provide a strong background and motivation for the beyond-binary logic system. For low power and real-time applications, computationally intensive digital signal processing algorithms are implemented in Dedicated VLSI systems. The computation speed of a processor is highly dependent on these arithmetic units. In order to reduce the delay, carry-free addition is introduced by QSD (Quaternary Signed Digit) Numbers. In this paper, a fast QSD Addition and Subtraction circuit is designed by use of DPG Reversible Logic Gates.

Keywords:- Reversible Gate, DPG Gate, Quaternary Signed Digit (QSD), Xilinx Software

I. INTRODUCTION

This logic is a four-valued (radix-4) logic meaning that there are four possible values for each digit (0, 1, 2, and 3). Similar to binary logic there are also numbers of basic gates in the multi-valued logic world as presented [1, 2]. Depending on the radix and number of the variables used, different logic functions can be generated. The numbers of possible functions are,

$$F(r, n) = r^{r^n} \quad (1)$$

Where r = radix, n = number of variables. For quaternary (r = 4, n = 2) = 4294967296 logic operations. Therefore, large number of operations is possible while going to higher radix.

Some factors influence in determining the best radix usable is observed [3, 4]. Logically, in theory, higher radix will be better to represent as many numbers as possible. But, in the real-world, the restrictions of usability and availability of suitable devices limit the usage of higher radix-based MVL circuits is presented [5]. The following four factors internment the trade-offs in choosing appropriate radix.

Area: Increased data density of multiple valued logic circuits ensures that to reduce the area when compared to equivalent binary circuits. Every circuit stores additional information per bit. The remaining result is that a large number of data sets can be combined and implemented in a lesser area. Even though, at smaller circuits, the additional overhead of supplementary‖ logic increases the area when compared to their equivalent binary gates. Therefore, the area advantages can only be found in larger circuits [6, 7].

Logic replication due to binary logic spread is avoided in MVL circuits. Also, higher radices would tolerate the increased number of functions that can be implemented, making it easier for larger and more complex functions implementation is presented [8].

An additional advantage is the reduction of signal wires. The reduced wires would shrink the size of the chip and also recover the routability of the design. One of the serious challenges in the Deep Sub-Micron technologies is the routing bottleneck and also the fabrication of the proximity of the wires is illustrated [9]. The restrictions of the current fabrication equipment would create several manufacturing defects like shorting of the wires, opening of the wires, etc. producing a lot of part defects and yield loss.

So, reducing the number of wires would considerably improve the device manufacturability and area improvement. An important parameter to deliberate for any MVL circuits though is the interface logic to the traditional binary circuits. The interface needs level conversion to permit efficacious integration. Radix converters help to address the cross-region interface needs. The radix conversion is comparatively easy for radices which are the power of two. (Example: radix-2 (binary), radix-4 (quaternary) and radix-8, radix-16 etc.) The radix conversion process gets difficult and requires more careful handling for other radices like radix-3, radix-5, radix-6, radix-7, radix9, etc. Therefore, the higher

radix, the greater area is. Higher radix (above 5) would improve the area. But the radices which are not in the power of two tend to need more complicated interface logic than for the radices which are the power of two.

Signal-to-Noise Ratio: Several voltage values are used to denote various logic levels used in MVL circuits. Higher radix would mean an increased number of logic levels. Every logic level shall have a voltage source. And the utmost important issue is how to ensure enough Signal-to-Noise Ratio that assurance the circuit operation in the existence of noise is presented [10, 11]. Noise in the signals can be affected by numerous factors in the circuits like power supply noise, cross-coupling noise, etc.

II. REVERSIBLE GATE

Reversible rationale is picking up significance in zones of CMOS configuration on account of its low power dissemination. The customary entryways like AND, OR, XOR are all irreversible doors. Consider the instance of conventional AND entryway. It comprises of two inputs and one yield. Thus, one piece is lost every time a calculation is completed Hence it is impractical to decide a remarkable information that brought about the yield zero. With a specific end goal to make an entryway reversible extra information and yield lines are added so that a coordinated mapping exists between the info and yield. This keeps the loss of data that is fundamental driver of force dispersal in irreversible circuits. The information that is added to a m x n capacity to make it reversible is known as steady information (CI). Every one of the yields of a reversible circuit need not be utilized as a part of the circuit. Those yields that are not utilized as a part of the circuit is called as junk yield (GO). The quantity of trash yield for a specific reversible door is not altered.

For all the aspects, radix-2 (binary) is chosen as a reference. As can be seen from this evaluation, radices above 4 would have an exponential cost increase due to the cost factors discussed above. According to Jhamb & Mohan's (2021) analysis, the benefits of area and power keep getting better; the exponential cost would exclude the usage of higher radix MVL circuits with existing components and existing technology. Identifies that maybe the new and evolving technologies like Quantum devices would allow higher radix MVL circuits to be implemented at a lesser cost when compared with radix-2 circuits.

The two main constraints of reversible logic circuit is

- Fan out not allowed
- Feedbacks or loops not allowed.

Several 4x4 gates have been described in the literature targeting low cost and delay which may be implemented

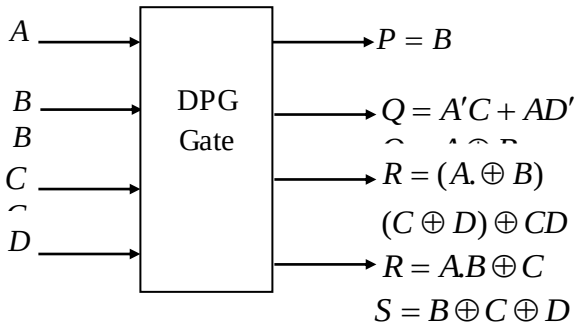


Figure 1: DKG

in a programmable manner to produce a high number of logical calculations. The DPG gate produces the following logical output calculations:

$$P = B \tag{1}$$

$$Q = A'C + AD' \tag{2}$$

$$R = (A. \oplus B)(C \oplus D) \oplus CD \tag{3}$$

$$S = B \oplus C \oplus D \tag{4}$$

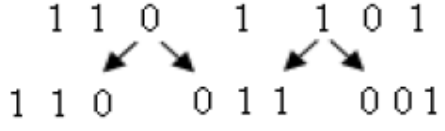
III. PROPOSED DESIGN

QSD NUMBER

1-digit QSD can be represented by one 3-bit binary equivalent as follows:

-3 = 101
-2 = 110
-1 = 111
0 = 000
1 = 001
2 = 010
3 = 011

So to convert *n*-bit binary data to its equivalent *q*-digit QSD data, we have to convert this *n*-bit binary data into *3q*-bit binary data. To achieve the target, we have to split the 3rd, 5th, 7th bit…. i.e. odd bit (from the LSB to MSB) into two portions. But we cannot split the MSB. If the odd bit is 1 then, it is split into 1 & 0 and if it is 0 then, it is split into 0 & 0. An example makes it clear, the splitting technique of a binary number $(1101101)_2$ is shown below:



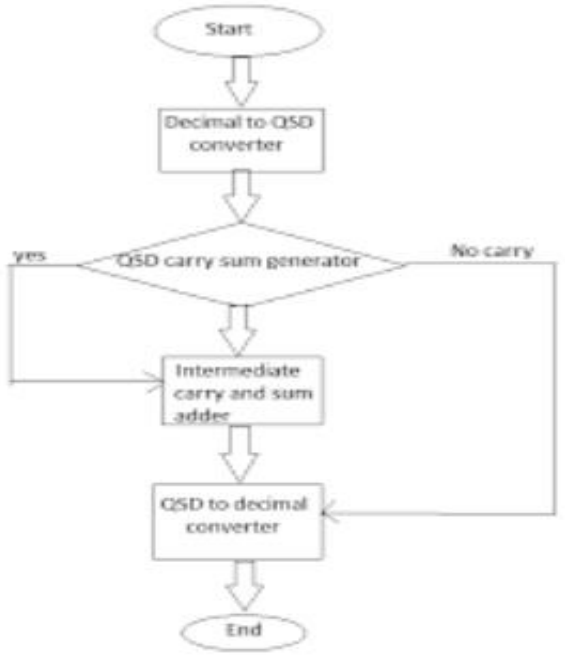


Figure 2: Flow Chart of Proposed Methodology

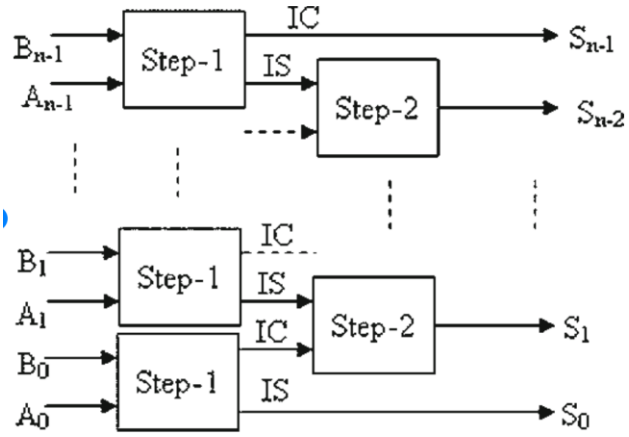


Figure 3: lock diagram of n-digit QSD carry free adder circuit

So we have to split the binary data (1)$q-$ times (as example, for conversion of 2-bit quaternary number, the splitting is 1 time; for converting 3-digit quaternary number the split is 2-times and so on). In each such splitting one extra bit is generated. So, the required binary bits for conversion to it's QSD equivalent (n) = (Total numbers of bits generated after divisions) – (extra bit generated due to splitting).

Table 1: Binary representation of Quaternary signed digit numbers

Serial Number	Quaternary signed digit	Binary Representation
1	-3	101
2	-2	110
3	-1	111
4	0	000
5	+1	001
6	+2	010
7	+3	011

IV. EVALUTION PARAMETERS

Garbage Output

Unused output or extra output is not used to circuit is called garbage output.

Constant Input

The constant inputs either '0' or '1' defined in the input are known as ancilla input or constant input.

Number 4-input LUTs

LUT stands for look up table that reduces the complex mathematics calculations and provide the reduced processing time.

Number of Slices

How many areas are used in this circuit is called number of slices.

Number of IOBs

All input output port used in this circuit are combined called number of input output buffer switch.

Maximum Combinational Path Delay

Maximum delay for signal propagation is called the maximum combinational path delay.

V. SIMULATION RESULT

Multi-valued logic systems are offering significant advantages like compact and easy development of circuits. A number of researchers have been working on the evolution of multi-valued logic systems. As an example, we have implemented discrete lossless transforms by redesigning these with a lifting scheme. We have also shown the design of a reversible computing architecture and implemented this using only reversible logic gates. While, these are still small systems, with further development it should be possible to use similar strategies to implement even larger systems.

Table II: Comparative Results of Existing Algorithm and Proposed Algorithm in 4-bit Adder/ Sub-tractor

Parameter	Previous Design	Proposed Reversible Adder/ Sub-tractor
No. of Gates	44	40
Garbage Output (GO)	8	8
Quantum Cost	28	24

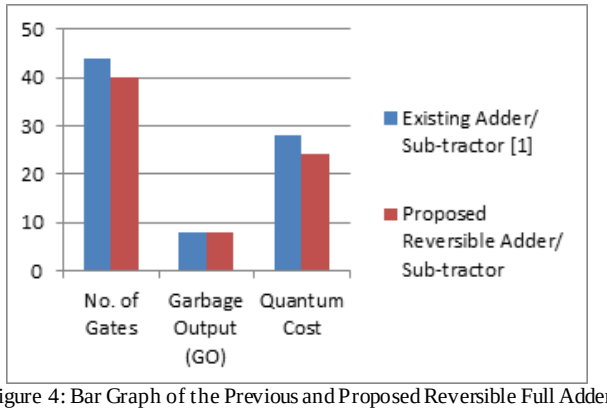


Figure 4: Bar Graph of the Previous and Proposed Reversible Full Adder

Table 3: Comparative Results of Existing Algorithm and Proposed Algorithm in 8-bit Adder Sub-tractor

Parameter	Previous Design	Proposed Reversible Adder/ Sub-tractor
No. of Gates	88	80
Garbage Output (GO)	16	16
Quantum Cost	56	48

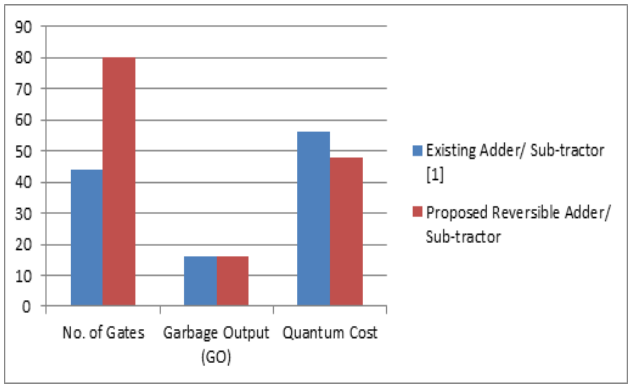


Figure 5: Bar Graph of the Previous and Proposed Reversible Full Sub-tractor

Table 4: Comparative Results for higher bits

Parameters	No. of Gates	GO	QC
16-bit	160	32	96
32-bit	320	64	192
64-bit	640	128	384
128-bit	1280	256	768

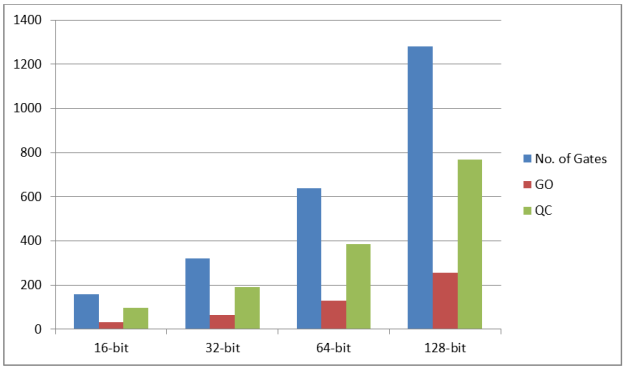


Figure 6: Bar Graph of the Previous and Proposed Reversible Full Sub-tractor

VI. CONCLUSION

The basic building blocks of all digital electronic circuits and microprocessor-based systems are made from digital logic gates. They can be intersected together to form moreover combinational logic circuits which are fully dependent on any external input signals applied to it or sequential logic circuits which are dependent on its present stable state, feedback of its output, as well as any external input signals that may trigger a switching event. A noticeable advantage of a quaternary illustration from binary is the economy of digits. Quaternary design admits sign convention also. The weakness of binary adders can be reduced by increasing the range of the numbers used. A signed number system can be used for this purpose. Signed digit numbers allow redundancy of numbers which permits the opportunity of carry-free addition, but the signed digit number system tolerates limited carry propagation with some complex addition process that involves large for its employment.

REFERENCES

[1] B Devika Rani and Dr S Govindarajulu, "Implementation of Modified Vedic Multiplier using on Quaternary Signed Digit Number System", Journal of Engineering Sciences, Vol 13 Issue 12,2022.

[2] Mohammed A. Al-Ibadi, "Hardware Implementation for High-Speed Parallel Adder for QSD 2D Data Arrays", International Conference on Electrical, Communication, and Computer Engineering (ICECCE), IEEE 2020.

[3] K. Deepak "Design and Analysis of High Speed and Low Power Reversible Vedic Multiplier Incorporating with QSDN Adder" International Journal of Innovative Technology and Exploring Engineering (IJITEE) vol. 8 no. 4 pp. 273-279 February 2019.

[4] P. Dalmia V. Vikas A. Parashar A. Tomar and N. Pandey "Novel High speed Vedic Multiplier proposal incorporating Adder based on Quaternary Signed Digit number system" 31th International Conference on VLSI Design IEEE computer society 2017 pp. 289-294 2018.

[5] Simranjeet Singh Sudan and Manish Singhal, "MIG and COG Reversible Logic gate Based QSD Addition /

Subtraction", International Conference on Computing, Communication and Automation (ICCCA2017).
[6] Radhika Thakur, Shruti Jain and Meenakshi Sood, FPGA Implementation of Unsiged Multiplier Circuit based on Quaternary Signed Digit Number System", IEEE Conference on Signal Processing, Computing and Control, IEEE 2017.
[7] I. Simranjeet Singh Sudan and Manish Singhal, "A review on basics of QSD number addition & subtraction", International Conference on Computing and Communication Technologies for Smart Nation (IC3TSN), IEEE 2017.
[8] Purva Agarwal and Pawan Whig, "Low Delay Based 4 Bit QSD Adder / Subtraction Number System By Reversible Logic Gate", 2016 8th International Conference on Computational Intelligence and Communication Networks.
[9] Ameya N. Bankar, Shweta Hajare, "Design of Arithmetic Circuit Using Quaternary Signed Digit Number System", International Conference on Communication and Signal Processing, April 3-5, 2014, India.
[10] Tanay Chattopadhyay and Tamal Sarkar, "Logical Design of Quaternary Signed Digit Conversion Circuit and its Effectuation using Operational Amplifier", Bonfring International Journal of Power Systems and Integrated Circuits, Vol. 2, No. 3, December 2012.
[11] Krishna Murthy, Gayatri G, Manoj Kumar "Design of Efficient Adder Circuits Using Proposed Parity Preserving Gate" VLSICS Vol.3, No.3, June 2012.
[12] M. D. Saiful Islam and Z. Begum, Reversible Logic Synthesis Of Fault Tolerant Carry Skip BCD Adder, Journal of Bangladesh Academy of Sciences, Vol. 32, No. 2, 193-200, 2008.
[13] M. K. Thomsen, R. Gluck, H. B. Axelsen, 2010, Reversible arithmetic logic unit for quantum arithmetic, Journal of physics A: Mathematical and Theoretical, 43 (2010) 382002 (10pp), doi: 10.1088/1751-8113/43/38/382002.
[14] M. Haghparast, K. Navi, 2008: A Novel Fault Tolerant Reversible Gate For Nanotechnology Based Systems, Am. J. Applied Sci., 5(5), 519-523.
[15] B. Parhami, Fault Tolerant Reversible Circuits, Proc. Asilomar Conf. Signals, Systems, and Computers, Pacific Grove, CA,Oct.2006.
[16] Haghparast, M. and K. Navi, " A novel fault tolerant reversible gate for nanotechnology based systems". Am. J. Appl. Sci., 5(5).2008.
[17] Jayashree H V and Ashwin S, "Berger Check and Fault Tolerant Reversible Arithmetic Component Design", 978-1- 4799 - 8364-3/ 15/ $31.00 @ 2015 IEEE.

.