Optimized Analysis of Reversible ALU based on Arithmetic and Memory Unit

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Abstract- Reversible computing spans computational models that are both forward and backward deterministic. These models have applications in program inversion and bidirectional computing, and are also interesting as a study of theoretical properties. In this paper, investigate reversible arithmetic logic unit (ALU) computing systems to physical gate-level implementation. Arithmetic operations are a basis for many computing systems, so a proposed the design of adder, sub-tractor, multiplexer, multiplier, comparator and memory element i.e. delay flip flop (D_FF) work towards a reversible circuit. The adder and sub-tractor circuit consist of DKG gate, multiplexer circuit consist of R gate, multiplier consist of toffoli, Peres and HNG gate, comparator consist of BJN gate and D_FF consist of Feynman and Fredkin gate. In all design implemented Xilinx software and simulated VHDL text bench.

Keywords—Reversible Gates, Arithmetic Logic Unit, Ancilla Input, Delay

I. INTRODUCTION

Quantum Computation and Quantum Information is the study of the information processing tasks that can be accomplished using Quantum mechanical systems. Quantum mechanics is a mathematical framework or set of rules for the construction of physical theories. Quantum computation taught us to think physically about computation, and this approach yields many new and exciting capabilities for information processing and communication. In the broadest terms, any physical theory, not just Quantum mechanics, may be used as the basis for a theory of information processing and communication. One of the messages of Quantum computation and information is that new tools are available for those problems that are relatively more difficult or impossible to solve on Classical computers. Quantum computing believes that what is computable and what is not computable is limited by the Laws of physics [1]. Traditional computer science is based on Boolean logic and algorithms. Its basic variable is a bit with two possible values, 0 or 1. These values are represented in the computer as stable saturated states off or on. Quantum mechanics offer a new set of rules that go beyond this classical paradigm [2]. The basic variable is now a qubit, represented as a vector in a two dimensional complex Hilbert space. $|0\rangle$and $|1\rangle$ form a basis in this space. The logic that can be implemented with such qubits is quite distinct from Boolean logic, and this is what has made Quantum computing exciting by opening new possibilities. A related historical strand contributing to the development of quantum computation and quantum information is the interest, dating to the 1970s, of obtaining complete control over single Quantum systems [3]. Applications of Quantum mechanics prior to the 1970s typically involved a gross level of control over a bulk sample containing an enormous 4 number of Quantum mechanical systems, none of them directly accessible. Since the 1970s many techniques for controlling single Quantum systems have been developed. For example, methods have been developed for trapping a single atom in an 'atom trap', isolating it from the rest of the world and allow us to probe many different aspects of its behavior with incredible precision [4]. Quantum computation and Quantum information provide a useful series of challenges at varied levels of difficulty for people devising methods to better manipulate single quantum systems, and simulate the development of new experimental techniques. The ability to control single quantum systems is essential if we are to harness the power of quantum mechanics for applications to Quantum computation and Quantum information.

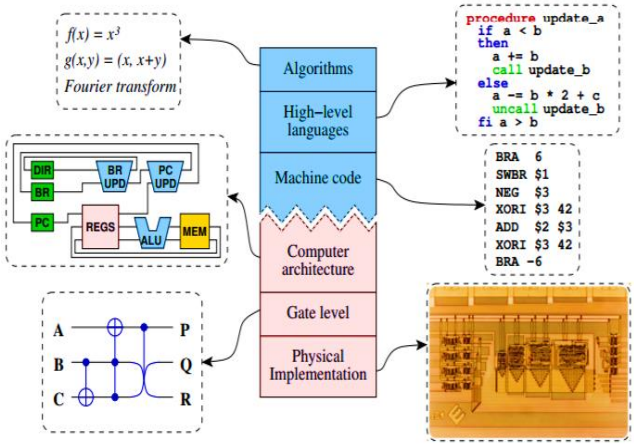

Figure 1: Tower of reversible computing system

Despite this intense interest, efforts to build Quantum information processing systems have resulted in modest success to date. Small Quantum computers, capable of doing dozens of operations on a few qubits represent the state of the art in Quantum computation. However, it remains a great challenge to physicists and engineers to develop techniques for making large-scale Quantum information processing a reality [5]. In his 1961 paper, Landauer wrote that "we shall label a machine as being logical reversible, if and only if all its individual steps are logically reversible" [6]. This is a very grand challenge and we know from Bennett (and later work) that, theoretically, such machines do exist – even when we add the requirement that the final result must not include garbage. But is it possible to realize such machines in practice and can it is done with the fabrication technology that exists today? And will we actually be able to achieve the expected reduced heat dissipation? The MicroPower research project [7], which started in 2009, has as objective to develop a proof-of-concept reversible computing system and the computer science theory behind it. To do this all parts of the reversible computation tower (Figure 1.1) must be

investigated. More specifically, the project investigates whether reversible computing can be applied in a power-limited application (specifically hearing aids) with the future hope to either reduce power consumption or increase functionality [8].

II. ARITHMETIC LOGIC CIRCUITS

Arithmetic operations lie at the foundation of most computing systems and good logical implementations of these are important. Improvements to arithmetic circuits can result in improvements to the entire computing system. In a garbage-free reversible computing system it is especially important that the arithmetic circuits are also garbage-free, but how to do this is not always obvious, and history shows that rethinking our current knowledge can be necessary.

The adder that Feynman proposed [9] was a reversible embedding of the ripple-carry adder. Though addition is an injective function if one of the inputs is kept, the conventional ripple-carry structure is not reversible. The problem lies in the use of the full-adder circuit, because it is not possible to calculate both the sum and the carry without copying one of the inputs. You can say that there is an overlap in the information contained in the two results and these results in a garbage bit.

2.1 2×1 Reversible Multiplexer

In RM 3×3 programmable structure is presented in Fig. 2. R gate is having three inputs and three outputs with a QC of 4. This gate implementation produces the outputs as P =A, Q = AB and R = A'B+AC. This particular gate is used for the realization of implement reversible combinational circuits (RCC) such as the 2×1 RM.

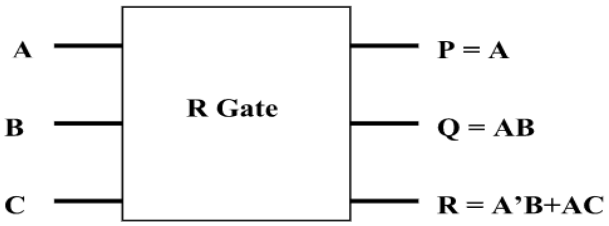

Figure 2: Block Diagram of R Gate

4×1 RM is circuit implementation shown in Fig. 3.3 is done in a reversible manner by using reversible logic R gate. The implemented design consisting of two selection lines S_0 and S_1, our input signal of the multiplexer are I_0, I_1, I_2, I_3, and Z as output line $Z = S_1'S_0'I_0 + S_1'S_0 I_1 + S_1 S_0' I_2 + S_1 S_0 I_3$. RM 4×1 in three R gate use.

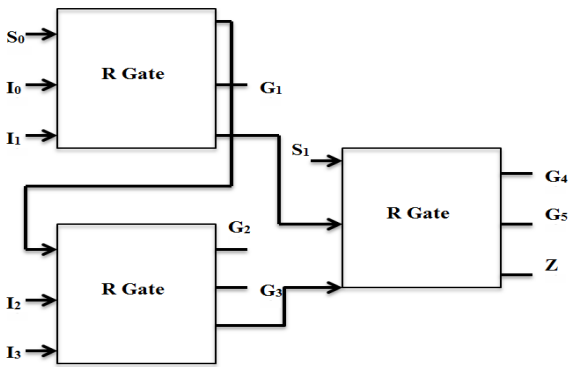

Figure 3: Implemented 4×1 RM

2.2 Reversible Comparator Circuit

Another common and very useful combinational logic circuit is that of the Digital Comparator circuit. Digital or Binary Comparators are made up from standard AND, NOR and NOT gates that compare the digital signals present at their input terminals and produce an output depending upon the condition of those inputs is shown in figure 4.

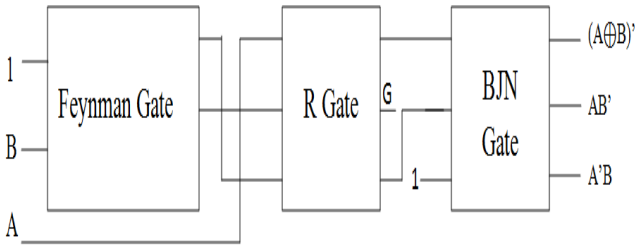

Figure 4: Proposed Comparator using BJN Gate

For example, along with being able to add and subtract binary numbers we need to be able to compare them and determine whether the value of input A is greater than, smaller than or equal to the value at input B etc. The digital comparator accomplishes this using several logic gates that operate on the principles of Boolean Algebra as shown in figure 5.

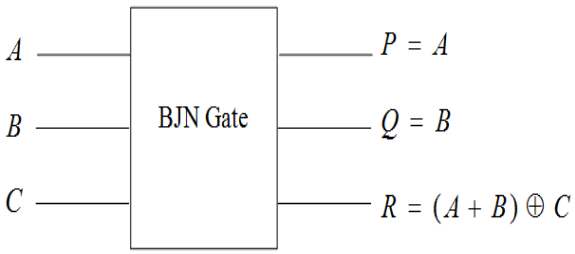

Figure 5: Block Diagram of BJN Gate

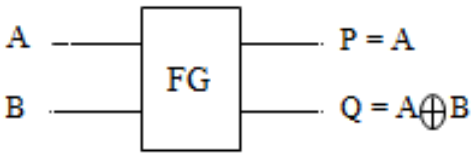

Figure 6: Block Diagram of Feynman Gate

2.3 Memory D_FF

In this section we design a reversible positive level triggered D Flip-Flop. The truth table of a D Flip-Flop is shown in Table I. The design of the D Flip-Flop is shown in Figure 7. A Fredkin gate is used as a 2:1 mux and the Feynman gate is used for getting fan-out of 2.

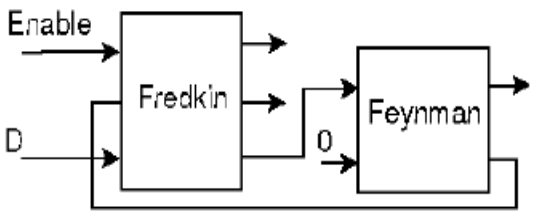

Figure 7: Reversible D Flip-Flop

Table I: D_FF

Enable	D	Q
1	0	0
1	1	1
0	x	Q(t-1)

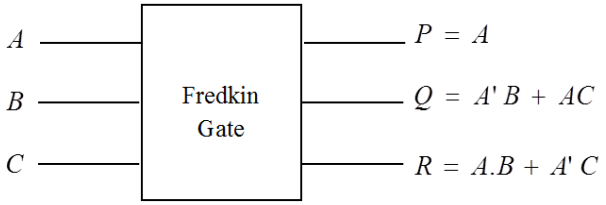

Figure 8: Block Diagram of Fredkin Gate

2.4 Reversible Adder/Sub-tractor

The N-bit Adder/ Sub tractor utilizes the DKG gate and DKG gate to produce two logical calculations: Adder and Sub tractor. DKG is a 1×1 reversible gate whose block diagram is shown in figure 9.

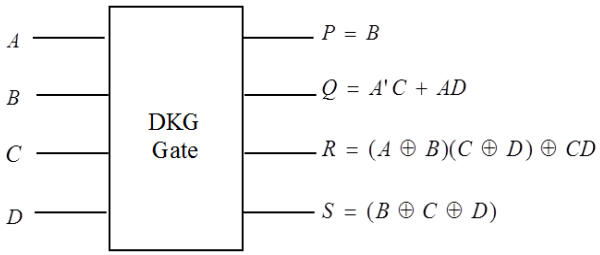

Figure 9: Block Diagram of DKG Gate

Table II: Reversible 4-bit Adder/ Sub tractor Opcodes and Logical Result for Proposed Design

A	X_0	Y_0	C_{in}	G_2	G_1	C_1	S_0/D_0
0	0	0	0	0	0	0	1/-
0	0	0	1	0	1	0	-/0
0	0	1	0	0	0	1	0/-
0	0	1	1	0	1	1	1/-
0	1	0	0	1	0	0	-/1
0	1	0	1	0	0	0	1/-
0	1	1	0	1	0	1	-/1
0	1	1	1	1	0	1	0/-
1	0	0	0	1	1	1	-/1
1	0	0	1	0	1	0	0/-
1	0	1	0	0	1	0	-/1
1	0	1	1	1	1	0	1/-
1	1	0	0	1	0	1	-/1
1	1	0	1	0	0	1	0/-
1	1	1	0	1	1	0	-/1
1	1	1	1	1	1	0	0/-

III. PROPOSED METHODOLOGY

The architecture of the proposed reversible processor is shown in Figure 10. In this figure design the overall structure of the reversible ALU has been divided into small components.

- Layout the data bus to handle all of the operations of the reversible ALU.
- Design the reversible realizations of the multiplexer.
- Design the reversible memory circuits such as d_ff and comparator.
- Design the arithmetic circuits such as multiplier, adder and sub-tractor.

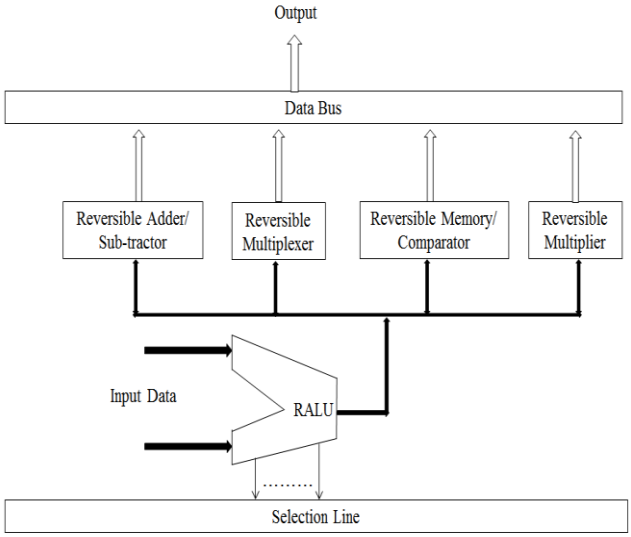

Figure 10: Flow Chart of Proposed Arithmetic Logic Unit

IV. SIMULATION RESULT

More specifically, we have developed new circuits for addition and are working towards a general multiplication circuit. We have also combined multiple operations together to implement a reversible arithmetic logic unit.

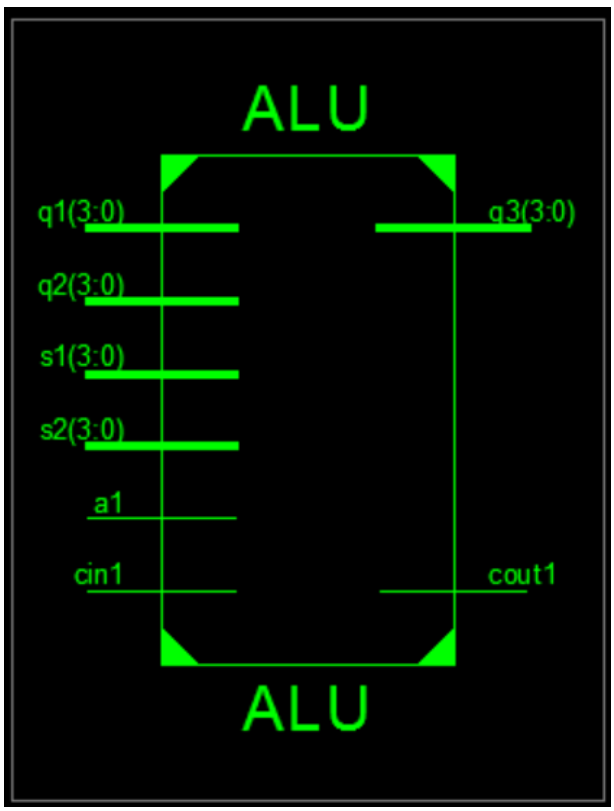

Figure 11: View Technology Schematic of 4-bit Reversible ALU

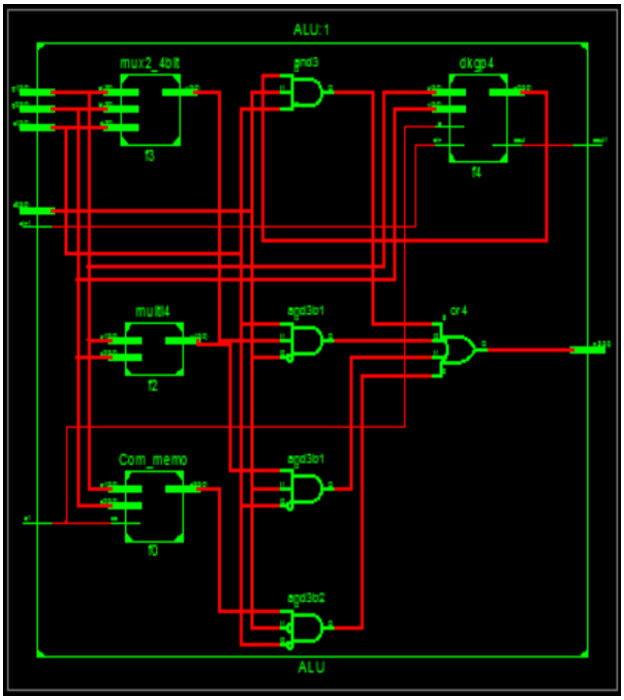

Figure 12: RTL view of 4-bit Reversible ALU

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Device utilization summary:
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Selected Device : 3s50pq208-5

 Number of Slices:                       29  out of    768     3%
 Number of 4 input LUTs:                 52  out of   1536     3%
 Number of IOs:                          23
 Number of bonded IOBs:                  23  out of    124    18%

Timing Summary:
---------------
Speed Grade: -5

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 13.840ns
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Figure 13: Simulation Result for 4-bit Reversible ALU

This is 2×1 RM simulation R_gate view technology schematic (VTS) in Fig. 14. It is first step 2×1 RM in I0 and I1 is input and S0 in select line .G1and G2 is garbage output and Y is final output.

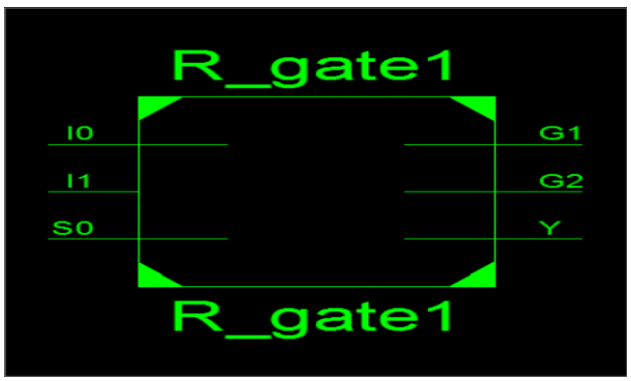

Figure 14: VTS for 2×1 RM

After first step, in this work get RTL view, this is second step R_gate 1:1. RTL view of the R _gate 1:1 in three AND gate used and2 (2), and2 b1, and one or2 gate.

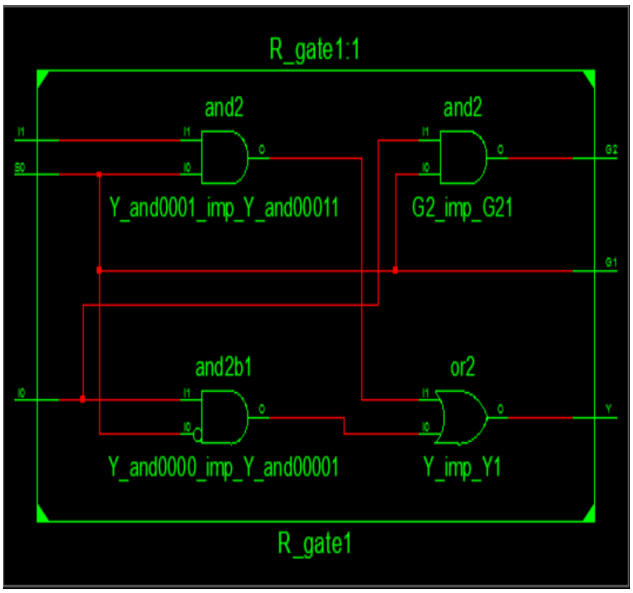

Figure 15: RTL for 2×1 RM

After first and second step get third step this is test bench (TB) representation. S0=1 (select line),input I0=0,input I1=1,garbage output g1=1,garbageoutput g2=0 and final output y=1.

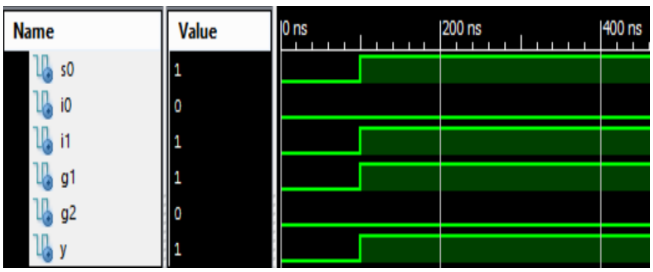

Figure 16: VHDL TB for 2×1 RM

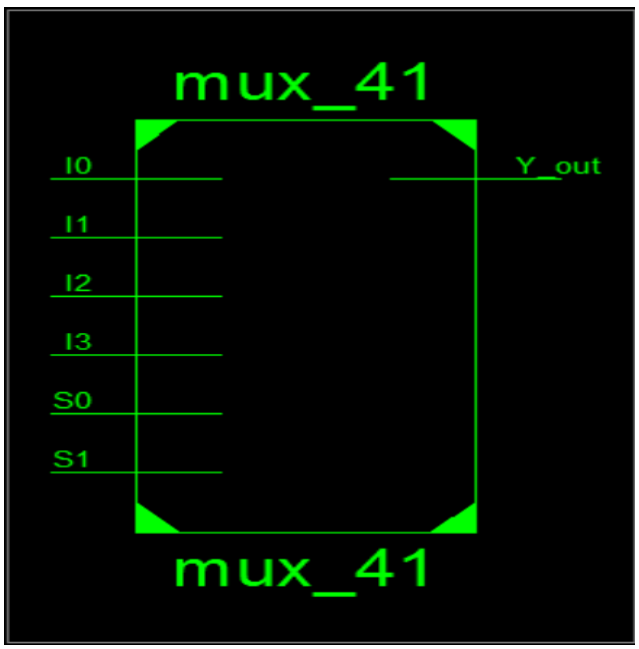

Figure 17: VTS for 4×1 RM

It is 4×1 RM view technology there four input I0, I1, I2, I3 and two select line y is out.

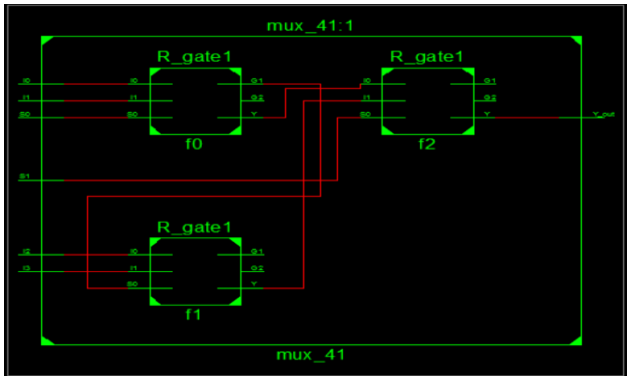

Figure 18: RTL for 4×1 RM

Second step in RTL view of the 4×1 RM.in RTL view four input I1, I2, I3, I0 and One output y.in second step show number of mux in RTL view with connection.

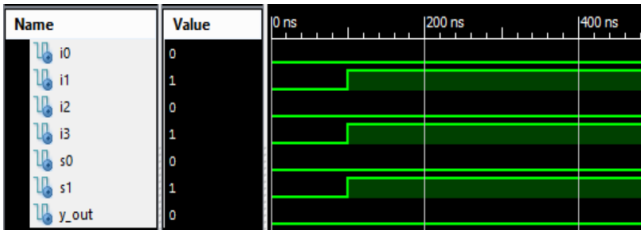

Figure 19: VHDL TB for 4×1 RM

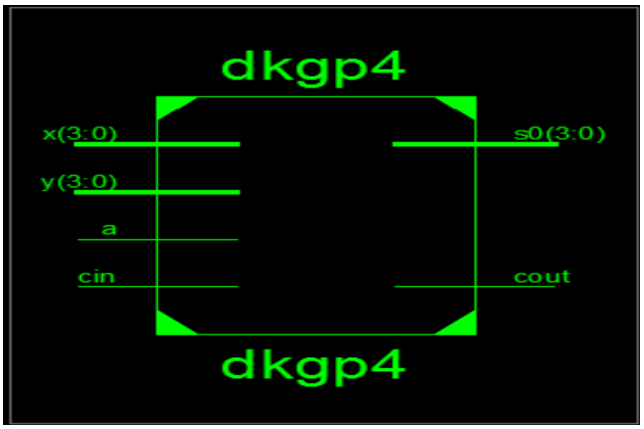

Figure 20: VTS for 4-bit Reversible Adder/Sub-tractor

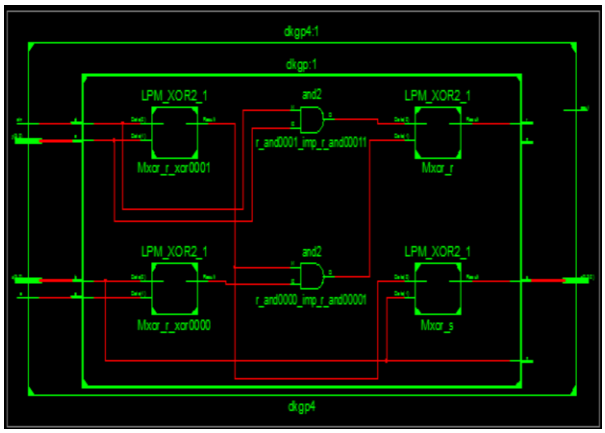

Figure 21: RTL for 4-bit Reversible Adder/Sub-tractor

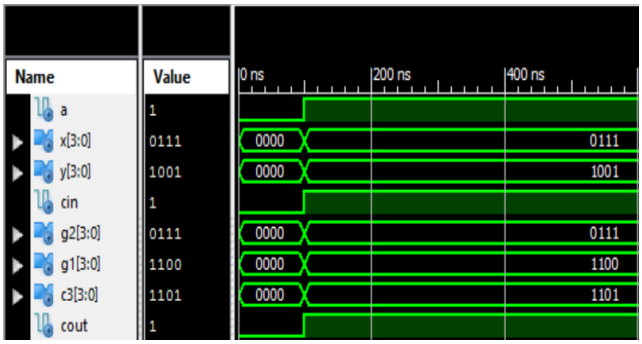

Figure 22: Output waveform of the 4-bit Adder/ Sub-tractor Circuit

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Device utilization summary:
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Selected Device : 3s50pq208-5

 Number of Slices:                        4  out of    768     0%
 Number of 4 input LUTs:                  8  out of   1536     0%
 Number of IOs:                          15
 Number of bonded IOBs:                  15  out of    124    12%
Timing Summary:
---------------
Speed Grade: -5

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 12.383ns
```

Figure 23: Simulation Result for 4-bit Reversible Adder/ Sub-tractor

V. CONCLUSION

In the proposed work the ALU had two fixed select lines, and produced the following logical outputs: ADDER/SUBTRACTOR, MULTIPLEXER, MULTIPLIER and MEMORY ELEMENT/COMPARATOR. Hence in this design we have proposed a design to calculate the simulation result i.e. number of slices, look up table and delay.

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