Reduce THD and High Gain Solar Power Generation with Seven-Level BANPC Inverter

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***Abstract*—**This study proposes a seven-level power conversion system for a solar power generation system. This seven-level power conversion system consists of a cascade DC–AC inverter. The cascade DC–AC inverter comprises a full-bridge inverter and a T-type inverter. To reduce the dc-link voltage, a recent topology that enhanced the voltage gain from half to unity has been presented. In this letter, an alternative ANPC topology is established by using two T-type inverters. Two floating capacitors with self-voltage balancing capability are integrated to achieve a voltage-boosting gain of 1.5. In addition, the proposed topology is capable of generating seven voltage levels. Its operation is validated through circuit analysis followed by experimental results of a prototype.

***Keywords:* -** Solar Power, PV Array, Inverter, Seven Level, Active Neutral Point Clamped

I. INTRODUCTION

The solar energy is becoming more important since it produces less pollution and the cost of fossil fuel energy is rising, while the cost of solar arrays is decreasing. The growing energy demand coupled with the possibility of reduced supply of conventional fuels, along with growing concerns about environmental preservation, has driven research and development of alternative energy sources that are cleaner, renewable and that produce little environmental impact. Among the alternative sources the electrical energy from PV is currently regarded as the natural energy source more useful, since it is free, abundant, and clean, distributed over the earth and participates as a primary factor of all other processes of energy production on earth.

The increasing need for electrical energy sources encourages people to use renewable electricity. The most popular renewable energy is photovoltaic. Photovoltaic is a component that utilizes sunlight to produce voltage.

Solar energy is a renewable energy that features easy installation, easy maintenance, no moving parts, no noise and negligible pollution. The cost of power generation from the solar power generation system (SPGS) is also decreasing so solar power is finding an increasing number of applications. The efficiency of SPGS is important because there is income from the generation source. The power efficiency is improved by improving solar cells and the power conversion interface. More new materials with high efficiency are still developed [1]. At the same time, many new power electronic components and power conversion topology have been proposed [2–3]. This study concerns power conversion topology. A power conversion interface suffers power losses from passive power devices and active power devices. The passive power devices include capacitors and inductors and they are used for voltage and current filtering. The power losses from passive power devices occur mainly because of ripples in voltage and current. The power losses from active power devices are due to conduction losses and switching losses. The conduction losses depend on the voltage drops of active power devices and count of active power devices in the current loop. The switching power loss is proportional to the change in voltage and current for a switching process for an active power device [4].

The switching power losses for active power devices can be attenuated by decreasing the voltage change in the switching process. Furthermore, the power losses of passive power devices are also improved because the ripples in voltage and current are suppressed by decreasing the voltage change in the switching process. Multilevel power converters generate more voltage levels in the AC output voltage so there is a smaller change in the voltage in the switching process for active power devices [5]. Therefore, multilevel power converters have lower switching losses due to active power devices. The ripples in the voltage and current for passive power devices are also reduced so power losses are decreased and their capacity is reduced. However, conduction losses due to active power devices are increased because there are more active power devices in the current loop. The control circuit and drive circuit are also complicated [6].

THD is a measurement of the quality of voltage or current. In normal conditions the output voltage form is a sinusoidal wave where THD is close to or equal to 0 (zero). THD is the percentage value between the total components of harmonics with its fundamental components. If the THD value is greater than the THD standard, it can lead to the destruction of electrical equipment, the burning of cable/conductor, overheat on the electric motor, and error on the electromechanical measurement of KWH meter [7].

II. MULTI LEVEL CONVERTER

Figure 1 shows the multilevel converter modulation methods. The modulation control schemes for the multilevel inverter can be divided into two categories, fundamental switching frequency and high switching frequency PWM such as multilevel carrier-based PWM, selective harmonic elimination and multilevel space vector PWM Multilevel SPWM needs multiple carriers. Each DC source needs its own carrier. Several multi-carrier techniques have been developed to reduce the distortion in multilevel converters, based on the conventional SPWM with triangular carriers. Some methods use carrier disposition and others use phase shifting of multiple carrier signals. By generalizing, for an 'n' level multilevel inverter, (n-1) carriers are needed. The implementation of the various carrier PWM techniques that is possible for multi-level inverters are [3]-[6]:

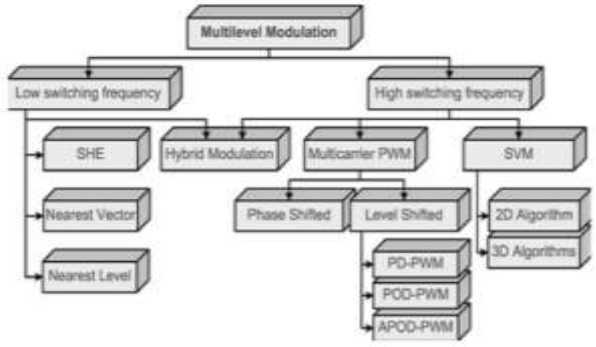

Figure 1: Multilevel converter modulation methods

Level Shifted PWM (LSPWM)

This modulation method is especially useful for NPC converters, since each carrier can be easily associated to two power switches of the converter. LSPWM leads to less distorted line voltages since all the carriers are in phase compared to PSPWM [8]. In addition, since it is based on the output voltage levels of an inverter, this principle can be adapted to any multilevel converter topology. However, this method is not preferred for CHB and FC, since it causes an uneven power distribution among the different cells. This generates input current distortion in the CHB and capacitor unbalance in the FC compared to PSPWM [3]-[6]. Figure 6 shows the LS-PWM carrier arrangements.

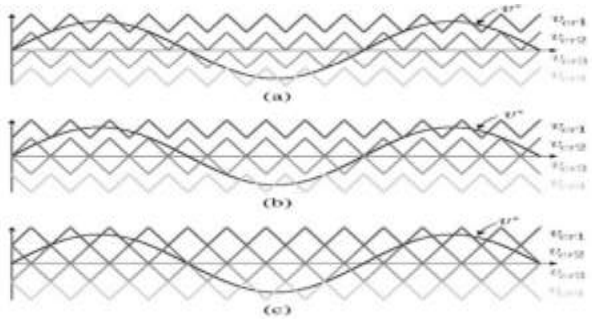

Figure 2: LS-PWM carrier arrangements: (a) PD, (b) POD, and (c) APOD.

Phase Shift Pulse Width Modulation

PWM signals are pulse trains which are applied to the gate of switches to perform the operation of converter. The pulse trains are fixed frequency and magnitude and variable pulse width [5]. There is one beat of settled extent in each PWM period. In any case, the width of the beats changes from period to period as indicated by a regulating signal. At the point when a PWM flag is connected to the entryway of a power transistor, it causes the turn on and kills interims of the transistor to change starting with one PWM period then onto the next PWM period as indicated by the same regulating signal and thus working of converter begins. The recurrence of a PWM flag must be substantially higher than that of the regulating signal, the major recurrence, with the end goal that the vitality conveyed to the heap depends generally on the tweaking signal. The control of yield voltage is done utilizing beat width balance.

This technique uses a set of carriers that are all phase-shifted. The four triangular carriers are phase-shifted by 90^{o}. Using the same sampling period, it has four times larger switching frequency than that of other techniques. This technique is specially conceived for FC and CHB converters. Since each FC cell is a two-level converter, and each CHB cell is a three-level inverter, the traditional bipolar and unipolar PWM techniques can be used, respectively. Due to the modularity of these topologies, each cell can be modulated independently using the same reference signal.

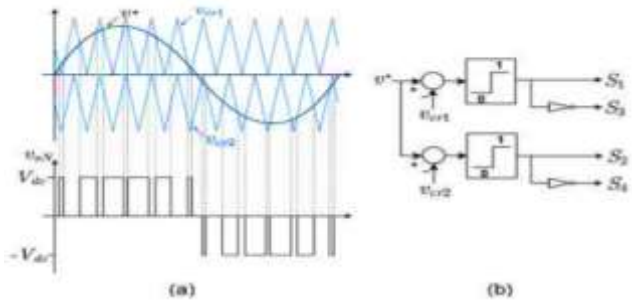

Figure 3: Phase Shift PWM

III. PV ARRAY

The photovoltaic cell converts the light energy into electrical energy depending on the irradiation of the sun and temperature in the atmosphere. Basically PVC is a PN junction diode [8] [4]. But in PN junction diode DCI AC source is needed to work, but here light energy is used as a source to produce DC output. PVC is a current control source not a voltage control source. The equivalent electrical circuit diagram of PVC is shown in the Figure 4.

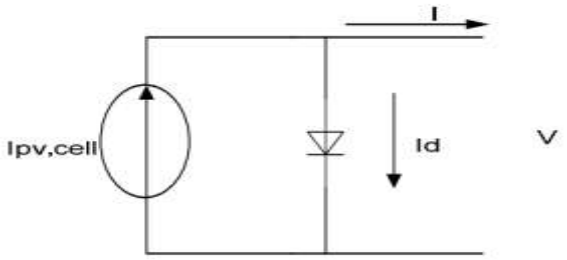

Figure 4: Show ideal photovoltaic cell equivalent circuit

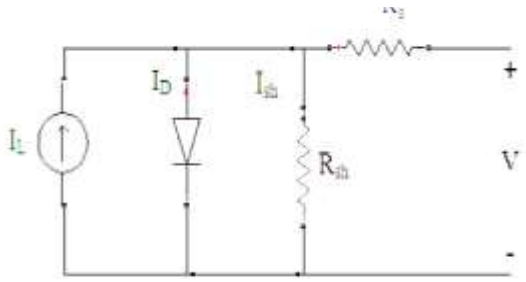

Figure 5: Equivalent Electrical Circuit of PVC

$$I_D = I_0[\exp(V + IR_S)/KT - 1] \quad (1)$$

Therefore PVC output current is given in equation 2.

$$I = I_L - I_D - I_{Sh} \quad (2)$$

$$I = I_L - I_0[\exp(q(V + IR_S))/KT - 1] - (V + IR_S)/R_{Sh} \quad (3)$$

Where I_D the diode is current, R_{sh} is the shunt resistance, I_L is the light generated current of solar array. Solar cell is basically a p-n junction fabricated in a thin wafer or layer of semiconductor. The electromagnetic radiation of solar energy can be directly converted electricity through photovoltaic effect. Being exposed to the sunlight, photons with energy greater than the band-gap energy of the semiconductor are absorbed and create some electron-hole pairs proportional to the incident irradiation. Under the influence of the internal electric fields of the p-n junction, these carriers are swept apart and create a photocurrent which is directly proportional to solar insolation. PV system naturally exhibits a nonlinear I-V and P-V characteristics which vary with the radiant intensity and cell temperature.

MPPT ALGORITHM:- Because of the lesser efficiency of photovoltaic array most of the energy, impacting over array gets wasted. The algorithm known as maximum power point tracking may be helpful to enhance the performance of solar panel. The MPPT algorithm works on principal of Thevenin, according which the power output of a circuit is maximum when impedance of circuit matches with the load of impedance. So now we have to match the impedance instead of tracking maximum power point.

There are different techniques used to track the maximum power point. Few of the most popular techniques are:

- Perturb and observe (hill climbing method)
- Incremental Conductance method
- Fractional short circuit current
- Fractional open circuit voltage
- Neural networks
- Fuzzy logic

Perturb and observe

The P&O algorithm and "hill-climbing", both names refer to the same algorithm depending on how it is implemented. The basic difference between these two is that Hill-climbing involves a deviation of the duty cycle of the power converter and in P&O anxiety on the operating voltage of the DC link between the PV array and the power converter takes place [3]. The deviation of duty cycle of the power converter is the modification of the voltage of DC link between the PV array and the power converter refer as Hill-climbing, so both names refer to the same technique. What should be the next perturbation is decided by considering the sign of the last perturbation and the sign of the last increment in the power.

The perturbation will remain in the same direction if power is incremented, and if power is decreased then next perturbation will be in the opposite direction. The process will be repeated until the point of maximum power will be reached. Then the operating point oscillates around the MPP.

Incremental conductance

The slope of the curve between power and voltage of PV module is the deciding factor in incremental conductance algorithm, if it is zero it shows point of MPP positive (negative) on the left of it and negative (positive) on the right.

- $\Delta V/\Delta P = 0$ at the MPP
- $\Delta V/\Delta P > 0$ on the left
- $\Delta V/\Delta P < 0$ on the right

The change of MPP voltage is identified by comparing the change of the power to increment of the voltage of current curve.

Fractional short circuit current

Fractional short circuit current method states that the ratio between array voltage at maximum power V_{MPP} to its open circuit voltage V_{OC} is nearly constant.

$V_{MPP} \approx k_1 V_{OC}$

The constant K_1 is having value between 0.71 to 0.78. Now the value of V_{MPP} can be calculate by periodically measuring V_{OC}. This method is simple and cheap to implement but its efficiency is relatively low due to the utilization of inaccurate values of the constant k1 in the computation of V_{MMP} .

Total Harmonic Distortion

The total harmonic distortion (THD or THDi) is a measurement of the harmonic distortion present in a signal and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency. Distortion factor, a closely related term, is sometimes used as a synonym.

In audio systems, lower distortion means the components in a loudspeaker, amplifier or microphone or other equipment produce a more accurate reproduction of an audio recording.

In radio communications, devices with lower THD tend to produce less unintentional interference with other electronic devices. Since harmonic distortion tends to widen the frequency spectrum of the output emissions from a device by adding signals at multiples of the input frequency, devices with high THD are less suitable in applications such as spectrum sharing and spectrum sensing.

In power systems, lower THD implies lower peak currents, less heating, lower electromagnetic emissions, and less core loss in motors.

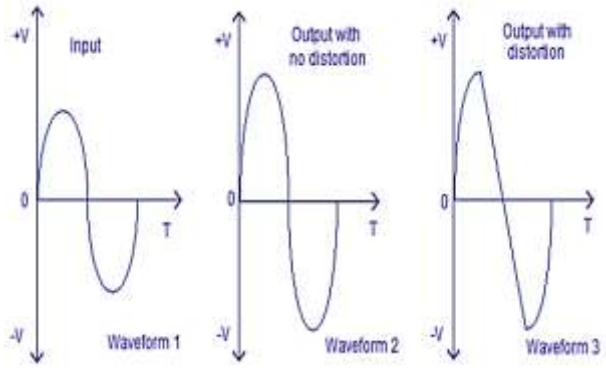

Figure 6: Output Waveform of Distortion

IV. PROPOSED METHODOLOGY

The proposed topology is called aDTT-7L BANPC following its circuit structure, which comprises two T-type inverters, as depicted in Fig. 7. Considering that all the power switches are metal-oxide-semiconductor field effect transistors, the proposed ANPC inverter requires only two additional power switches to those in the previous study [11]. Two floating capacitors (C_{F1} and C_{F2}) are integrated to achieve a voltage-boosting gain of 1.5. With the magnitude of each level is 0.5 V_{dc}, the proposed topology is capable of generating seven levels from −1.5 V_{dc} to 1.5 V_{dc}. Analysis of the proposed DTT-7L-BANPC inverter is illustrated. The floating capacitor C_{F1} is charged to V_{dc} when S4 and S9 are ON during 0.5 V_{dc} and−1.5 V_{dc}. In contrast, C_{F2} is charged to V_{dc} during 1.5 V_{dc} and −0.5 V_{dc}. The floating capacitors operate symmetrically for each half-cycle, which results in self-balancing of their voltages during operation.

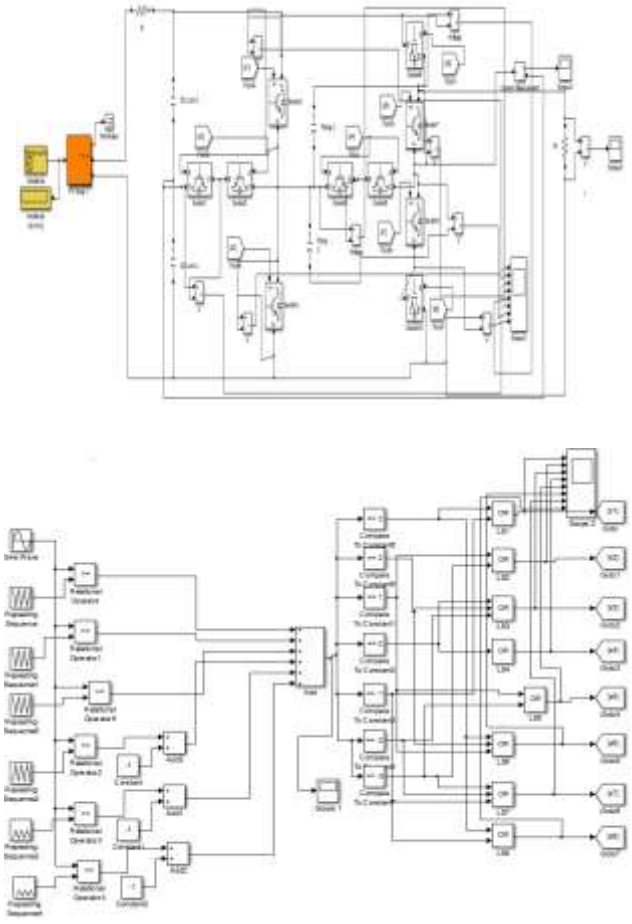

Figure 7: Simulation Model of Proposed Methodology

V. SIMULATION RESULT

The precomputed switching angles using selective harmonic elimination pulse width modulation (SHEPWM) were first considered to analyze the operation of the proposed topology. Fig. 8 shows that the average floating capacitor voltages is equal to the input voltage V_{dc} of 100 V. Seven distinct voltage levels with the magnitude of each level equal to 50 V were clearly observed.

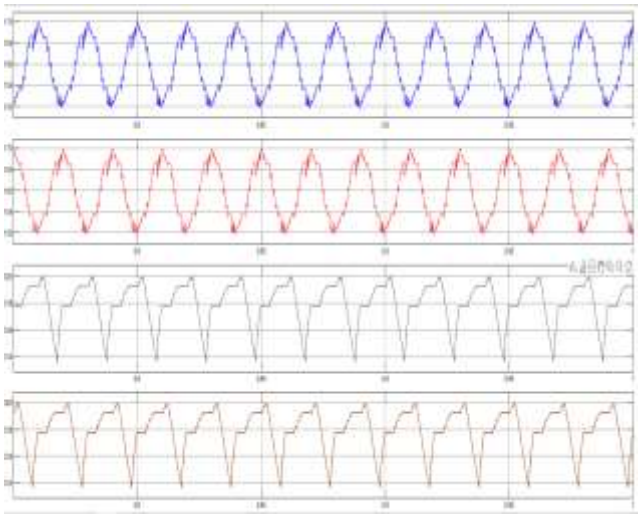

Figure 8: Output of Capacitor Voltage for Seven Level Inverter

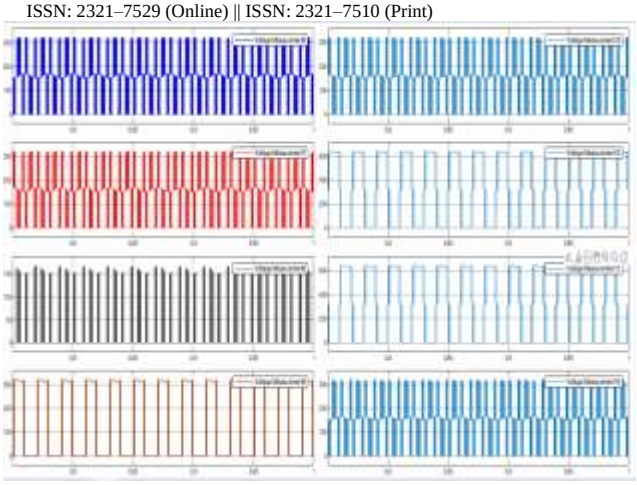

Figure 9: Switching Blocking Voltage

The voltage ripples of the floating capacitors were also measured. It is apparent from Fig. 10 that C_{F1} was charged during 50 and −150 V, discharged during 100 and 150 V, and constant elsewhere. Symmetrical operation for C_{F2} was observed such that it was charged during 150 and −50 V and discharged during −100 and −150 V. Good agreement between the experimental results and analysis conducted.

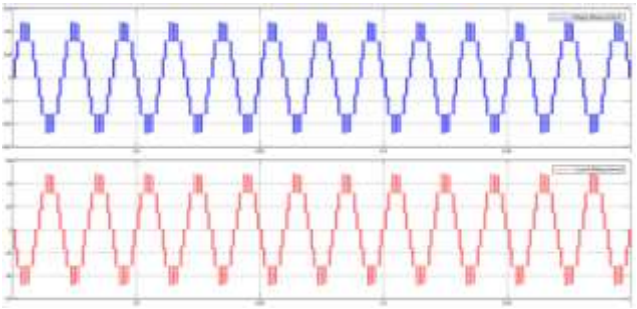

Figure 10: Output Voltage and Current of Seven Level Inverter

Table 1: Result Comparison

Parameters	Previous Topology		Proposed Topology
	3L Boost ANPC	5L Boost ANPC	DTT 7L Boost ANPC
Number of levels	3	5	7
Number of Switch	6	8	10
Maximum level (Vmax)	0.5 Vdc	1 Vdc	1.5 Vdc
Voltage Gain	0.5	1	1.5
Number of floating capacitors	0	1	2
Total Harmonic Distortion	18.45%	14.78%	11.86%

VI. CONCLUSION

A novel inverter topology, DTT-7L-BANPC, is reported in this letter. As the name implies, the proposed topology is capable of generating seven voltage levels with a voltage-boosting gain of 1.5. Self-voltage balancing of two floating capacitors was achieved during operation. The proposed topology was analyzed and tested. Experimental results validated its operation and feasibility. It is an alternative for a single-stage multilevel boost dc–ac power conversion system.

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