New Design of CMOS Current Comparator with reduced Delay Time and Marginal Power Consumption

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Abstract— **This work proposed the new CMOS comparator with marginal low power and reduced delay time suitable for precision biasing of op-amp with accepted power consumption and improved speed. Proposed circuit had been simulated in a proprietary 180 nm CMOS process, using Cadence Spectre Simulator and models. Current comparator circuit had impressed with current pulses ranging from micro-Amperes to Nano-Amperes and its delay time and Power consumption had been measured after simulation. By incorporating the effect of different capacitances of the CMOS the transient response confirms the reduced delay time or high speed of operation of the proposed comparator circuit. In addition to the above, proposed comparator circuit consume small power.**

Keywords: ***Current Comparator, High Speed, Power***

I. INTRODUCTION

With the need for high speed and/or low power consumption as CMOS VLSI devices are scaled down in size, current-mode operation have been considered as an alternative in analog circuit designs. Comparators are used in ADC/DAC and other front-end signal processing applications. In Earlier days Voltage Comparators are very common and most popular . However, the Voltage

Comparator having several difficulties including operational frequency, power consumption and input offset voltage. Current Comparison implemented by impressing the current pulse signal at the input of the comparator and finding whether it is Positive or Negative. The output Voltage generated by the comparator is used conveniently to indicate the result of operation.

First widely accepted Current Comparator proposed by H.Traff [1]. Circuit uses source follower input stage and a CMOS inverter as the positive feedback. In [2] offset free current comparator had demonstrated with an input current range up to 0.5uA. Drawbacks of this comparator are, it requires more number of MOS components and consumes more power. Later Buying-moo Min and So-won Kim [3] had come up with a new current comparator. It has the requirement of an extra current reference generator and a resistor. Speed of operation of the circuit is very less when

compared to our proposed new circuit. In 2000, the author had come up with a current amplifier cum comparator [4] has the response time of 50nS for 5uA input current, which indicates very much delayed response when compared to the response time of the recently published designs. A new current comparator proposed by [5], which comprises of one CMOS complementary amplifier, two resistive load-amplifiers and two CMOS inverters. Though the above circuit resolves the speed and power issue of [1],but it consumes more power and takes more response time than recently published approaches. Designs [6] [7] [8] have come up with high speed circuits , but when compared to proposed one those consume more power and slow in response. In 2010 author [9] had come up with a new approach, a low input impedance current comparator using pulse width modulation. Circuit [9] pre-occupied with more number of MOS and Capacitors than any of the designs. In this paper we are comparing the results obtained by the new proposed design with earlier published papers [1], [6] and[8].

In paper section-II & III, we analyze and simulate the behaviour of the conventional and the proposed current comparator circuits. In section-VI, all the results are compared and discussed.

II. ANALYSIS OF CONVENTIONAL CURRENTCOMPARATORS

A. Basic - Traff Current Comparator[1]

Tarff's comparator is one of the earlier proposed and widely accepted Current Comparator, which delivers moderately high speed of operation and low power consumption. Figure.1 shows the schematic diagram of the conventional positive feedback current comparator circuit [1]. One disadvantage of the novel approach concerns the input voltage to the positive feedback inverter. It does not slew from rail to rail, making neither M2 nor M3 totally shut off. To calculate the Speed and the Power Consumption, the raff's [1] current comparator is subjected to the Transient and the DC analysis. Simulations performed over the circuit from +/-1mA to +/- 100nA input current range and the responses are computed. Later in Section- IV along with the results of the current comparators [6] and [8], the simulation outcome of the Traff [1] will be compared with the newly proposed current comparator. Results confirm the better performance of the newly proposed current comparator.

B. Current Comparators [6] and [8]

Figure.2 shows the schematic diagram of the conventional current comparator circuit published in [6]. Positive feedback operates at the output nodes of the inverters

M2/M5 and M3/M4 respectively. In the prerecession state transistors M0 and M6 are closed and transistors M1 and M7 are open. As the voltage on the comparator node is affected by input current, so the inverter M5/M2 begins to switch. As this slews to either rail the transistors M0 or M6 are switched open, and then with a delay of about 10ns the transistors M1 or M7

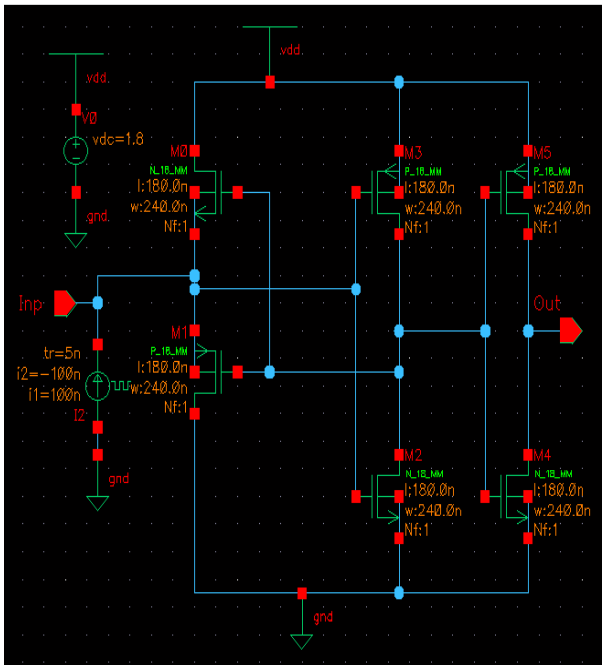

Figure 1: Traff's Current Comparator

respectively are switched closed. This latched feedback dumps enough charge on the comparator node to significantly speed the decision process, particularly at low current inputs. Main disadvantage of the system is that input node slews from rail to rail and this can slow the operation of the comparator.

Transient and DC analysis has been performed using Cadence Spectre simulator with UMC 180nm technology model files. Below Figure 3.shows the Transient response of the current comparator [6] when the input current is at +/- 10uA. In this manner the Current Comparator [6] is subjected to the Input current pulse ranges from 1mA to 100nA and the Transient analysis had been performed. Current comparator [6] performs the successful comparison till +/- 10uA and below this range output voltage starts distorted. Transient analysis can be used to confirm the operating range of the comparator.

Thereafter, DC analysis had been performed to calculatethe average power consumption of the given current comparator [6]. Below Figure 4 Shows the Power plot of the current comparator at +/-10uA.

Figure 5.shows the current comparator circuit published in [8]. When compared to the earlier implemented [6] circuit, in [8] author had added two more additional MOS transistors M8 and M9. These two MOS transistors speed up the decision process happening in the circuit. In the pre-decision

state transistors M0 and M6 are closed and transistors M1, M9 and M7, M8 are open. When compared to the speed of [6], the speed of operation of the comparator [8] is well increased

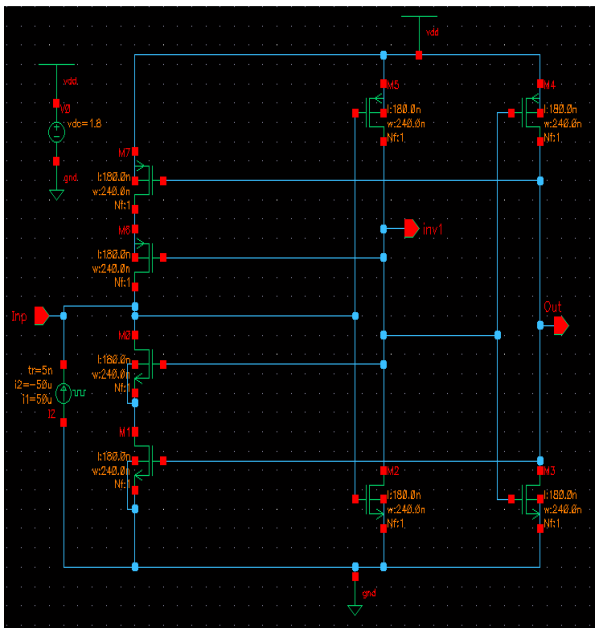

Figure 2: Conventional Current Comparator [6]

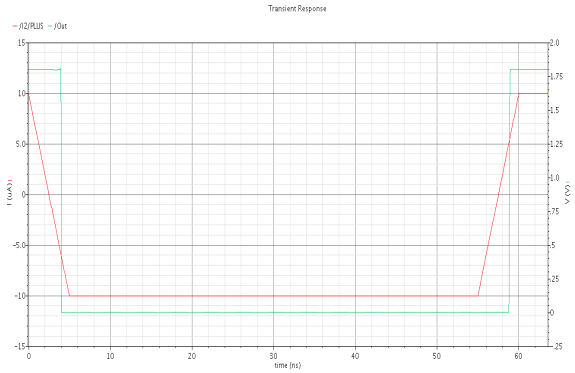

Figure 3: Transient Response of Conventional Current Comparator [6] at +/-10µA

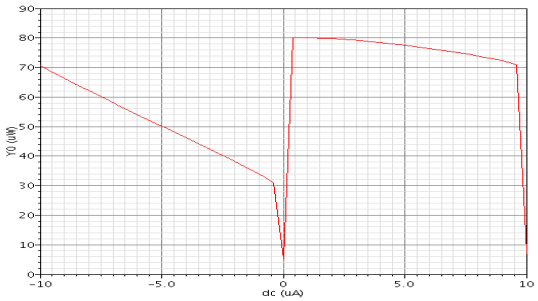

Figure 4:Power Plot of Current Comparator [6] at +/-10µA

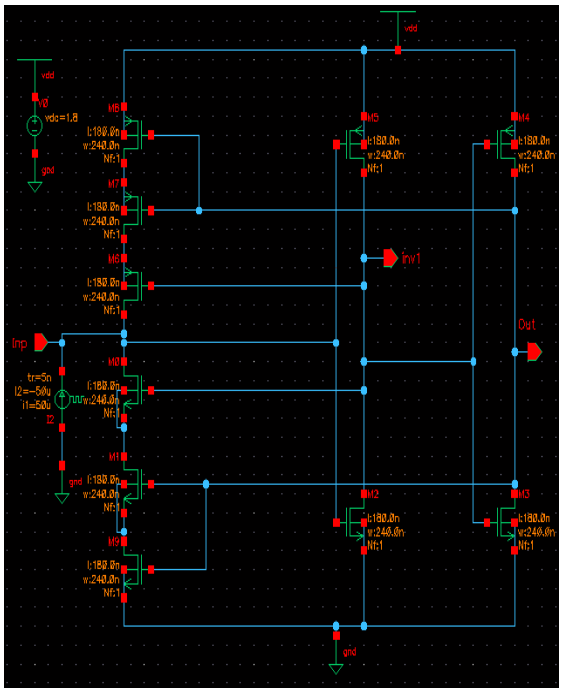

Figure 5: Conventional Current Comparator [8]

Below Figure 6.shows the Transient response of the current comparator [8], when the input current pulse is at +/-10uA. This way the Current Comparator [8] is subjected to the Input current pulse ranges from 1mA to 100nA and the Transient analysis had been performed. Current comparator well performs the Comparison operation till +/-10uA and below this range onwards output starts distorted. From Figure 6, the calculated 50%propagation delay of the circuit is 1.493nS. DC analysis had been performed to compute the total power consumption of the comparator [8]. Below Figure 7., shows the power consumption of the Comparator [8] when the input current is kept at +/-10uA . At 10uA, the computed average power consumption of this comparator is 32.6uW.

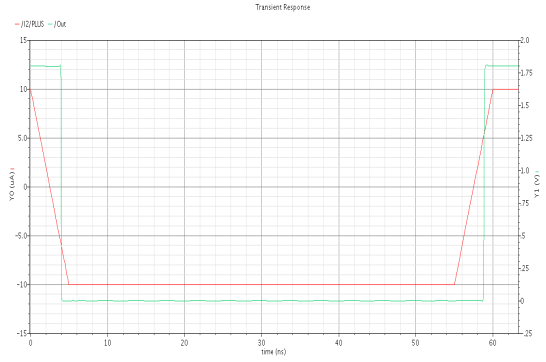

Figure 6:Transient Response of Conventional Current Comparator [8] at +/-10µA

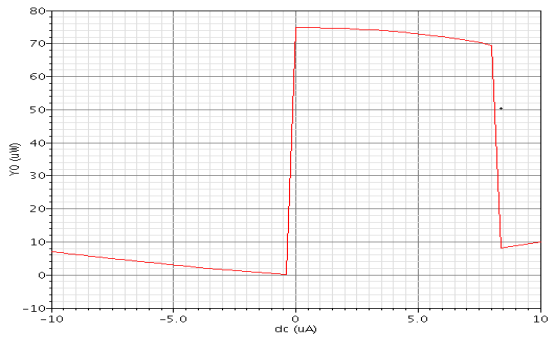

Figure 7:Power Plot of Current Comparator [8] at +/-10µA

III. ANALYSIS OF PROPOSED CURRENT COMPARATOR

Below Figure 8.shows the schematic of the proposed current comparator. The circuit consists of 5-parts, such as Wilson Current Mirror, Standard Current Mirror, CMOS Inverter, Power supply and Input current pulse generator. Wilson current Mirror used to reduce the total power consumption of the circuit. Comparator uses the high output impedance of the Wilson current mirror to amplify small differences in input currents to large variations in output voltage.

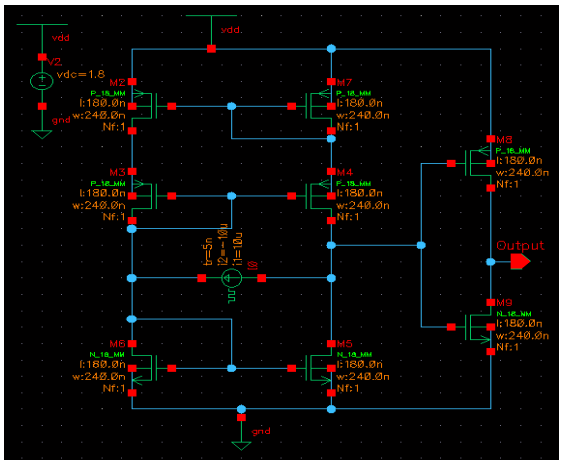

Figure 8: Proposed Current Comparator

Below Figure 9.shows the Transient response of the newly proposed current comparator for the variation of input current pulse from -10uA to +10uA. Throughout the Transient analysis the Input current pulse has been varied from 1mA to 400nA and the characteristics curves were plotted. Current comparator does successful comparison till 400nA and below this value the output starts distorted. Earlier published [6], [8] works till 10uA and this proposed circuit works till 400nA. So when compared to [6] and [8], the input range is increased. Our circuit achieves 50% propagation delay of 575 Picoseconds.

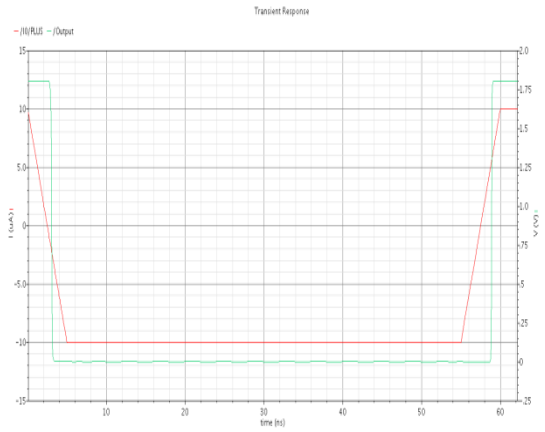

Figure 9:.Transient Response of the Proposed Current Comparator at +/- 10uA.

DC analysis has been performed to compute the total power consumed by the proposed comparator. Below Figure 10., shows the power consumed by the comparator when the input current is at 10uA. Average power consumed by this proposed comparator at 10uA is 8.6uW.

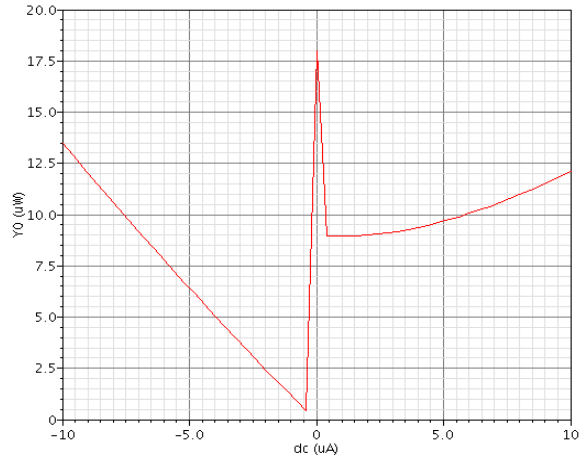

Figure 10:.Power Plot of the Proposed Current Comparator at +/-10uA.

IV. COMPARISON OF CURRENT COMPARATORS

Simulated Characteristics and parameters of the both conventional and proposed current comparator are compared and the observations are explained in detail. From TABLE I we observes as when compared to the earlier proposed current comparators [6] and [8] the proposed new Current Comparator operates at Very High Speed. Also the proposed Current Comparator operates well up to the input current of 400nA, though the comparators [6] and [8] functions only up to 10uA.

Also from TABLE II, observed that from 10uA onwards the power consumption of the proposed new Current Comparator is Very Low when compared to the power consumed by either of the current Comparators [6] and [8]. At 1mA the proposed comparator consumes little extra power than [6] and [8]. On the other hand, the Power consumption has been improved a lot when the circuit is subjected with the input current below 100uA. From 100uA onwards, the proposed current comparator consumes Very less power than [8].

TABLE I. COMPARISON BETWEEN THE CURRENT COMPARATORS – 50% PROPAGATION DELAY

Input Current (mA)	**Propagation Delay (in Nano Seconds)**		
	Proposed New Current Comparator	***Current Comparator [14]***	***Current Comparator [16]***
1	0.100	0.219	0.229
0.1	0.235	0.561	0.577
0.01	0.575	1.964	1.493
0.001	1.544	Not Working	Not Working
0.0004	2.391	Not Working	Not Working

Below Figure 11.shows the Delay Time versus Input current graph. It clearly describes that the proposed current comparator achieves better performance than its counter parts [6] and [8].

TABLE II.COMPARISON BETWEEN THE CURRENT COMPARATORS – POWER DISSIPATION

Input Current (mA)	**Power Dissipation (in µWatts)**		
	Proposed New Current Comparator	***Current Comparator[14]***	***Current Comparator[16]***
1	1380	763	1150
0.1	81	52.7	81.8
0.01	8.6	61.4	32.6
0.001	5.28	Not Working	Not Working

Input Current (mA)	Power Dissipation (in µWatts)		
	Proposed New Current Comparator	***Current Comparator[14]***	***Current Comparator[16]***
0.0004	21.1	Not Working	Not Working

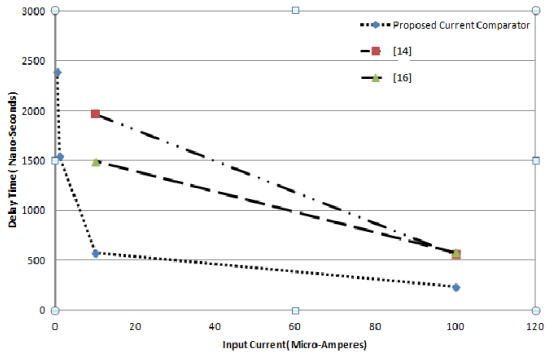

Figure 11: Delay Time versus Input Current.

Figure 12.shows the Power Dissipation versus Input current graph. For Large current inputs say 1mA, the proposed circuit dissipates little extra power. But from 100uA onwards newly proposed comparator dissipates lower power than earlier published paper [8], and from 61uA onwards it dissipates lower power than both [6] and [8]. As shown in TABLE II below 100uA, circuit power dissipation is far better than its counterparts.

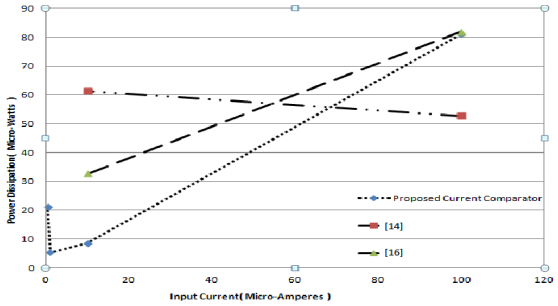

Figure 12: Power Dissipation versus Input Current..

V. CONCLUSION

Main intention of this paper is to present a simple idea of designing a new CMOS Current Comparator topology for high speed applications such as Data converters and Digital switching circuits. From Figure 11 and Figure 12, when compared with the performance of the existing current comparators [6] and [8], the proposed current comparator operates at very high speed. In addition to the above advantage, from +/-10uA onwards the proposed new current comparator consumes very low Power when compared to the current comparators published in [6] and [8].

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