Design of a CMOS Op-Amp and Second Order Sigma Delta Analog to Digital Converter Using 0.18 μm CMOS Technology

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Abstract: **This paper presents the design of a CMOS OP-AMP and second order single bit Sigma-Delta Analog-to-Digital Converter (ADC) which is realized using CMOS technology. In this paper, of a CMOS OP-AMP and Second order Sigma-Delta ADC is designed which accepts an input signal of frequency 2 KHz, an OSR of 153, and 240 KHz sampling frequency .It is implemented in a standard 0.18um CMOS technology. The ADC operates at 0.7 V reference voltage. The Design and Simulation of the Modulator is done using Microwave offive sofware(9.1).This paper Sigma Delta Modulator. Op-amp which is a key componentused in the design, has the open loop voltage gain of 65db, Phase Margin of 44.5 Degree, output resistance of 130.5KΩ, and power dissipation of 0.096 mW. A CMOS OP-AMP and second order single bit Sigma Delta ADC is implemented using ±3.0 power supply and simulation results are plotted using Microwave offive sofware(9.1).After the modulator is designed, the output pulse train of the modulator is transferred from Microwave offive sofware(9.1) to MatlabWorkspace[9].**

Keywords: **Analog Circuit,2 stage CMOS Operational amplifie, High Frequency.**

I. INTRODUCTION

With developments in deep sub micrometer CMOS processes, the available dynamic range in Operational Amplifiers (Op-Amps) is reduced due to lower power supply voltages [1].The design of analog circuits such as operational amplifiers (Op-Amps) in CMOS technology becomes more critical. Many authors have noted the disproportionately large design time devoted to the analog circuitry in mixed mode integrated circuits. In this paper we introduce a new method for determining the component values and transistor dimensions for CMOS Op-Amps. The method handles a very wide variety of specifications and constraints, is extremely fast, and results in globally optimal designs[11].In this paper, we present a systematic design methodology for split-length compensated low-voltage three-stage Op-Amps. The aim of the design methodology in this paper is to propose straightforward yet accurate equations for the design of high-gain 2 staged CMOS op-amp. To do this, a simple open-loop analysis with some meaningful parameters (phase margin, gain-bandwidth, etc.) is performed. A sigma–delta modulator is one method for providing the front end to an analog to digital converter. When an analog signal is digitized, quantization error is introduced into the frequency spectrum. The sigma–delta's function is to push the quantization error that is near the signal into a higher frequency band near the sampling frequency. After this is done the signal can be low pass filtered and the original signal can be restored in a digitized form .The sigma–delta modulator with first order and second order noise shaping characteristics is designed The block diagram second order loop is shown in Figure 1.In the sigma–delta modulator, the difference between the analog input signal and the output of the DAC is the output of the Summer. This difference is given as an input to the Integrator.The integrator integrates over each clock period.The clock is at a much higher frequency than the input sinusoid,causing the sine wave to be approximately flat over the clock period.

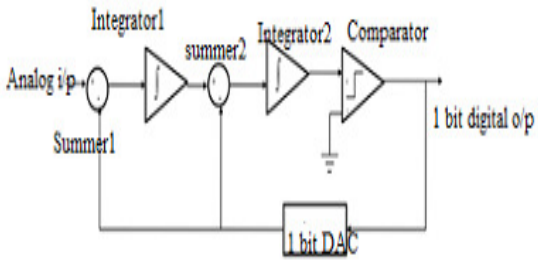

Fig 1: Block diagram of 2nd order sigma-delta modulator

II. CMOS TECHNOLOGY

In CMOS (Complementary Metal-Oxide Semiconductor) technology, both N-type and P-type transistors are used to realize logic functions. Today, CMOS technology is the dominant semiconductor technology for microprocessors, memories and application specific integrated circuits (ASICs). The main advantage of CMOS over NMOS and bipolar technology is the much smaller power dissipation. Unlike NMOS or bipolar circuits[4], a CMOS circuit has almost no static power dissipation. Power is only dissipated in case the circuit actually switches. This allows to integrate many more CMOS gates on an IC than in NMOS or bipolar technology, resulting in much better performance. An n-type MOS (NMOS) and a p-type MOS (PMOS) device are fabricated on the same p-doped wafer, with the PMOS device embedded in an n-doped well.

III. SECOND STAGE OP-AMP AND ITS EXPERIMENTAL RESULT

The operational amplifier that the integrator uses must have high gain to effectively carry out a smooth integration, as well as a large enough bandwidth to support the high frequency square waves that it will be integrating[6]. The amplifier used is shown in Figure 2.

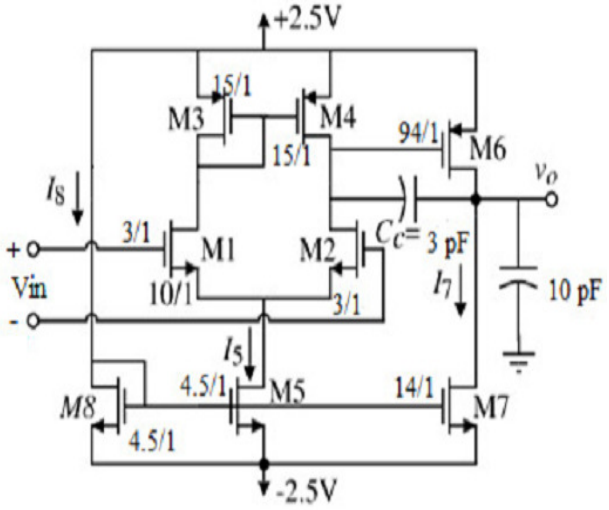

Fig 2: Design Of Two Stage Op-amp

IV. RESULT OF OP-AMP

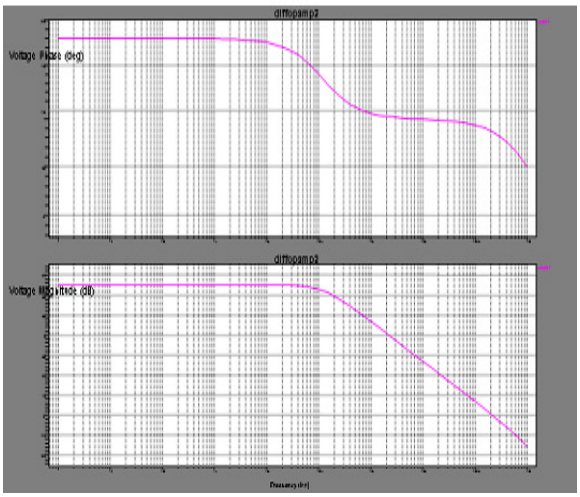

Figure 3. Gain and phase of a op-amp

Parameter	Two stage op amp
Gain (dB)	65
-3 dB frequency (MHz)	19.8
Phase Margin (°)	44.5
Unity gain frequency (GHz)	65
Power (mW)	0.096

Table 1:Parameters of Second Stage Op-Amp

V. SECOND ORDER SIGMA DELTA ADC CONVERTER AND ITS EXPERIMENTAL RESULT

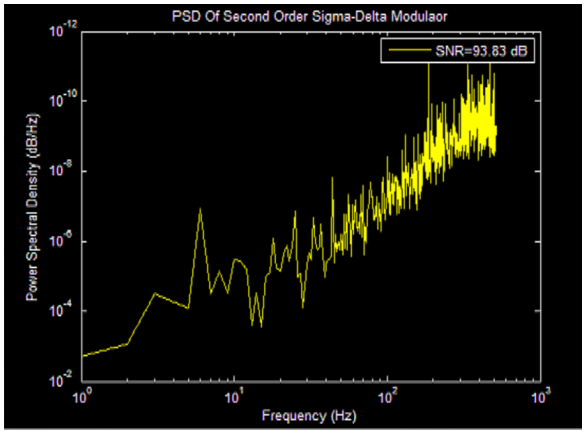

Fig 4: PSD of 2nd order Modulator

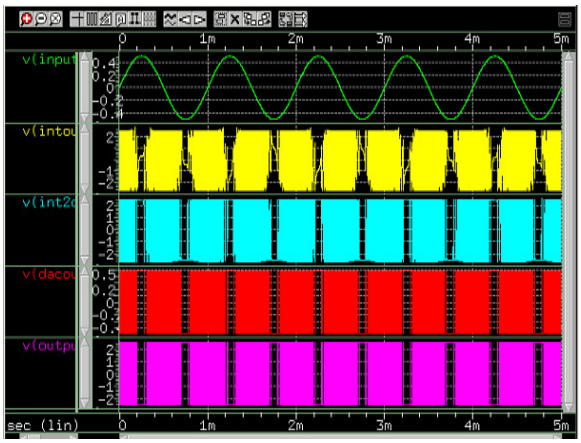

Fig 5: Step by Step Performance of Second Order Modulator

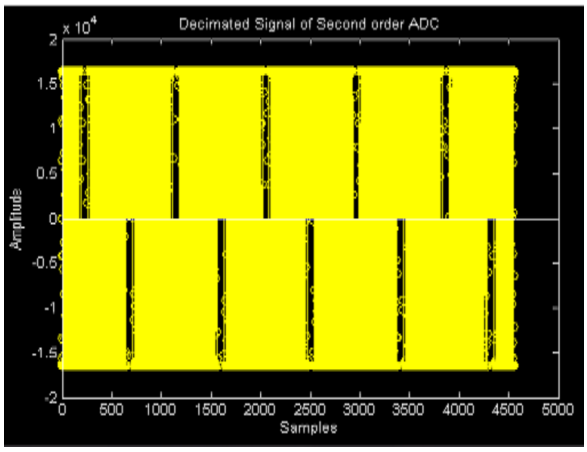

Fig 6: Decimated Output of Second Order Modulator.

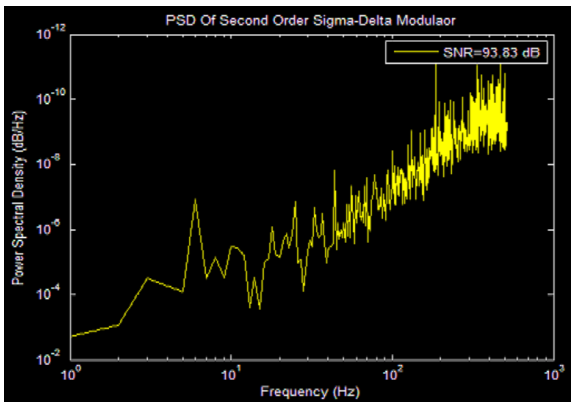

Fig 7: PSD of 2nd order Modulator

VI. CONCLUSION

This project primarily aims to demonstrate the design of a OP-AMP and second order sigma-delta ADC to adapt to multiple communications standards. The simulated parameter for of a OP-AMP and second Order Modulators using an integrator of capacitance 1nF and a Comparator with a propagation delay of 5 ns care shown below.

Parameter	Second Order Modulator
SNR	90.13 dB
ENOB	15its
DR	135 dB

Table 2: Simulated Parametric Value

VII. FUTURE WORK

We can also change in NMOS design TSMC based on 0.18 CMOS Technology .The area which will be of interests optimizing the power distribution among the various blocks like continuous-time analog filter preceding the ADC, the ADC, and the digital filter following the ADC should be explored. We can also works on NMOS Transistor for increase gain and phase margin. We can also work on three stage of OP-AMP.

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