COMPARATIVE DESIGNING OF POWER EFFICIENT AND HIGH-SPEED DOMINO LOGIC

Sanjay Patware [1], Suresh Gawande [2]
[1]PG Student [VLSI], Dept. of ECE, Bhabha College of Engineering, RGPV Bhopal, M.P. India
Email: [1]sanjay.patware1990@gmail.com, [2] suresh.gawande@rediffmail.com

Abstract— **The microprocessors in the modern era are propelled by high speed, small area and low power circuits. Dynamic logic circuits are used for high performance and high speed applications. Wide OR gates are used in Dynamic RAMs, Static RAMs, high speed processors and other high speed circuits. In spite of their high performance, dynamic logic circuit has high noise and extensive leakage which has caused problems for the circuits. To overcome these problems Domino logic circuits are used which reduce sub threshold leakage current in standby mode and improve noise immunity for wide OR gates. High noise sensitivity is the result of sub threshold leakage current that flows through the evaluation network. With the advancements in CMOS manufacturing process to scale down into the ultra deep sub-micron regime, the leakage current becomes an increasingly. The conventional footed standard domino logic is modified to add a new circuit to improve leakage tolerance, especially in the initial phase of evaluation. The conditions for our simulations are: CMOS 90nm and 65nm technology, 1V and 0.9V power supply and bottleneck operating temperature of 27^0C.**
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Keywords— ***Domino Circuit, Low Power, High Speed, CMOS.***

I. INTRODUCTION

Wide OR gates are used in Dynamic RAMs, Static RAMs, high speed processors and other high speed circuits. Implementation of wide OR gate using static CMOS circuit requires large number of transistor and leakage power dissipation is also considerable [1]. While in comparison to static CMOS circuits, dynamic CMOS circuits have a large number of advantages such as lower number of transistors, low-power, higher speeds, short-circuit power free and glitch-free operation. Dynamic CMOS circuit technique [2] allows us to significantly reduce the number of transistors used to implement any logic function. In spite of their high performance, dynamic logic circuit has high noise [3] and extensive leakage which has caused problems for the circuits. The main limitations of dynamic logic are cascading and charge sharing. To overcome these problem domino circuits are use. In addition to dynamic logic an inverter and a weak pMOS pull-Up keeper transistor (with a small (W/L) ratio) is added to the dynamic CMOS output stage in domino logic. Inverter is use to avoid cascading problem and to avoid charge sharing problem weak keeper is used, which essentially forces high output level unless there is a strong pull-down path between the output and the ground.

High fan-in [4] domino circuits are used to design high performance register files, ALU front ends, and priority encoders in content addressable memories. Wide domino logic refers to domino logic gates with N parallel pull down branches when N is greater than 4; that are used to design circuits in microprocessor critical path. By scaling down the technology the sensitivity of the dynamic node to the noise sources has emerged as a serious design challenge. For improving noise immunity and reducing leakage the keeper transistor is added. However, power dissipation increases and performance degrades by adding this pMOS keeper transistor. Upsizing the keeper transistor improves robustness at a cost of higher power dissipation and delay. The severity increases many fold in wide Domino circuits because of higher number of parallel pull-down branches [38]. Therefore small size keeper is desired for high-speed applications while to increase the robustness, larger keeper is required. The keeper ratio *K* is defined as

$$K = \frac{\mu p \left(\frac{W}{L}\right) keeper\ transistor}{\mu n \left(\frac{W}{L}\right) evaluation\ transisitor}$$

where *W* and *L* denote the transistor size, and μn and μp are the electron and hole mobility, respectively. However, the traditional keeper approach is less effective in new generations of CMOS technology. Although keeper upsizing improves noise immunity, it increases current contention between the keeper transistor and the evaluation network. Thus, trade off exist between delay and power to improve noise and leakage immunity.

II. Literature Review

Varies circuit design for low leakage and noise immune wide fan-in domino circuits is presented. The varies technique uses the difference and the comparison between the leakage current of the OFF transistors and the switching current of the ON transistors of the pull down network to control the PMOS keeper transistor, yielding reduction of the contention between keeper transistor and the pull down network. Moreover using the stacking effect, leakage current is reduced and the performance of the current mirror is improved.

Gaetano Palumbo, Melita Pennisi, and Massimo Alioto [1] titled **"A simple circuit approach to reduce Delay variation in Domino logic gates "** presents a new circuit approach in the conventional circuit which makes a new circuit having less delay variability as compare to the conventional circuit. It

acquires a different circuit having two keeper transistors. The main highlight of this paper is reduce the delay variability by reducing the loop gain associated with the feedback.

Massimo Alioto, Gaetano Palumbo and Melita Pennisi [2] titled **"Understanding the effect of Process variation on the Delay of Static and Domino logic"** describes about two different process variation namely interdie and intradie process variation and it's influence on circuit. The paper analysis also shows a view of delay dependency on fan-in, fan-out and sizing. Finally it shows that delay variation is mainly caused due to variation in current delivered by logic gates and impact of variation of parasitic capacitance is negligible in the entire process.

Ali Peiravi and M. Asyaei [3] titled **"Robust low leakage controlled keeper by current comparision Domino for wide fan-in gates"** presents various domino logic circuits. This paper proposes a new Controlled keeper by current comparison domino (CKCCD) which is a leakage and noise tolerant domino logic circuit. The main idea in this technique is that the keeper is controlled to decrease contention and yield a high performance using current comparison between the leakage current due to the low level inputs and the current due to at least one input at high level.

A.Kabbani and A.J. Al-khalili [4] titled **"A Technique for Dynamic CMOS Noise immunity evaluation"** analyses noise immunity of dynamic CMOS logic circuit. It shows how amplitude and width of noise pulse play an important role to determine response of a dynamic logic circuit. In this paper for determination of noise in dynamic logic circuit a mathematical model is presented. The analysis of noise discussed here is done for both long-channel and short-channel of the MOSFET.

2.1 Concept of Domino Logic

Dynamic logic is over twice as fast as normal logic; it uses only fast N transistors. Static logic is slower because it uses slow p-type transistors to compute logic. Dynamic logic is harder to work, but if we need the speed there is no other choice. Dynamic logic requires two phases, the first phase is set up phase or pre-charge phase, in this phase the output is unconditionally go to high (no matter the values of the inputs).The capacitor which represents the load capacitance of this gate becomes charged. During the evaluation phase, CLK is high. Popular implementation of dynamic logic is domino logic.

The domino CMOS circuit shown has two modes of operation as shown in the Fig. 2.1.

1) Pre-charge phase**, 2)** Evaluation phase.

Pre-charge phase

This happens when clock signal is low. Thus the NMOS pull-down network is turned off [6-7]. The clock controlled PMOS transistor is turned on. So the output node is charged to V_{dd}. Hence this is called pre-charge phase or setup phase.

Evaluation phase

This happens after the pre-charge phase and when the clock signal is high [5]. The output node is either pull down or pull up depending on the inputs to the NMOS transistors. This defines the operation of the dynamic CMOS circuit.

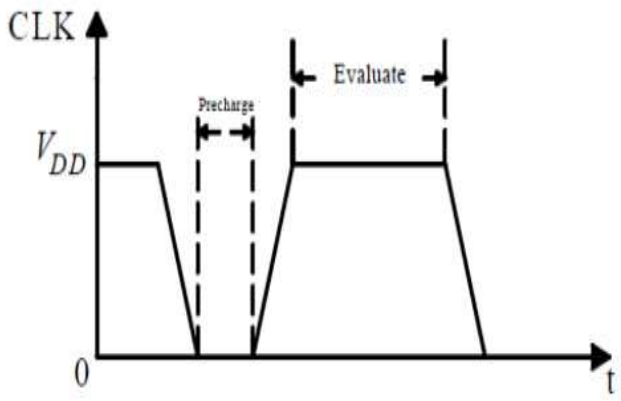

Fig. 1: Waveform Of The Clock Needed To Operate Domino Logic Circuit [6].

Domino logic is the most popular dynamic logic. It runs 1.5-2 times faster than static CMOS logic because, dynamic gates present much lower input capacitance for the same output current and a lower switching threshold. Domino circuits are in function very similar to the clocked CMOS circuit. In Domino logic a single clock is used to pre-charge and evaluate a cascaded set of dynamic logic blocks. During the pre-charge phase (CK=0) all output nodes all (N) of the dynamic gates are pre-charged to high, as shown in Fig.1. through the PMOS transistor, and thus the outputs of the corresponding buffers are pre-charged to low. Since all transistors of subsequent dynamic gates are fed from such buffers, these will be turned off during the pre-charge phase [8-9].

The necessity for low-power design is also important in high performance digital systems, such as microprocessors and digital signal processors because of high integration density and the high clock frequency. The magnitude of power per unit area is increasing with high density and the problem of heat removal and cooling is worsening. As a result, today it is widely accepted that power efficiency is a design goal at par in importance with miniaturization and performance. Minimizing power consumption calls for conscious effort at each abstraction level and at each phase of the design process.

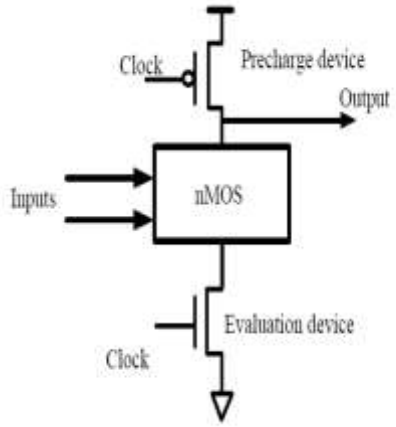

Fig. 2: Basic Structure of Domino Logic

Next during the evaluation phase, dynamic node are either discharged through transistor NMOS or they remain high, according to the realized function. Thus the outputs of the buffers either go to high or remain low, respectively [10-11]. It should be noted that in Domino logic the Output Node is always from low to high and it is rippled through the logic from the primary inputs to the primary outputs. Since there are cascaded logic blocks, the evaluation of a stage causes the next stage to evaluate and so on. Obviously, any number of logic stages may be cascaded, provided that they can be evaluated within the evaluate phase of the clock. Domino logic design is used for better performance with a smaller number of transistors. In a novel Domino logic design pre-charged by clock and data has been proposed that also presents high performance and reduced area requirements.

32.2 Noise (leakage) immunity metric

For robustness measurement, identical noise pulses are applied to all inputs in the evaluation phase, and the amplitude of the noise at the output of the static inverter. In this measurement, the duration of the input noise pulse is kept constant at 50 ps (typical gate delay at 65-nm technology) and the amplitude of the output noise is observed for different amplitudes of the input noise [12]. The metric we use for leakage and noise robustness comparison is the unity noise gain (UNG), defined as the amplitude of the input noise that causes the same amplitude of noise at the output.

$$UNG = \{ V_{noise}; V_{noise} = V_{out} \}$$

We use a pulse noise to simulate cross-talk type of noise at the input. The effective noise depends on both the amplitude and duration of the noise pulse [13]. The input noise level can be increased by increasing either the noise pulse duration or amplitude. In our experiments, we change the input noise level by changing its amplitude.

2.3 Power Dissipation in CMOS Digital Circuit

Power dissipation in CMOS digital circuits is categorized into two type peak power and time-averaged power consumption. Peak power is a reliability issue that determines both the chip lifetime and performance. The voltage drop caused by the excessive instantaneous current flowing through the resistive power network effect the performance of a design due to the increased gate and interconnects delay. [9].

The time-averaged power consumption in conventional CMOS digital circuits occurs in two forms dynamic and static. Dynamic power dissipation occurs in the logic gates that are in the process of switching from one state to another. During this process, any internal and external capacitance associated with the gate's transistors has to be charged, thereby consuming power. Static power dissipation is associated with inactive logic gates (i.e., not currently switching from one state to another). Dynamic power is important during normal operation, especially at high operating frequencies, whereas static power is more important during standby, especially for battery-powered devices.

2.3.1 Dynamic Power Dissipation

For a fraction of an instant during the operation of a circuit, both the PMOS and NMOS devices are "on" simultaneously. The duration of the interval depends on the input and output transition (rise and fall) times. During this time, a path exists between V_{dd} and gnd and a short circuit current flow. However, this is not the dominant factor in dynamic power dissipation. The major component of dynamic power dissipation arises from transient switching behaviour of the nodes. The signal in the CMOS devices transition back and forth between the two logic levels result in the charging and discharging of parasitic capacitances in the circuit. Dynamic power dissipation is proportional to the square of the supply voltage. In deep sub-micron processes, supply voltages and threshold voltages for MOS transistors are greatly reduced. This to an extent reduces the dynamic power dissipation.

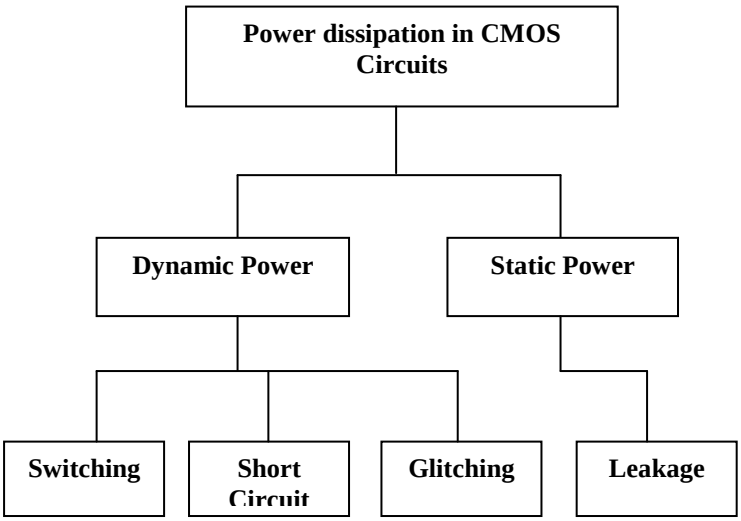

Fig.3: Block Diagram of Power Dissipation in CMOS Circuit

2.4. Conventional– Keeper Domino Logic

Due to their high speed and low device count especially compared to complementary CMOS, dynamic logic circuits are used in a wide variety of applications including microprocessors, digital signal processors, and dynamic memory As shown in the Fig.4, At first, consider the footless standard domino logic (FLSDL). In standard domino logic gates, a feedback keeper transistor is employed to maintain the state of the dynamic node against coupling noise, charge sharing, and sub-threshold leakage current [14-15]. The keeper transistor is fully turned on at the beginning of evaluation phase, then the keeper transistor and evaluation network compete to determine the logical state of the dynamic node. This contention between the keeper transistor and the pull down network degrade the circuit speed and power characteristics.

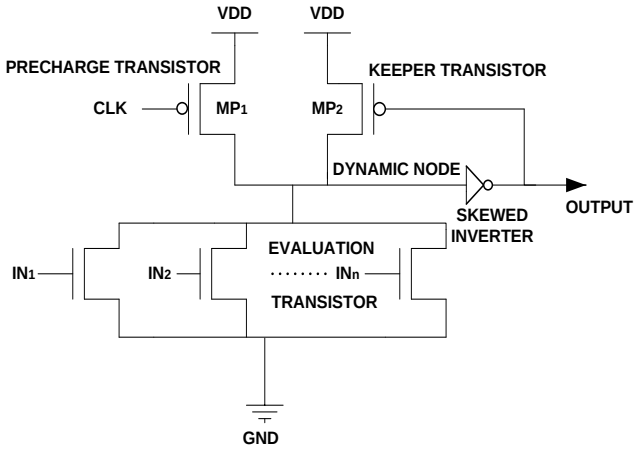

Fig. 4: Footless Standard Domino Logic (FLSDL) [10]

The footless standard domino circuit works as follows: when clock is low, the circuit is in pre-charge mode. The dynamic node starts to go high through MP_1 and MP_2. The output node goes low, and then the MP_2 device is turned on. Therefore, it causes faster charging in dynamic node. When clock is high, MP_1 is off; hence the circuit has two states, standby mode and active mode. The standby mode is when all inputs to evaluation network devices are low. In fact, in this mode all input signals applied to pull down network are at zero, so the dynamic node remains high, but due to sub-threshold leakage current, the dynamic node encounters some discharging. [11,16].

The second standard technique is footed standard domino logic (FSDL) as shown in the Fig. 2.5. This circuit's treatment is look like the footless domino logic style. However because of the stacking effect in FSDL, the speed of logic is lower than footless one, but the noise immunity is higher. When clock is low, the dynamic node is pre-charged to V_{DD}. In this phase the footed transistor is turned off. When clock goes high, footer transistor is tumed on. So, depending to incoming data to pull-down network the state of circuit is standby or active [10]. One of the disadvantages of this kind of domino circuit is that it should be constructed with only true-logic gates. Moreover, simultaneous pre-charge may causes an unacceptable IR-drop noise [12].

So, in order to compensate for the leakage current, the weak PMOS keeper must be replaced by a stronger one, that is a PMOS keeper with larger W/L ratio. However, if only one of the inputs is activated during the evaluation phase, then the corresponding NMOS transistor will act to discharge the pre-charge node fighting the relatively large current provided by the strong PMOS keeper.

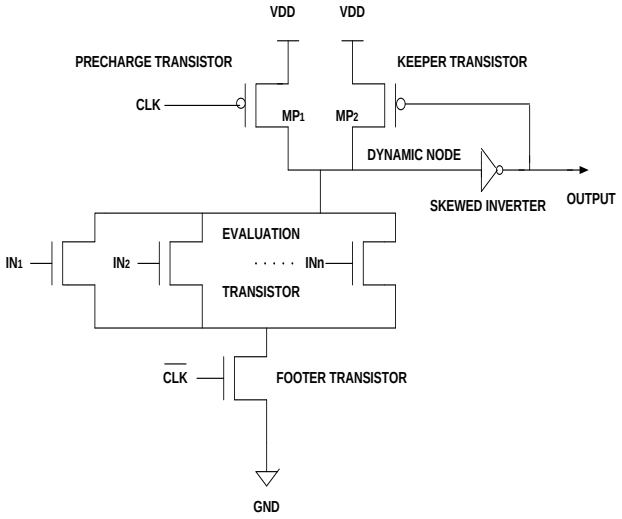

Fig.5: Footed Standard Domino Logic (FSDL) [10]

This leads to one of the two following cases depending on the value of the strong keeper current; if the current of the NMOS transistor in the PDN is larger than that of the strong keeper, then the dynamic node will discharge very slowly resulting in very low speed for the circuit.

On the other hand, if the current of the NMOS transistor in the PDN is smaller than that of the strong keeper, then the dynamic node will not discharge at all in this case resulting in an erroneous output for the circuit and excessive power consumption.

2.4.2 High-speed domino

The architecture of an 8-input HS-Domino OR gate is shown in Fig.8. It is similar to CD-Domino except that the gate O/P is connected to the keeper through an NMOS (MN_1) and a PMOS (MP_3) device, whose gates are connected to the delayed clock signal.

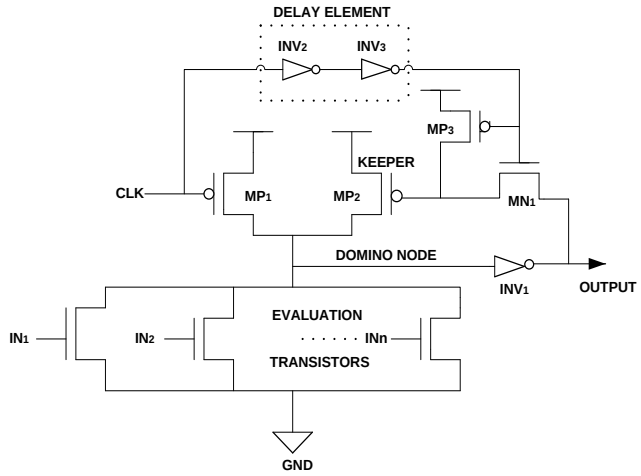

Fig.6: An 8-input HS-Domino OR gate [13]

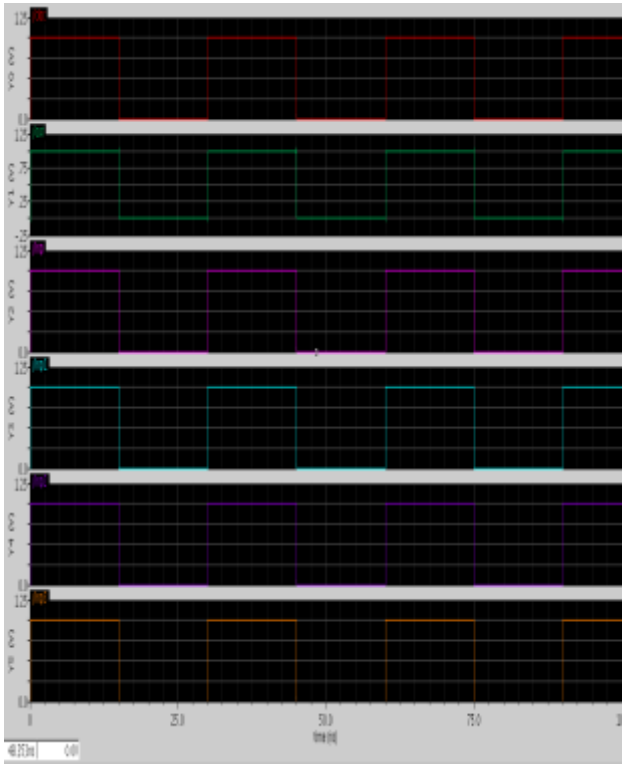

Fig.7: Output waveforms of HS domino circuit

HS-Domino operates as follows: when the clock is LOW during pre-charge, the Domino node is pre-charged to V_{dd}. Transistor MN_1 is OFF, MP_3 is ON charging the gate of the keeper transistor MP_2 to V_{dd}, thus turning MP_2 OFF. MP_2 is therefore OFF at the beginning of evaluation phase [12,17]. Contention is thus eliminated between the keeper and the pull-down devices during evaluation. Therefore, the Domino gate evaluates faster and no contention current exists.

Need of Domino Logic

Avoid duplication of logic twice as both NMOS and PMOS, as in standard CMOS. Typically, it can be used in very high performance applications like small sequential memory circuits, amenable to synchronous logic, High density achievable and also consume less power.

IV. Problem Formulation

High fan-in compact dynamic gates are often used in high performance critical units of microprocessors. However, the use of wide dynamic gates is strongly affected by subthreshold leakage and noise sources. This is mainly due to decreased threshold voltage that results in exponentially increased leakage currents in scaled technologies. To reduce power consumption, supply voltage scaling is used across technology scaling. However, threshold voltage needs to be scaled down as well to maintain transistor overdrive for large ON currents. Less threshold voltage means smaller gate switching trip point in domino circuits.

. Dynamic logic circuit has several advantages over the static logic circuit. These are :-

i) Dynamic logic circuit requires less number of transistors as compare to the static logic circuit. Generally dynamic logic circuit requires (n+2) transistors for a particular function and for the same function static logic circuit requires 2n transistors.

ii) The number of transistor are less, therefore the speed of operation is faster as compare to the static logic circuit.

iii) Dynamic logic does not participate in short circuit power dissipation and glitching power dissipation.

iv) Dynamic logic circuit is having smaller static power dissipation as compare to static logic circuit.

v) The load capacitance in dynamic logic circuit is less than the static CMOS logic circuit.

Apart from these advantages the dynamic logic circuit is having some limitations which

affect the performance of dynamic logic circuit. Some of these are:-

a) Charge leakage problem

b) Charge sharing problem

c) Clock skew problem

III. PRAPOSED METODALOGY

The tremendous success of the low-power designs of VLSI circuits over the past 50 years has made significant changes in

our electronic market. Currently Dynamic logic such as domino logic is widely used in many applications to achieve high performance, which cannot be achieved with static logic styles. However, the main drawback of dynamic logic families is that they are more sensitive to noise than static logic families. On the other hand, as the technology scales down, the supply voltage is reduced for low power, and the threshold voltage (V_{th}) is also scaled down to achieve high performance. Since reducing the threshold voltage exponentially increases the sub-threshold leakage current, reduction of leakage current and improving noise immunity are major concern in robust and high-performance designs in recent technology generations, especially for wide fan-in dynamic gate. However, in wide fan-in dynamic gates, especially for wide fan-in OR gates, robustness and performance is significantly degraded with increased leakage current. As a result, it is difficult to obtain satisfactory robustness–performance Tradeoffs.

TABLE .1: COMPARISION OF POWER DESSIPATION (in μW)

S. No.	LOGIC STYLE	8 INPUT		16 INPUT		32 INPUT	
		65nm	90nm	65nm	90nm	65nm	90nm
1.	SFLD	7.200	18.84	9.586	14.01	12.33	16.29
2.	FLD	8.227	13.44	14.00	22.97	17.04	23.83
3.	HSD	494.1	835.5	495.6	4220	5633	5762
4.	CKD	264.5	496.6	266.8	499.4	298.3	301.2
5.	WFD	8.908	13.69	14.30	14.30	19.38	27.91
6.	LCR	6.039	9.015	8.210	11.85	12.39	15.27
7.	CCD	6.125	11.75	14.86	16.93	19.34	26.20

TABLE.2: COMPARISION OF Delay (in pS)

S. No.	LOGIC STYLE	8 INPUT		16 INPUT		32 INPUT	
		65nm	90nm	65nm	90nm	65nm	90nm
1.	SFLD	8.243	8.644	11.58	12.92	16.29	17.28
2.	FLD	13.53	24.96	32.02	38.37	39.20	42.29
3.	HSD	5.882	6.699	12.50	13.83	17.33	19.38
4.	CKD	14.48	16.26	22.20	25.02	21.28	25.39
5.	WFD	21.15	22.39	29.92	31.36	38.46	45.39
6.	LCR	13.08	16.29	21.83	26.34	28.25	32.34
7.	CCD	14.61	18.27	25.01	28.33	30.62	38.48

VI. Conclusion

The leakage current of the evaluation network of dynamic gates was dramatically increased with technology scaling, especially in wide domino gates, yielding reduced noise immunity and increased power consumption. Thus, new designs were necessary to obtain desired noise robustness in very wide fan-in circuits. Moreover, increasing the fan-in not only reduced the worst case delay, it also increased the contention between the keeper transistor and the evaluation network. Further work will focus on high speed and leakage-tolerant domino logic implementations. In particular, we plan to design a new domino logic in which the keeper transistor is design in such a way that improves the speed of the domino logic. Furthermore, we plan to explore the trade-off between the speed and noise immunity by moderating its complexity and by using.

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