FPGA Implementation of Digital IF Filter with Low Complexity and Less Delay using Multi-rate Approach

Ankesh Singh[1], Prof. Suresh. S. Gawande[2], Prof. Sher Singh[3]

M. Tech. Scholar, Department of Electronics and Communication, Bhabha Engineering Research Institute, Bhopal[1]

Guide, Department of Electronics and Communication, Bhabha Engineering Research Institute, Bhopal[2]

Co-guide, Department of Electronics and Communication, Bhabha Engineering Research Institute, Bhopal[3]

Abstract

Because of restricted recurrence assets, new administrations are being applied to the current frequencies, and specialist co-ops are apportioning a portion of the current frequencies for recently improved versatile interchanges. In light of this recurrence condition, repeater and base station frameworks for portable correspondences are getting more confused, and recurrence obstruction brought about by numerous groups and administrations is deteriorating. In this manner, a heterodyne recipient utilizing IF channels with high selectivity has been utilized to limit the obstruction between frequencies. Notwithstanding, repeater and base station frameworks in portable interchanges utilizing fixed IF channels can't effectively adapt to the use of different recurrence groups, the use of different administrations, and recurrence reusing. In this paper design digital IF filter using multi-rate approach. Multi-rate approach is reduced the hardware complexity is reduce in the way of adder and multiplier. Digital IF is implemented Xilinx software and simulate different parameter i.e. slice, LUTs, minimum frequency and delay.

Keywords

Filter Coefficient, Digital IF Filter, Pass-band Multi-rate Approach.

1.   Introduction

Recently, mobile communications has to ensure a wide frequency band to transmit a large amount of data with a high data rate. It is evolving into advanced communications such as LTE (4G services) to realize large amounts of data and fast transmission speed, and now has 5G mobile communications in the spotlight [1]. Therefore, spectrum allocation for mobile communications is becoming increasingly complicated. In base stations and repeaters, spectrum efficiency is maximized by using filters to minimize the interference of adjacent frequencies [2]. The filters are employed to suppress crosstalk between adjacent signals, to minimize interference between transmission and reception frequencies, and to suppress spurious emissions caused by inter modulation in the system. General base stations and repeaters in mobile communications adopt super-heterodyne receivers, which eliminate adjacent bands at intermediate frequency (IF). This system generally utilizes analogue IF band pass filters to minimize various frequency interference between heterogeneous services, adjacent service providers, and transmission and reception [3]. These analog filters include an LC filter and a surface acoustic wave (SAW) IF filter. Recently, SAW filters have been replaced with digital IF filters based on finite impulse response (FIR). The SAW filter has high frequency stability and selectivity. However, when repeaters and base stations want to change the center frequency and bandwidth for new service adaptation, a new SAW filter should be developed and embedded due to its fixed frequency characteristics. As a result, system development is needed for the changed frequency environment or is supposed to adopt multiple SAW filters of two or more types, which causes both the increase of system costs and the delay in service opening. For these reasons, development of a variable digital filter responding to changeable frequency environments is required [4].

Variable computerized FIR channels have been explored to be applied to different determinations of use administrations. Consequently, in this concise, we propose a reconfigurable computerized IF channel that can modify both the middle recurrence and transfer speed while keeping up high recurrence selectivity as a current fixed SAW channel. Since the computerized band pass channel of IF band needs to help high inspecting rate, countless taps are required for high recurrence selectivity, which brings about expanding equipment multifaceted nature altogether. Different advanced FIR structures with low unpredictability have been proposed. As indicated by this propensity, in this short, we propose a channel bank bringing down the inspecting rate so as to lessen the equipment unpredictability of a solitary computerized band pass channel. Furthermore, we additionally propose a band pass channel with a recursive multi-stage structure working at a lower inspecting rate [5].

Multi rate simply means "multiple sampling rates". A multi rate DSP framework utilizes different testing rates inside the framework. At whatever point a flag at one rate must be utilized by a framework that anticipates an alternate rate, the rate must be expanded or diminished, and some preparing is required to do as such. Along these lines "Multi rate DSP" truly alludes to the workmanship or study of changing testing rates. Multi-rate preparing discovers use in flag handling frameworks where different sub-frameworks with varying example or clock rates should be interfaced together. At different occasions multi-rate preparing is utilized to decrease computational

overhead of a framework. For instance, a calculation requires k tasks to be finished per cycle. By diminishing the example rate of a flag or framework by a factor of M, the number-crunching transfer speed prerequisites are decreased from kfs activities to kfs/M tasks every second. Customary converters are regularly hard to actualize in scarcely discernible difference huge scale coordination (VLSI) innovation. By remembering these things the general population is going for over examining converters, these converters make broad utilization of computerized flag handling.

- Higher reliability.
- Increased functionality.
- Reduced chip cost.

Those attributes are regularly required in the advanced flag handling condition of today. An essential use of computerized flag handling techniques is in deciding in the discrete-time do-fundamental the recurrence substance of a ceaseless time flag, all the more generally known as unearthly examination. All the more specifically, it includes the assurance of either the vitality range or the power range of the flag [6].

2.   Multirate Approach

Theoretically, there is an exceptionally basic and direct methodology for changing the testing pace of an advanced sign. In this methodology one only recreates the consistent time signal from the first arrangement of tests and afterward resamples the sign at the new rate by expecting that no extra enemy of associating separating is required. This methodology, in any case, has some related issues by and by. A significant handy issue is that the perfect tasks required to recreate the ceaseless time signal from the first examples and to resample the sign at the new rate can't be actualized precisely. By a cautious structure of the individual segments, these functional twists can be limited however can't be wiped out altogether [7]. A multirate channel can be characterized as a computerized channel wherein the testing pace of the information signal is changed in at least one halfway focuses. Multirate procedures can be utilized in channels for inspecting rate transformation where the info and yield rates are extraordinary, and furthermore in building channels with equivalent information and yield rates. The essential job of multirate separating in present day signal handling frameworks can be summed up in three different ways.

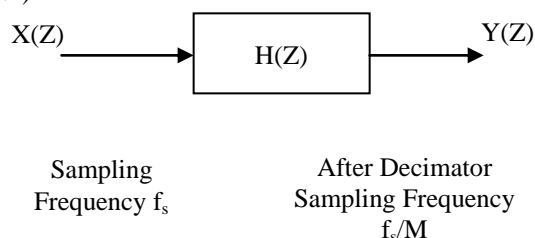It sets up an association between the data and yield limits (1.1)

X(Z) ⟶ [H(Z)] ⟶ Y(Z)

Sampling Frequency f_s

After Decimator Sampling Frequency f_s/M

Fig. 1: Block Diagram of Decimator

$$H(Z) = \frac{X(Z)}{Y(Z)} = \frac{1}{M} \sum_{x=0}^{M-1} z^{-x} \qquad (1.1)$$

$F_S \longrightarrow [\uparrow L] \longrightarrow LF_S$
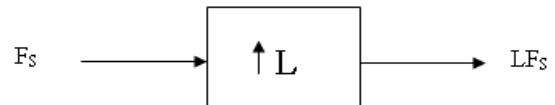
Fig. 2: Interpolation with factor L

3.   Proposed Methodology

Multirate signal handling strategies are broadly utilized in numerous territories of current designing, for example, correspondences, picture preparing, computerized sound and mixed media. The primary bit of leeway of a multirate framework is the considerable abatement of computational multifaceted nature and hence the cost decrease. The computational productivity of multirate calculations depends on the capacity to utilize distinctive inspecting rates in [3] all the while the diverse piece of the framework. The inspecting rate changes produce the undesirable impacts through the framework: otherworldly associating in the examining rate decline and ghastly pictures in the testing rate increment. The pivotal job of multirate sifting is to empower the testing rate transformation of the advanced sign without essentially wrecking the sign segments of intrigue. The multirate separating makes the overall idea of multirate signal preparing pertinent practically speaking.

Filter order of the Decimator:

Input sampling frequency: 250 Hz

Output sampling frequency: of the narrowband filter is 62.5 Hz.

Down sampling factor M=4

Specification of the anti-imaging filter of the decimator:

Specification of decimator:

$$F_s = 250Hz$$

$$\delta_s = 42dB$$

$$\delta_p = 0.08dB$$

$$\Delta f = .1217$$

$$f_{s1} = F_s - \frac{F_s}{2M}$$

$$\Delta f (normalized) = \frac{(f_{s1} - f_p)}{F_s}$$

By Kaiser formulation-

Filter order of the decimator $N_1 = 17$

Design of Narrow band filter

Sampling frequency, $F_s = 62.5Hz$

Pass band ripple, $\delta_p = 0.08dB$

Stop band ripple, $\delta_s = 42dB$

Pass band frequency, $f_p = .825Hz$

Stop band frequency, $f_s = 4.15Hz$

$\Delta f (normalized) = .7767$

Filter order of the narrow band filter $N_2 = 38$

Filter order of the Interpolator:
Input sampling frequency: 62.5 Hz
Output sampling frequency: of the narrowband filter is 250 Hz.
Up sampling factor L=4
Specification of the anti-imaging filter of the interpolator:

$F_s = 62.5Hz$

$\delta_s = 42dB$

$\delta_p = 0.08dB$

$\Delta f = .2467$

L=4

$\Delta f (normalized) = \dfrac{(f_{s1} - f_p)}{F_s}$

By Kaiser Formulation

Filter order of the interpolator $N_3 = 9$

4.   Simulation Result

The proposed architecture has very low hardware complexity compared to direct approach based structures, because direct method requires more multiplier compare to proposed architecture. In the proposed architecture, calculate the decimator and interpolator structure for design a narrow band filter.

Table 1: Comparison Result for Previous and Proposed Approach for N=5

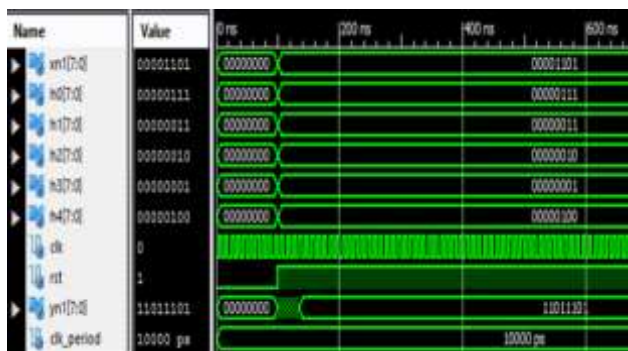|	Previous Approach	Proposed Approach
Number of Slice	45	34
Number of Flip Flops	39	32
No. of Slice LUTs	63	57
MCPD (ns)	17.564	14.352

Fig. 3: Output Test Bench Waveform of Narrow Band Filter (Filter Coefficient N=5)

Table 1 shows the theoretical analysis of direct method & multi-rate approach for different filter coefficient and sampling frequency. Table 2 shows cell usage for the Comparison of Performance of the Proposed Implementation and the Existing Implementation of Narrow Band Filter.

The design as were discussed in figure 3 and figure 4 were implemented using VHDL and then were tested on model sim to determine the number of slice and maximum high frequency. In figure 5, figure 6 and figure 7 have shown the output waveform of narrow band filter and chat between filter order and slices. In figure 7, compare the result between numbers of slice and filter order. Increase the filter order also increase the number of slice shown if figure 7.

Table 2: Comparison Result for Previous and Proposed Approach for N=9

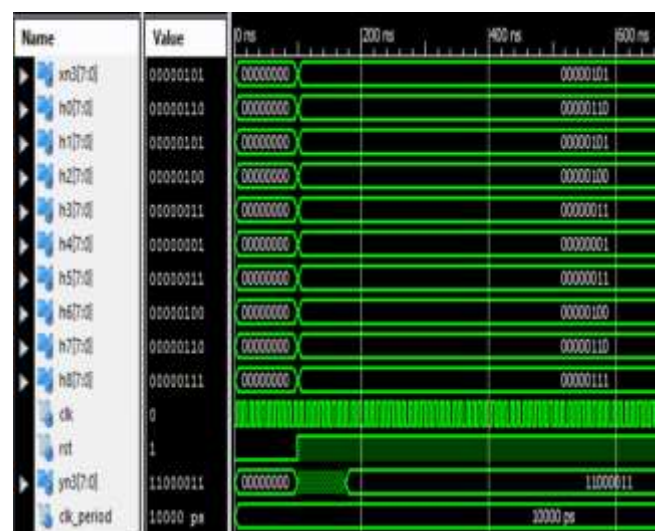|	Previous Approach	Proposed Approach
Number of Slice	74	66
Number of Flip Flops	71	64
No. of Slice LUTs	141	113
MCPD (ns)	22.432	17.085

Fig. 4: Output Waveform of 9_tap Narrow Band Filter

5.   CONCLUSION

Straight time-invariant frameworks work at a solitary examining rate which is same at the information and at the yield of the framework and at all hubs inside the framework. Consequently, in a straight time invariant (LTI) framework, the testing rate doesn't change in various phases of the framework. Though, frameworks that utilizes distinctive testing rates at various stages are known as the multirate frameworks. The multirate procedures are utilized to change over the given testing rate to the ideal examining rate and to give distinctive inspecting rates through the framework without devastating the sign parts of intrigue.

Thusly, in this short, we propose a reconfigurable advanced IF channel that can change both the middle recurrence and transfer speed while keeping up high recurrence selectivity as a current fixed SAW channel. Since the computerized band pass channel of IF band needs to help high inspecting rate, countless taps are required for high recurrence selectivity, which brings about expanding equipment multifaceted nature essentially. Different advanced FIR structures with low intricacy have been proposed. As indicated by this inclination, in this concise, we propose a channel bank bringing down the examining rate so as to diminish the equipment multifaceted nature of a solitary advanced band pass channel.

REFERENCES

[1]   Hyobeen Park, Myoungseok Yu, Yunho Jung, and Seongjoo Lee, "Design of Reconfigurable Digital IF Filter with Low Complexity", IEEE Transactions on Circuits and Systems II, 2018.

[2]   Dwaipayan Ray, Nithin V. George, and Pramod Kumar Meher, "Efficient Shift-Add Implementation of FIR Filters Using Variable Partition Hybrid Form Structures", IEEE Transactions On Circuits And Systems–I: Regular Papers, Vol. 32, Issue 6, June 2018.

[3]   Mohammed Alawad and Mingjie Lin, "Memory-Efficient Probabilistic 2-D Finite Impulse Response (FIR) Filter", IEEE Communication Letters, Vol. 99, No. 04, April 2017.

[4]   A. Mehrnia, M. Dai, A. N. Willson, "Efficient half band FIR filter structures for RF and IF data converters", IEEE Transactions on Circuits and Systems II: Express Briefs63, no. 1 (2016): 64-68.

[5]   S. Dhabu, and A. P. Vinod, "Design and FPGA Implementation of Reconfigurable Linear-Phase Digital Filter With Wide Cutoff Frequency Range and Narrow Transition Bandwidth", IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 63, no. 2, pp. 181-185, 2016

[6]   Basant Kumar Mohanty, and Pramod Kumar Meher, High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 78, No.06, April 2016.

[7]   Indranil Hatai, Indrajit Chakrabarti, and Swapna Banerjee, "An Efficient VLSI Architecture of a Reconfigurable Pulse-Shaping FIR Interpolation Filter for Multi-standard DUC", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 23, No. 6, June 2015.

[8]   Sang Yoon Park and Pramod Kumar Meher, "Efficient FPGA and ASIC Realizations of DA-Based Reconfigurable FIR Digital Filter", IEEE Transactions on Circuits And Systems-Ii: Express Briefs, 2014.

[9]   Pramod Kumar Meher, Sch. of Autom., IEEE, Shrutisagar Chandrasekaran, Member, IEEE, andAbbes Amira, Senior Member, IEEE, "Distributed Arithmetic for FIR Filter implementation on FPGA", Proceedings of IC-BNMT 2011.

[10]   Ms. S.Manjui, Mr. V. Sornagopae, "An Efficient SQRT Architecture of Carry Select Adder Design by Common Boolean Logic", 978-1-4673-5301-4/13/$31.00 ©2013 IEEE.

[11]   Basant K. Mohanty, And Pramod Kumar Meher, "A High-Performance Energy- efficient Architecture For FIR Adaptive Filter Based On New Distributed Arithmetic Formulation Of Block LMS Algorithm", in IEEE Transactions on Signal Processing, Vol. 61, No. 4, PP. No. 45-52, February, 2013.