FPGA Implementation of the CRC using Parallel Pipelining Architecture for Error Detection and Correction

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Abstract— **VLSI architecture for fast extended Golay encoder and decoder are presented in this paper. The extended golay code encode and decode of the bit is (24, 12, 8) format. The first bit of the format is represent the transmit Golay encoder bit, second bit of the format is represent the polynomial bit and third bit of the format is represent the hamming distance. Extended Golay codes are detection up to eight bit error and correction up to three bits. The extended Golay code is main block of the cyclic redundancy check (CRC). CRC is error detection code commonly used in wireless communication system. The extended Golay code is implemented Xilinx software with vertex-2p device family. The extended Golay code is implemented in term of number of slice, number of LUT and maximum combinational path delay compared with existing Golay code.**

Index Terms- Binary Golay Code (23, 12, 7), Extended Golay Code (24, 12, 8), Adder, Weight Measurement Unit

I.   INTRODUCTION

With the rapid growth of digital communications, such as Digital Audio Broadcasting (DAB) and ATM systems, increased data rate and advanced error control coding techniques are required. Consequently, the parallelism innate in the unraveling calculation and the territory productive rapid VLSI designs must be abused. The (24,12,8) expanded Golay code is a notable blunder remedying code, which has been effectively applied in a few existing correspondence frameworks to improve the framework bit-error rate (BER) execution. One goal of this research was to provide a strong error protection for the important head information in the transmission of the high quality compressed music signal of the DAB system. The equal Golay decoder can be, obviously, utilized for the most part to ensure the information transmission or capacity against channel mistakes for rapid information preparing.

Various delicate choice interpreting of the (24, 12) twofold Golay code were seriously examined over the most recent couple of years and point by point examination of computational unpredictability were talked about. Notwithstanding, none of these calculations have been acknowledged proficiently with equal VLSI circuits. This paper presents a full equal change interpreting procedure with look-ahead mistake rectification and a quick delicate choice translating for (24, 12, 8) expanded Golay code. The zone proficient equal VLSI models and the PC reproduction results are additionally exhibited. The look-up table used in this improved algorithm consists of syndrome patterns and corresponding error patterns which have one to three errors occurred in the message block of the codeword. Then the look-up table contains only 25 syndrome patterns and corresponding error patterns. Suppose that there are only three or less errors occurred in (15, 5, 7) BCH codeword. Due to the latter part of H is a 10x10 identity matrix and $S = eH^T$, if the weight of S $w(S){\le}3$, it means at most three errors only occurred in the parity check block and the location of 1 in S is just the error location in the parity check block. Then shift the syndrome right 5 bits to form a 15-bit length word and minus (modulo 2) the received codeword to decode. If $w(S) \ge 4$, it means at least one error occurred in the message block. First, the syndrome minus (modulo 2) all syndrome patterns in the table to obtain the difference and compute the weight of these difference, respectively.

II.   GOLAY CODE

The Binary Golay code is spoken to as (23, 12, 7) that delineates that length of codeword is 23 bits, while message is of 12 bits and the base separation between two parallel Golay codes is 7.

$$A = \begin{bmatrix} 0 & 1 & 1 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & 1 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 0 \\ 1 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 0 & 1 \\ 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 \\ 1 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 \\ 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 \\ 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 \\ 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 \\ 1 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 \\ 1 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 \end{bmatrix}$$

A Galois field (GF) is important to build double codes. All in all, parallel field is signified by GF (2), which underpins distinctive twofold number juggling activities. The age of coding arrangement needs a generator polynomial. The conceivable generator polynomials [13] over GF (2) for Golay (23, 12, 7) code are x11 + x10 + x6 + x5 + x4 + x2 + x1 and x11+x9+x7+x6+x5+x1+1. Right now, is considered as the trademark polynomial. The rest of the long division gives the necessary check bits. At last, attaching the produced check bits with the message gives us the all-encompassing Golay codeword. The all-inclusive Golay code (24, 12, 8) can be produced by affixing an equality bit with the twofold Golay code or utilizing a generator grid G, which is characterized as [I, B], where I signifies a personality network of request 12.

III. PROPOSED METHODOLOGY

The primary byte of the ROM code is a cyclic excess check. On the off chance that a Golay code is determined from the accompanying 12 message bits, at that point concurrence with this worth infers that the ROM code is without blunder. Despite the fact that this doesn't need to be utilized in basic applications.

The hypothesis behind this is somewhat troublesome, yet is essentially working with polynomials with parallel numbers as coefficients- - that may be, 1 or 0. The xor work is the main straight capacity of two bits. This move register compares to the polynomial $x^8 + x^5 + x^4 + 1$. It is anything but difficult to copy the move register in programming, in spite of the fact that the PIC can just set, clear or test bits, not move them or do tasks with them.
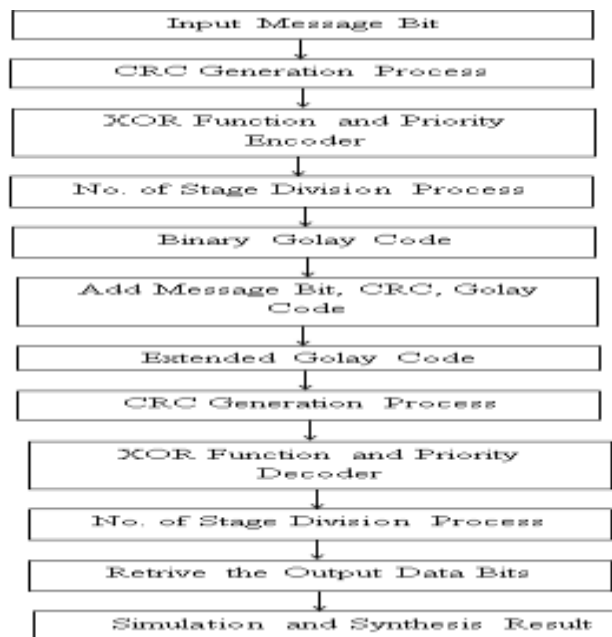

Figure 1: Flow Chart of Golay Encoder and Decoder

Golay Encoder:-

The encoding algorithm of Golay code is based on the cyclic redundancy check generation process and it includes Conversion of binary Golay code into extended Golay code. The check bit generation example is shown below.

Figure 2: Golay Encoder Example

In above example, 555h information data to be encoded. Hence m(x) = 555h in binary format is represented as 0101 0101 0101 0000 0000 000.The polynomial used in this example is P(X)= AE3h and the binary representation of this polynomial is 1010 1110 0011.The check bit generated by using modulo 2 division is 686h.A Golay code word is generated by taking message of 12 bits and adding 11 check bits which are obtained from modulo2 division process ,as with CRC. Hence, the binary Golay [23, 12,7] code word is 555686h.

Golay Decoder:-

First we collect the encoder output data bits and to modify the decoder architecture using extended Golay code architecture. This architecture is to analysis the overall encoder output data. Then to calculate the majority output data bits and to compare the Golay code architecture data bit location. Then to check the CRC key data bits. So we apply the CRC calculation process and to solve the final data bit in '0' level. Then to collect the original message data bits. The output bits are not equal to '0' level, so the error bits are present in receiving bits.

Binary and Extended Golay Code Architecture:-

Binary Golay code has two types the first one is Golay (23, 12, 7). In this (23, 12, 7) Golay code, if we send 12 bit message, then we add additional 11 bits to it. After adding check bits which are obtained from CRC generation process to the 12 bit message, total will come to 23 bit now, we send this 23 bit.

The 23 bit message obtained at receiver side is able to convert these 23 bit messages into 12 bit message even if there is distortion of 12 bit. This is applicable to all 23 bits and hence it is called a perfect Golay code. Another type is Golay (24, 12, 8).This code detects up to 4, but it can correct up to 3 bits error. The architecture of Golay code encoder is divided into two parts one is generation of G_{23} and other is conversion of G_{23} to G_{24}.
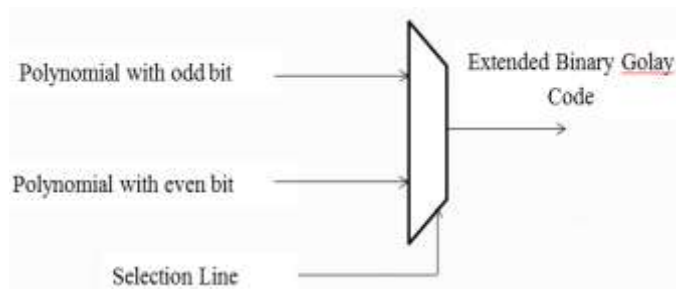

Figure 3: Binary Golay Code to Extended Binary Golay Code

IV. SIMULATION RESULT

All the designing and experiment regarding algorithm that we have mentioned in this paper is being developed on Xilinx 6.1i updated version. Xilinx 5.2i has couple of the striking highlights, for example, low memory prerequisite, quick troubleshooting, and minimal effort. The most recent arrival of ISETM (Integrated Software Environment) plan apparatus gives the low memory necessity inexact 27 rate low. ISE 6.1i that gives propelled devices like shrewd order innovation with better utilization of their processing equipment gives quicker planning conclusion and higher caliber of results for a superior time to structuring arrangement. ISE 6.1i Xilinx instruments grants more noteworthy adaptability for plans which influence implanted processors. The ISE 6.1i Design suite is joined by the arrival of chip scope ProTM 6.1i troubleshoot and check programming. By the guide of that product we investigate the program effectively. Also included is the newest release of the chip scope Pro Serial IO Tool kit, providing simplified debugging of high-speed serial IO designs for Virtex-2 FX and Virtex-2P LXT and SXT FPGAs. With the help of this tool we can develop in the area of communication as well as in the area of signal processing and VLSI low power designing.

1. CRC Technique

The architecture of CRC Golay code encoder has been implemented in field programmable gate array using Xilinx ISE tool.
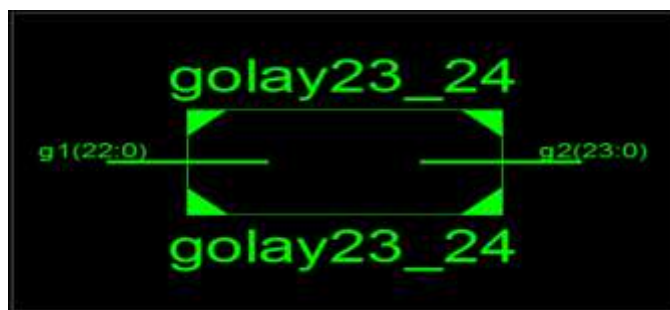

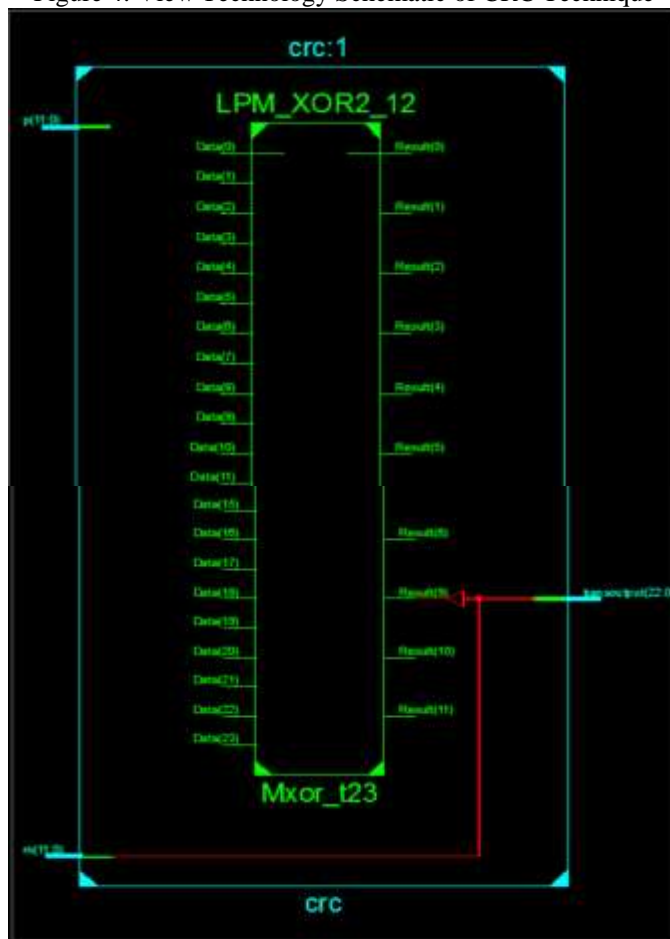
Figure 4: View Technology Schematic of CRC Technique

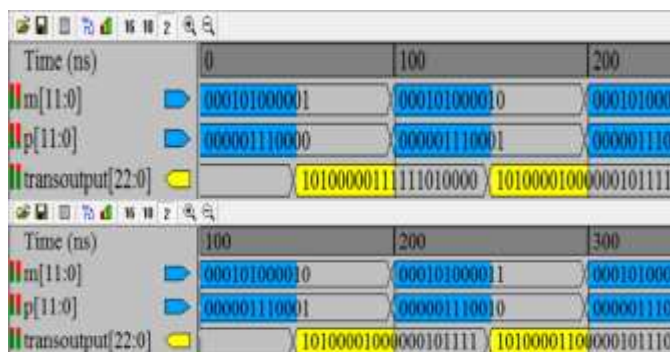Figure 5: RTL View of CRC Technique

Figure 6: Output Waveform of CRC Technique

2.　　Binary Golay Code to Extended Golay Code:-

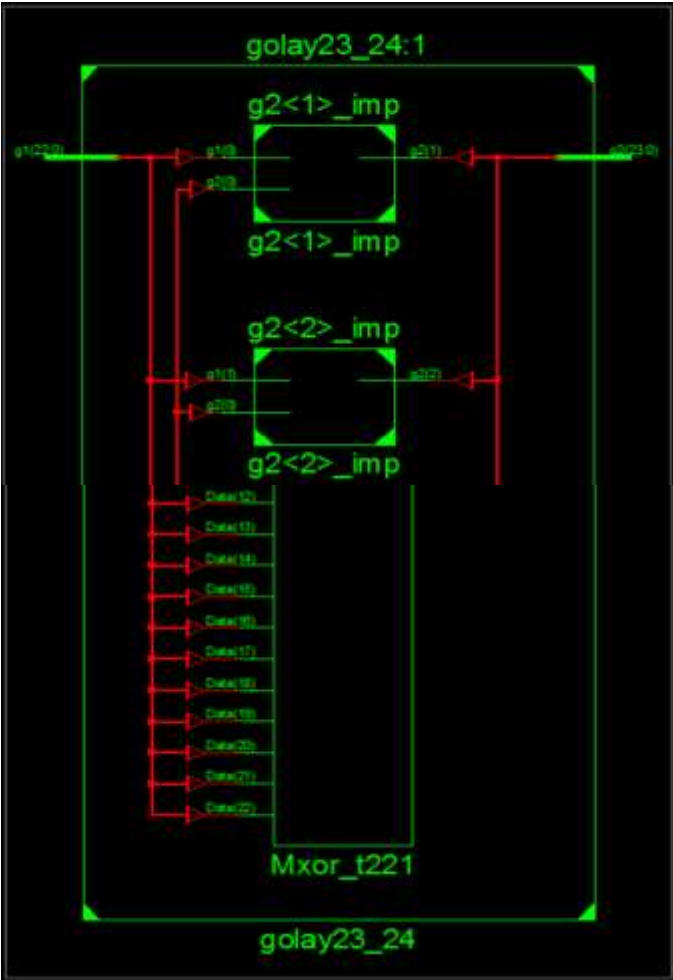Figure 7: View Technology Schematic of Extended Golay Code

Figure 8: RTL View of Extended Golay Code

Figure 9: Output Waveform of Extended Golay Code

3. Weight Measurement Unit:

The weight measurement unit primarily counts the number of binary 1 in the sequence, which can be efficiently done by the circuit shown in Fig. 4, which results in less critical path delay.
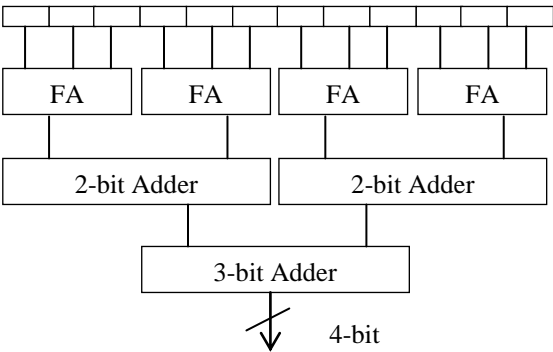

Figure 10: Structure of Weight Measurement

Table 1: Comparison result for weight measurement

Spartan-3			
Architecture	Slice	LUTs	Delay
Previous Algorithm	11 out of 768	19 out of 1536	13.069 nsec
Proposed Architecture	10 out of 768	18 out of 1536	11.823 nsec
Virtex-2			
Previous Algorithm	11 out of 256	19 out of 512	9.106 nsec
Proposed Architecture	10 out of 256	18 out of 512	8.139 nsec
Virtex-2p			
Previous	11 out	19 out of	8.205 nsec

Algorithm	of 1408	2816	
Proposed Architecture	10 out of 1408	18 out of 2816	7.350 nsec

Table 2: Result for proposed Encoder and Decoder for Extended Golay code

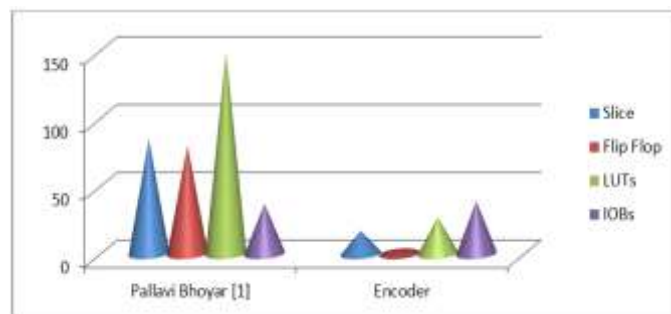| Architecture	Slice	Flip Flop	LUTs	IOBs
Pallavi Bhoyar [1]	85	80	149	37
Encoder	17	3	27	39
Pallavi Bhoyar [1]	60	34	113	26
Decoder	53	23	92	47

Figure 11: Shows the bar graph of the existing algorithm and proposed architecture
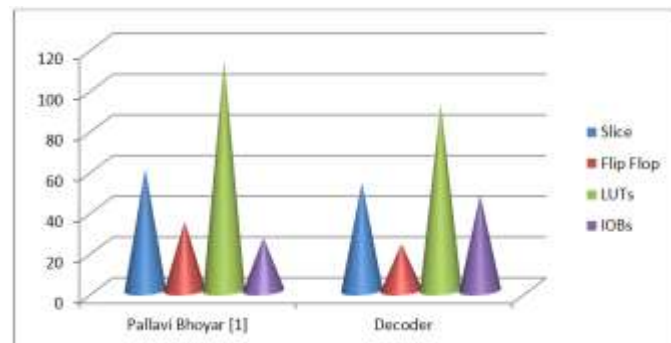

Figure 12: shows the bar graph of the delay in different device family

V. CONCLUSION

Proficient equipment engineering for both paired Golay encoder and expanded twofold Golay encoder have been planned and executed in the wake of confirming the proposed calculation. The outcomes got from reproduction express that the proposed equipment design for encoder supplants the customary LFSR-based CRC age plans. Also, the proposed equipment module for decoder demonstrates better execution to a portion of the ongoing distributions thinking about different execution measurements. These equipment modules for encoder and decoder can be a decent contender for different applications in fast correspondence joins, photograph spectroscopy, and ultrasonography.

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