AN OVERVIEW AND REVIEW ON MULTIPLIER IN VHDL

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INTRODUCTION

Multipliers are most commonly used in various electronic applications e.g. Digital signal processing in which multipliers are used to perform various algorithms like FIR, IIR etc. Digital computer arithmetic is an aspect of logic design with the objective of developing appropriate algorithms in order to achieve an efficient utilization of the available hardware. The basic operations are addition, subtraction, multiplication and division. In this, we are going to deal with the operation of additions implemented to the operation of multiplication. The repeated form of the addition operations and shifting results in the multiplication operations. Given that the hardware can only perform relatively simple and primitive set of Boolean operations, arithmetic operations are based on a hierarchy of operations that are built upon the simple ones. In VLSI designs, speed, power and chip area are the most often used measures for determining the performance and efficiency of the VLSI architecture. Multiplications and additions are most widely and more often used arithmetic computations performed in all digital signal processing applications.

In this project we are going to compare the performance of different adders implemented to the multipliers based on area and time needed for calculation. On comparison with the carry look-ahead adder (CLAA) based multiplier the area of calculation of the carry select adder (CSLA) based multiplier is smaller and better with nearly same delay time. Here we are dealing with the comparison in the bit range of n*n (32*32) as input and 2n (64) bit output. Hence, to design a better architecture the basic adder blocks must have reduced delay time consumption and area efficient architectures. The demand is of DSP style systems for both less delay time and less area requirement for designing the systems. Our interest is in the basic building blocks of arithmetic circuits that dominate in DSP applications, VLSI architectures, computer applications and where ever reduced area computation is needed.

1.1 Carry look ahead Adder (CLAA)

Carry Look Ahead Adder can produce carries faster due to carry bits generated in parallel by an additional circuitry whenever inputs change. This technique uses carry bypass logic to speed up the carry propagation.

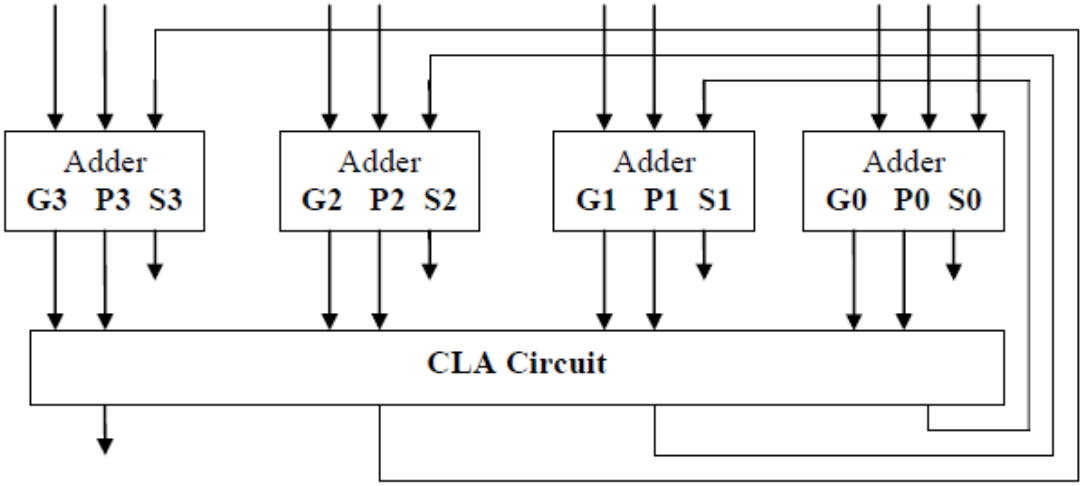

FIGURE 1.1 4-BIT CLAA Logic equations

Let ai and bi be the augends and addend inputs, ci the carry input, si and ci+1 , the sum and carry-out to the ith bit position. If the auxiliary functions, pi and gi called the propagate and generate signals, the sum output respectively are defined as follows. pi = ai + bi gi = ai bi si = ai xor bi xor ci ci+1 = gi + pici .

- As we increase the no of bits in the Carry Look Ahead adders, the complexity increases because the no. of gates in the expression Ci+1 increases. So practically its not desirable to use the traditional CLA shown above because it increase the Space required and the power too.
- Instead we will use here Carry Look Ahead adder (less bits) in levels to create a larger CLA. Commonly smaller CLA may be taken as a 4-bit CLA. So we can define carry look ahead over a group of 4 bits. Hence now we redefine terms carry generate as [Group Generated Carry] g[i,i+3] and carry propagate as [Group Propagated Carry] p[i,i+3] which are defined below.

1.2 Carry select adder (CSLA)

In Carry select adder scheme, blocks of bits are added in two ways: one assuning a carry-in of 0 and the other with a carry-in of 1.This results in two precomputed sum and carry-out signal pairs (s0i-1:k , c0i ; s1i-1:k , c1i) , later as the block's true carry-in (ck) becomes known , the correct signal pairs are selected. Generally multiplexers are used to propagate carries.

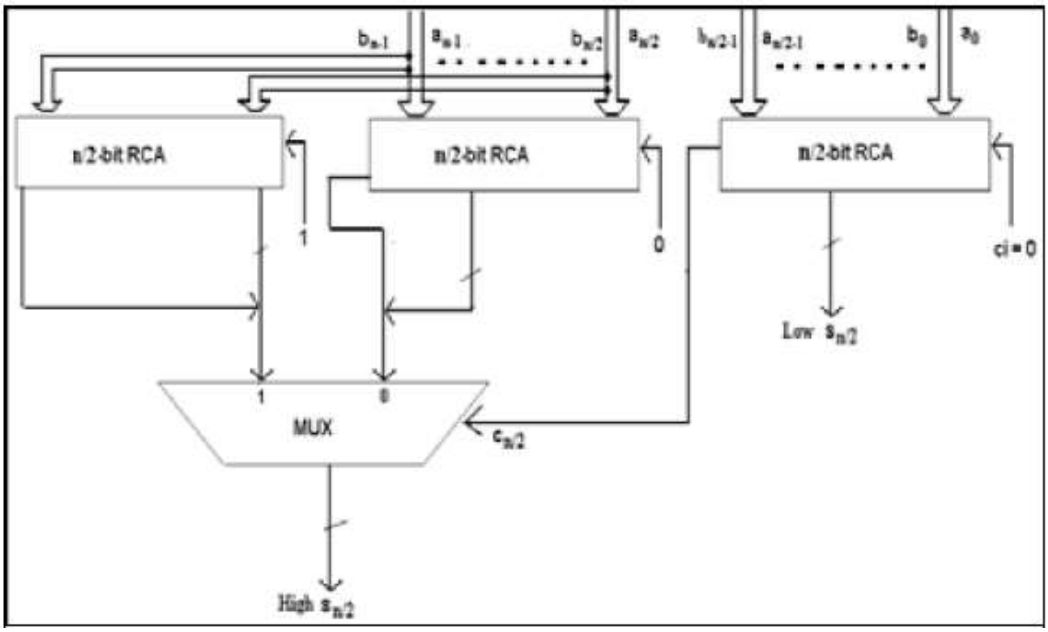

FIGURE 1.2 A Carry Select Adder with 1 level using n/2- bit RCA

- Because of multiplexers larger area is required.
- Have a lesser delay than Ripple Carry Adders (half delay of RCA).
- Hence we always go for Carry Select Adder while working with smaller no of bits.

P. C. H. Meier et.al [1996] "Exploring Multiplier Architecture and Layout for low Power", , Multiplication represents a fundamental building block in all DSP tasks. Due to the large latency inherent in multiplication, schemes have been devised to minimize the delay. Two methods are common in current implementations: regular arrays and Wallace trees. Previous gate-level analyses have suggested that not only are Wallace trees faster than array schemes, they also consume much less power. However these analyses did not take Wiring into account,

resulting in optimistic timing and power estimates. We develop a simplified comparative layout methodology to analyze the effect of physical layout on these designs. Results for short bit-width (8, 16, 24 bit) DSP multipliers show that while wiring has a major impact on signal delay and power, Wallace trees still show roughly a 10% power advantage overarray-based designs.

Sertbas et.al [2004] "A performance analysis of classified binary adder architectures and the VHDL simulations",. In this paper, the four binary adder architectures belong to a different adder class are studied and compared with each other to analyze their performances.Comparisons include the unit-gate models for area and delay. As the performance measure, the product of the area and the delay is used. By a VHDL simulator, the adder structures are simulated to verify the functional correctness and to measure delay times. The other adders, the carry look ahead (CLA) and the carry select (CSLA) adders, behave similar and, have medium area and delay requirements with respect to RCA and COSA. In the studied adder structures, COSA and CLA architectures have the highest performance; result in the lowest area-delay product values.

P. Asadi et.al [2007]. **"A novel highs-speed 54-54 bit multiplier",** A new 54*54 bit multiplier using high speed CLA has been fabricated by CMOS technology. This paper presents a self timed carry look ahead adder in which the logic complexity was a linear function of n, the number of inputs. Ouradder has the best area time efficiency. The simulation results meet the estimated delay closely. This work has 7.6% reduction in delay and 8.6%improvement in power consumption.

RaminderPreet et.al [2009], In this paper, design of two different array multipliers are presented, one by using carry-look-ahead (CLA) logic for addition of partial product terms and another by introducing Carry Save Adder (CSA) in partial product lines. The multipliers presented in this paper were all modeled using VHDL (Very High Speed Integration Hardware Description Language) for 32-bit unsigned data. The comparison is done on the basis of three performance parameters i.e. Area, Speed and Power consumption.. Multiplier with CSA gives better result in terms of speed (78.3% improvement), area (reduced by 4.2%) and power consumption (decreased by 1.4%).This paper presents two different multipliers that are modeled

using VHDL. According to the results obtained, implementation of CSA logic in each partial product lines improves overall performance of multiplier unit (Speed improved by 78.3%, Area reduced by 4.2% and power consumption decreased by 1.4%) as compare to CLA logic. This work is performed on 32-bit unsigned data. Therefore, it can be extended for signed multiplication.

HasanKrad et.al [2010], analysis on the performance analysis of two different multipliers for unsigned data, one uses a carry-look ahead adder and the second one uses a ripple adder. The paper's main focus is on the speed of the multiplication operation on these 32-bit multipliers which are modeled using VHDL, A hardware description language. The multiplier with a carry-look-ahead adder has shown a better performance over the multiplier with a ripple adder in terms of gate delays. Under the worst case, the multiplier with the fast adder shows approximately twice the speed of the multiplier with the ripple adder. The multiplier with a ripple adder uses time = 979.056 ns, while the multiplier with the carry-look-ahead adder uses time = 659.292 ns. This work can be extended to cover signed multipliers using VHDLTwo different multipliers using a fast carry-look-ahead adder and a ripple adder have been modeled and simulated using VHDL. In other words, the multiplier with the carry-look-ahead adder has approximately twice the speed of the multiplier with the ripple adder, under the worst case.

Nageswarara et.al[2012], worked on analysis of the performance of different types of adders are analyzed. And carry select adder (CSLA) is the lowest delay compare to other adders. Carry select adder is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. From the structure of the CSLA, there is a possibility for increasing the speed and reducing the area and in the CSLA. This work uses a simple and efficient gate- level modification to significantly reduce the area and power of the CSLA. Based on this modification 8-, 16-, 32 bit CSLA architecture have been developed and compared with the regular CSLA architecture. The proposed design has increased speed and reduced area and power as compared with the regular CSLA with only a slight increase in the delay.

V.Vijayalakshmil et.al [2013],presented Design and Implementation of 32 Bit Unsigned Multiplier Using CLAA and CSLA. Both the VLSI design of multiplier multiplies two 32-bit

unsigned integer values and gives a product term of 64-bit values. The CLAA based multiplier uses the delay time of 99ns for performing multiplication operation where as in CSLA based multiplier also uses nearly the same delay time. But the area needed for CLAA multiplier is reduced to 31 % by the CSLA based multiplier to complete the multiplication operation. This 32 bit multiplier can be further extended to 64 bit multiplier and 128 bit multiplier using the proposed method for multiplication operation can be done as future work.

Analysis Methodology

- Cell-level generators for the multipliers' partial product reduction networks: where "cell" here means the component (3,2) carry save adders and single-product AND gates needed in the design.
- Cell-level generators for multipliers' final 2-level reducing adders: each style requires a final addition, and each can use different adder styles to achieve different tradeoffs.
- Cell characterization: to understand power consumption in each of these primitive component cells, as implemented byconventional static CMOS circuits.
- Layout model: to allow exploration and first-order estimation of wiring, delay and area, we need a simple layout style that is easily automatable, yet not so detailed as to demandmanual, full-custom layout.
- Power and delay estimation: to measure power and delay for the completed multiplier layouts–including the delay and capacitance of all the intercell wiring.

Topic Name	**Exploring Multiplier Architecture and layout for low power**	**A novel high-speed 54-54 bit multiplier**	**Energy and Delay Optimization of 64 bit carry look ahead adder with CMOS design**	**Design & implementation of 32 bit unsigned Multiplier using CLAA & CSLA.**
Year	**1996**	**2007**	**2009**	**2013**
Author Name & Publication	**P.C.H.MENIER&L.R.CARLEY**	**P.Asadi and K.Navi American Journal of Applied Science**	**Radu Zlatanovici IEEE Journal**	**v.vijayalakhsmi IEEE Journal**
Methodologies Used for analysis	**1Regular arrays 2.Wallace Trees(8,16,24 bit) DSP multipliers**	**CMOS TECHNOLOGY**	**16 bit full tress Radix (kogge stone & ladner Fischer) for analysis**	**Array Multiplier**
Keywords &Tools software used	**Multipliers, Array architecture**	**Booth Encoder Multiplier, Compressor, CMOS, Adder**	**CMOS; Adder; CLAA**	**CLAA; CSLA; VHDL Modeling & simulation, xiling**
Parameters **1. Power** **2. Area** **3. Speed**	**Less power 10%**	**8.6% improvement in power consumption** **7.6% reduction in delay**	**Low Power**	**Area delay product reduced to 31%**
Proposed Work	**The model is clearly coarse, but capable of making basic predictions for area, for average power, and delay**.	**A 54-54bit CMOS parallel multiplier was proposed to reduce the number of transistor, delay and power consumption.**	**By analyzing te impact of the main design choices on adder behaviour in the energy delay space.**	**This 32 bit multiplier can further extended to 64 bit and 128 bit multiplier using proposed method for multiplication operations.**

CONCLUSION

This work evaluates the performance of the proposed designs in terms of delay, speed(frequency)and memory. The results analysis shows that the proposed CSLA structure is better than the regular CSLA. And it is implemented in multiplier as application for efficient performance. Performance analysis of various Adders is analyzed in terms of delay, frequency and memory from these carry select adder is better parameter values than other adders. and the regular carry select is further modified for speed and area efficiency. The proposed design that modified carry select adder having better speed than regular carry select adder and area also reduced .by this architecture the efficient multiplier designed. Finally, the desirable continuation of this work is to investigate the other binary adder architectures and to extend to the performance comparisons for the all adder structures.

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