Study of Design and Implementation of PLL clock generator

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Abstract **-** The digital phase-locked loop, DPLL, is a circuit that is used frequently in modern integrated circuit design. Consider the waveform and block diagram of a communication system, Digital data1 is loaded into the shift register at the transmitting end. The data is shifted out sequentially to the transmitter output driver. At the receiving end, where the data may be analog (and, thus, without well-defined amplitudes) after passing through the communication channel, the receiver amplifies and changes the data back into digital logic levels. The next logical step i n this sequence is to shift the data back into a shift register at the receiver and process the received data. However, the absence of a clock signal makes this difficult. The DPLL performs the function of generating a clock signal, which is locked or synchronized with the incoming signal. The generated clock signal of the receiver clocks the shift register and thus recovers the data. This application of a DPLL is often termed a clock-recovery circuit or bit synchronization circuit. This paper basically reviews the design and implementation of DLL.

Keywords **-** DPLL, Clock generator, VCO, SoC, Charge pumps

I .INTRODUCTION

PLLs are extensively used to generate on-chip clocks in high-performance digital systems. These are incorporated into almost every large-scale mixed-signal and digital system-on-chip (SoC). A PLL can be integrated into a single IC to fan out multiple clocks of different frequencies. The other absolute property of such a distribution system is that all the output clocks can be made to have a fixed phase relationship to each other.

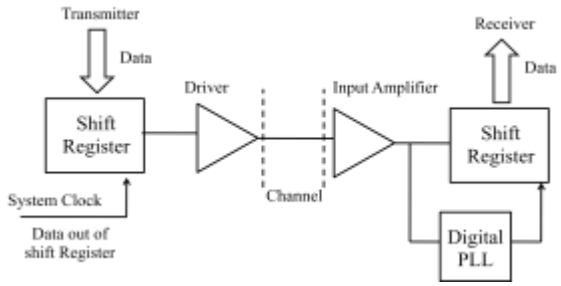

Fig.1 Block Diagram of a communication system using DPLL
This feature is useful in systems where it is required to deliver varying frequency signals to different digital blocks while keeping their operation in sync.

Phase-locked loops are widely employed in radio, telecommunications, computers and other electronic applications. They can be used to demodulate a signal, recover a signal from a noisy communication channel, generate a stable frequency at multiples of an input frequency (frequency synthesis), or distribute precisely timed clock pulses in digital logic circuits such as microprocessors. Since a single integrated circuit can provide a complete phase-locked-loop building block, the technique is widely used in modern electronic devices, with output frequencies from a fraction of a hertz up to many gigahertz.

II. DESIGN

PLL: A basic PLL is a negative feedback system that receives an incoming oscillating signal and generates an output waveform that exerts the same phase/frequency relationship as the input signal. This is achieved by constantly comparing the phase of output signal to the input signal with a phase/frequency detector (PFD).

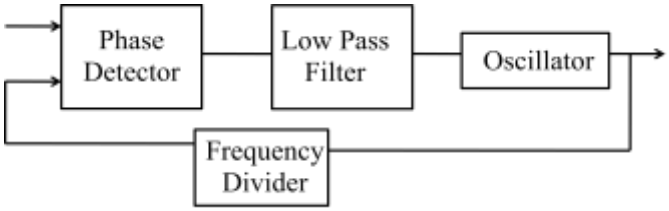

Fig.2. Block diagram of a Digital PLL

A PLL is a closed-loop feedback system that sets fixed phase relationship between its output clock phase and the phase of a reference clock. A PLL is capable of tracking the phase hanges that falls in this bandwidth of the PLL. A PLL also multiplies a low-frequency reference clock CKref to produce a high-frequency clock CKout this is known as clock synthesis. A PLL has a negative feedback control system circuit. The main objective of a PLL is to generate a signal in which the phase is the same as the phase of a reference signal. This is achieved after many iterations of comparison of the reference and feedback signals. In this lock mode the phase of the reference and feedback signal is zero. After this, the PLL continues to compare the two signals but since they are in lock mode, the PLL output is constant.

In general a PLL consists of five main blocks:

1. Phase Detector or Phase Frequency Detector (PD or PFD)
2. Charge Pump (CP)
3. Low Pass Filter (LPF)
4. Voltage Controlled Oscillator (VCO)
5. Divide by N Counter

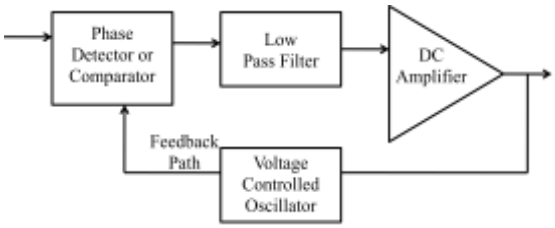

Fig.3. Block Diagram of Digital PLL

III. DIGITAL PLL DESCRIPTION

A PLL is comprised of a phase/frequency detector (PFD), charge pump (CP), a low-pass filter (LPF), and a voltage-controlled oscillator (VCO). An input reference frequency (FREF) is sent to one of the PFD inputs. The other input terminal of PFD is driven by a divided version of VCO output signal to provide a negative feedback to the loop. The PFD detects differences in phase and frequency between the reference and feedback inputs to generate compensating up (UP) or down (DN) signals.

If reference input (FREF) occurs before that of feedback input (FBK), indicating that the VCO is running too slowly, the PFD produces a UP signal that lasts until the rising edge of the FBK. If the FBK occurs before FREF, the PFD produces a DN signal that is triggered on the rising edge of the FBK input and lasts until the rising edge of FREF. If the FBK frequency is less than that of FREF, the pulse-width of the UP signal is greater than the width of DN signal and vice versa. In this way, the PFD produces control signals that are unique for any phase and frequency relationship between reference and feedback signal.

These control signals are then passed through CP and a loop filter to generate a control voltage (Vctrl), which feeds into a VCO, the frequency of which is dependent on the control voltage input. Thus, based on phase/frequency relationship of input and feedback signal, the VCO can be forced to run faster or slower, which finally locks to oscillate at a fixed frequency once two inputs at PFD are phase/frequency aligned. The output of the VCO is an internally generated oscillator waveform. At steady state, the PLL system frequency is: The PLL is designed to operate within a limited band of input frequencies. If FREF is outside the defined band, circuit will not lock, thus FVCO will be different than expected one.

FPLL = FVCO = FREF * P
Where:
FPLL = PLL frequency
FREF = Reference frequency
P = Feedback divider

The range of FREF from Fmin to Fmax where the PLL remains in locked condition is called the lock range of the PLL. Out of lock range (i.e., Fmax < Fref < Fmin), the PLL becomes unlocked. When the PLL is unlocked, the VCO oscillates at the frequency Ffr, called the free-running frequency of VCO. The PLL can achieve the lock again if FREF gets close enough to Ffr. This narrow band (△Fc) of frequency, centered at Ffr so that the initially unlocked PLL acquires the lock again, is called the 'capture range' of the PLL.

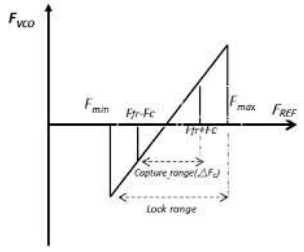

Fig.4. Characteristics plot VCO freq vs Reference freq

IV. Architecture of PLL

The architecture of a charge-pump PLL is shown in Figure 4. A PLL comprises of several components. They are (1) phase or phase frequency detector, (2) charge pump, (3) loop filter, (4) voltage-controlled oscillator, and (5) frequency divider.
The functioning of each block is briefly explained below.

A) Phase frequency Detector

The "Phase frequency Detector" (PFD) is one of the main part in PLL circuits. It compares the phase and frequency difference between the reference clock and the feedback clock. Depending upon the phase and frequency deviation, it generates two output signals "UP" and "DOWN". Figure below shows a traditional PFD circuit.

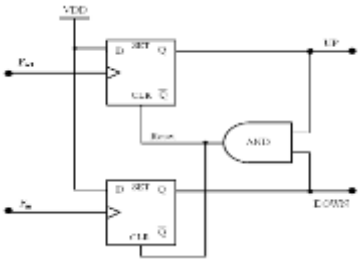

Fig.5. PFD Circuit

If there is a phase difference between the two signals, it will generate "UP" or "DOWN" synchronized signals. When the reference clock rising edge leads the feedback input clock rising edge "UP" signal goes high while keeping "DOWN" signal low. On the other hand if the feedback input clock rising edge leads the reference clock rising edge "DOWN" signal goes high and "UP" signal goes low. Fast phase and frequency acquisition PFDs [6-7] are generally preferred over traditional PFD.

B) Charge Pump and Loop Filter

Charge pump circuit is an important block of the whole PLL system. It converts the phase or frequency difference information into a voltage, used to tune the VCO. Charge pump circuit is used to combine both the outputs of the PFD and give a single output which is fed to the input of the filter. Charge pump circuit gives a constant current of value IPDI which should be insensitive to the supply voltage variation [8]. The amplitude of the current always remains same but the polarity changes which depend on the value of the "UP" and "DOWN" signal. The schematic diagram of the charge pump circuit with loop filter is shown in the Figure below

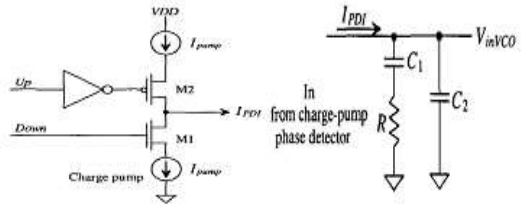

Fig.6. Charge pump circuit with loop filter

When the UP signal goes high M2 transistor turns ON while M1 is OFF and the output current is IPDI with a positive polarity. When the down signal becomes high M1 transistor turns ON while M2 is OFF and the output current is IPDI with a negative polarity. The passive low pass loop filter is used to convert back the charge pump current into the voltage. The filter should be as compact as possible [9].The output voltage of the loop filter controls the oscillation frequency of the VCO. The loop filter voltage will increase if Fref rising edge leads Fin rising edge and will decrease if Fin rising edge leads Fref rising edge. If the PLL is in locked state it maintains a constant value. Phase frequency detector

C) VCO IN PLL

Electrical oscillators are used in all kinds of electronic systems. Oscillators that will be discussed in this paper will find its application in synchronization of control logic with various analog and digital integrated circuits. Oscillatory behavior is ubiquitous in all physical systems specially in memory and mixed signal integrated circuits, in frequency and communication systems. Oscillators are the prime requirements of circuits needing time references and also to synchronize operations. An ideal oscillator would provide perfect time reference i.e. a perfect periodic signal [1], but oscillators are corrupted by undesired noise.

A variety of Oscillators are available but the principle of operation, the frequency of oscillation, their fabrication with respect to different CMOS logics relative, process technologies and their performance in noisy environment is different from one class of oscillators to other.

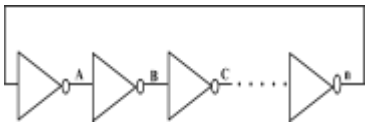

Fig.7. Ring Oscillator realization with n digital inverters

This ring oscillator is designed to be controlled in a oscillation frequency by a voltage input. The physical design of the very same will include C5 process, 300 nm process technology simultaneously various design rule checks and network consistency checks were performed. CMOS inverter ring oscillators offer numerous advantages like tuning ranges, signal swing and a small chip area.

C.1)Barkhausen Criteria

The Barkhausen criterion is used to determine the oscillation startup condition. The Barkhausen stability criterion is necessary but not sufficient for oscillation[4].

$$|H(j\omega)| \geq 1 \qquad \text{(i)}$$

$$\angle |H(j\omega)| = \pi \qquad \text{(ii)}$$

The criteria for oscillation is not well understood, there is no known sufficient criteria for oscillation. If considering the unity gain negative feedback which is as shown below, where

$$\frac{V_{out}}{V_{in}}(s) = \frac{H(s)}{1+H(s)} \qquad \text{(iii)}$$

Them the circuit may oscillate at ω if the conditions (i) and (ii) are met called the Barkhausen criterion.

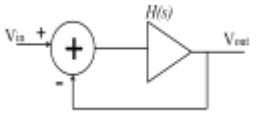

Fig.8. Generalized Feedback System[6]

D) Frequency Divider

The output of the VCO is fed back to the input of PFD through the frequency divider circuit. The frequency divider in the PLL circuit forms a closed loop. It scales down the frequency of the VCO output signal. A simple D flip flop (DFF) acts as a frequency divider circuit. The schematic of a simple DFF based divide by 2 frequency divider circuit is shown in the Figure below

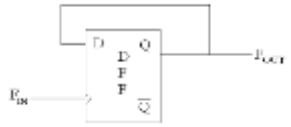

Fig.9 Schematic of a simple DFF based divide by 2 frequency divider circuit

V. PERFORMANCE COMPARISONS

TABLE 1.1

Performance Comparisons of DPLL Implementations with respect to various process technologies [1]

CMOS Process Technology	180nm	130nm	65 nm	45 nm
Core Area	0.14 mm^2	0.2 mm^2	0.07mm^2	0.07mm^2
Power	26.7 mW	16.5 mW	1.81 mW	16mW
Output Range	62-616 MHz	0.3-1.4 GHz	90-527 MHz	0.8-12 GHz
Locking Time	NA	3.5us	NA	46us
Jitter RMS	7.28ps	3.7ps	8.64ps	1.32ps

In this review[1], the proposed novel successive approximation algorithm to improve the frequency and phase locking time of BBPHD-based ADPLL without much scarification of output clock jitter. 790ns locking time demonstrates that such design is suitable for microprocessor, which needs to switch to a different frequency during dynamic frequency scaling. Although achieving fast-locking, it still needs to stall CPU during the locking process because the oscillator is reset and the frequency changes dramatically during SAR search. Therefore, future works will be to design an ADPLL that can both achieve fast locking and a smooth frequency change in DCO.

TABLE 1.2

Performance Comparisons of ADPLL[2]

Process	180 nm	180nm
Power Consumption	26.7 mW	25.02 mW
Resolution	-	2.1 ps
Jitter Performance	56 ps	32.86 ps
Frequency Range	62 MHz- 616 MHZ	400 MHz- 860 MHz

In review [2] An all-digital PLL was proposed and designed with a tristate inverter delay cell based LPI-TDC using 0.18μm CMOS process. The proposed delay-cell in LPI-TDC is exploited to obtain high performance and low power consumption. Other parts in the proposed ADPLL such as DLF and DCO are implemented to reduce jitter, and to generate a proper frequency through accurate digitized control words. The proposed ADPLL performs better than the conventional ones, and it will be a good reference for the future work.

VI. CONCLUSION

In this paper a Digital PLL clock generator design and analysis is presented. The PLL circuit consumes an optimal power respective D.C. The centre frequency of oscillation of the VCO depends upon the sizing of the transistors. The frequency deviation from the desired value can be reduced by properly choosing the transistor sizes.

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