Design, Implementation and Fast Fourier Analysis of Digital Locked loops for clock generation using C5 SCMOS

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Abstract—The most versatile application for digital phase locked loops is for clock generation and clock recovery in any complex computer architecture like a microprocessor or microcontroller, network processors. Digital Phase locked loops are commonly used to generate timing on chip clocks in high performance mixed signal analog and digital systems. Most of the systems employ digital PLL mainly for synchronization , skew and jitter optimization. Because of the need of high speed circuitry there is a need of PLL. Mostly communication, wireless systems, RF Processors operate in Gigahertz range, there is a necessity of PLL that too digital which operate in high order frequencies. Digital PLL is a mixed signal integrated circuit and presented work focuses on design and analysis of efficient digital phase locked loops for clock generation using 50nm SPICE models. The presented design Digital PLL performs the function of mainly generating a clock signal also consists of design of sub circuits and systems like phase detector, loop filters and voltage controlled oscillators. A detailed FFT analysis is also presented with parameters magnitude, phase and group delay calculated for each sub circuits and systems. The results of DPLL designed using proper optimization method is also compared with traditional method.

Index Terms — Digital PLL, SPICE, VCO, Phase Detector, FFT, Loop filters

I. INTRODUCTION

Digital Phase locked loop is a   mixed signal analog integrated circuit. Digital PLL is the heart of many communication as well as electronic systems. Mostly a higher lock PLL range with lesser locking time and should have tolerable phase noise. The most versatile application of a digital PLL is for clock generation or synchronization, clock recovery, communication systems and frequency synthesizers. In high performance digital systems like processors digital PLL or DPLL are commonly used to generate well timed on chip clock signals. Modern RF circuits or wireless   mobile communication systems use PLL for synchronization , timing based synthesis, skew and jitter reduction. Digital PLL is extensively used in advanced communication systems, electronic and medical instrumentation systems. The PLLs are an integrated part of larger circuits on a single chip.
A simple PLL consists of namely four to five integrated blocks. They are phase frequency detector, charge pump, Loop filters, voltage controlled oscillator and frequency dividing circuits.
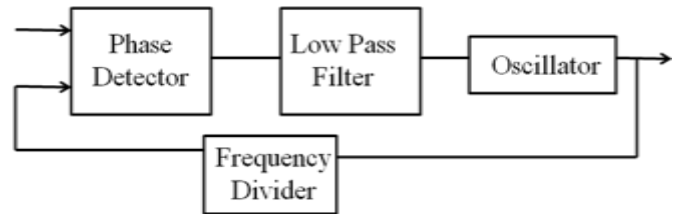

Fig.1 Basic Block diagram of a Digital Phase locked loop

Today in terms of high frequency usage in mixed signal analog integrated circuits deploy PLLs of faster locking abilities. In this paper the faster locking of PLL is particularly concentrated with respected to 50 nm process technology. The design and simulation results are based on cmos models using the same process technology. Digital PLL takes in to account suitable circuit architectures and associated parameters. The optimization of the Voltage controlled oscillator is also carried out using simple CMOS and current starved CMOS inverters to get a better frequency precision.

II. DESIGNING A DIGITAL PLL

A PLL is a closed-loop feedback system that sets fixed phase relationship between its output clock phase and the phase of a reference clock. A PLL is capable of tracking the phase hanges that falls in this bandwidth of the PLL. A PLL also multiplies a low-frequency reference clock CKref to produce a high-frequency clock CKout this is known as clock synthesis. A PLL has a negative feedback control system circuit. The main objective of a PLL is to generate a signal in which the phase is the same as the phase of a reference signal. This is achieved after many iterations of comparison of the reference and feedback signals. In this lock mode the phase of the reference and feedback signal is zero. After this, the PLL continues to compare the two signals but since they are in lock mode, the PLL output is constant. A basic PLL is a negative feedback system that receives an incoming oscillating signal and generates an output waveform that exerts the same phase,frequency relationship as the input signal. This is achieved by constantly comparing the phase of output signal to the input signal with a phase frequency detector (PFD).

The Phase frequency Detector (PFD) is one of the main parts in PLL circuits. It compares the phase and frequency difference between the reference clock and the feedback clock. Depending upon the phase and frequency deviation, it generates two output signals UP and DOWN. The Charge Pump (CP) circuit is used in the PLL to combine both the

outputs of the PFD and give a single output. The output of the CP circuit is fed to a Low Pass Filter (LPF) to generate a DC control voltage. The phase and frequency of the Voltage Controlled Oscillator (VCO) output depends on the generated DC control voltage. If the PFD generates an up signal, the error voltage at the output of LPF increases which in turn increase the VCO output signal frequency. On the contrary, if a Down signal is generated, the VCO output signal frequency decreases. The output of the VCO is then fed back to the PFD in order to recalculate the phase difference, and then we can create closed loop frequency control system.

III. PLL ARCHITECTURE

In general a PLL consists of five main blocks:
1. Phase Detector or Phase Frequency Detector (PD or PFD)
2. Charge Pump (CP)
3. Low Pass Filter (LPF)
4. Voltage Controlled Oscillator (VCO)
5. Divide by N Counter

Fig.2 A generic architecture of Digital PLL

3.1 Phase frequency Detector

The phase frequency detector is one of the main integral parts of PLL circuits. It compares the phase and frequency difference between the reference clock and feedback clock. Depending upon the phase and frequency deviation it generates two output signals Up and Down. If there is a phase difference between the two signals, it will generate UP or DOWN synchronized signals. When the reference clock rising edge leads the feedback input clock rising edge UP signal goes high while keeping "DOWN" signal low. On the other hand if the feedback input clock rising edge leads the reference clock rising edge "DOWN" signal goes high and "UP" signal goes low. Fast phase and frequency acquisition PFDs are generally preferred over traditional PFD.

Following is the basic PFD circuit designed for the presented digital PLL
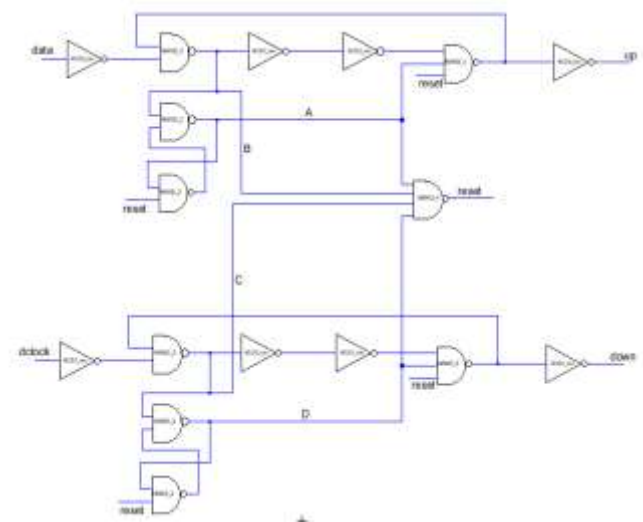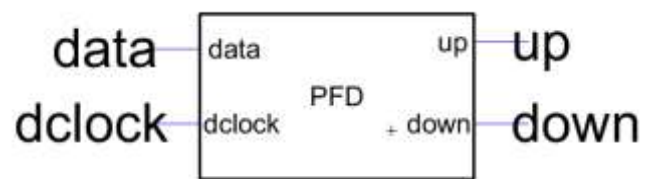

Fig. 3 Schematic Diagram for Phase frequency Detector

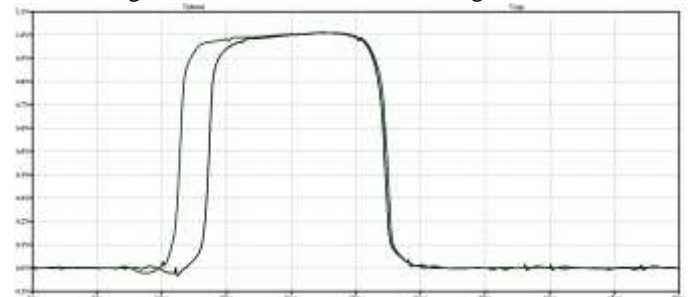Fig.4 Icon view for schematic in figure 3 PFD

Fig. 5 Simulation plot for Up and Down signals in PFD

3.2 Charge Pump and Loop Filter

Charge pump circuit is an important block of the whole PLL system.
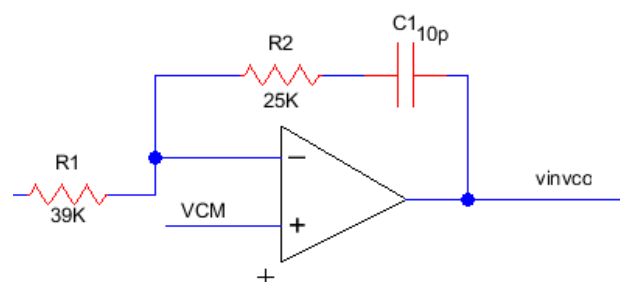

Fig. 6 Basic Charge Pump Loop Filter using Opamp

It converts the phase or frequency difference information into a voltage, used to tune the VCO. Charge pump circuit is used

to combine both the outputs of the PFD and give a single output which is fed to the input of the filter.

3.3 Voltage Controlled Oscillator
An oscillator is an autonomous system which generates a periodic output without any input.The most popular type of the VCO circuit is the current starved voltage controlled oscillator (CSVCO). Here the number of inverter stages is varied, generically used with 21 stage with simple inverter or current starved configurations
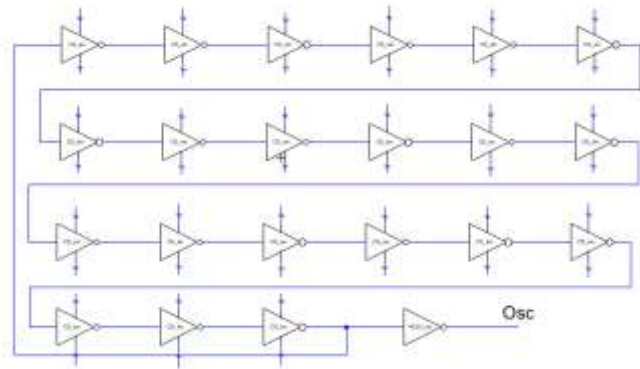

Fig.7 Schematic for 21 stage Voltage Controlled Oscillator

3.4 Frequency Divider
The output of the VCO is fed back to the input of PFD through the frequency divider circuit. The frequency divider in the PLL circuit forms a closed loop. It scales down the frequency of the VCO output signal. A simple flip flop (FF) acts as a frequency divider circuit. The schematic of a simple divider based divide by 2 frequency circuit is shown in the Figure 8

Fig.8 Schematic view for frequency divider network

IV. DESIGN AND SYNTHESIS OF DPLL

The schematic level design entry of the circuits is carried out in the Electric CAD VLSI Design Environment. The structure of the DPLL is designed in Electric CAD using 50 nm SPICE models for CMOS. In order to analyze the performances, these circuits are simulated in the LTSPICE simulator of Level 3 or 4 BSIM SPICE CAD . Different performance indices such as phase,group delay and corresponding magnitude are measured in this environment. Transient parametric sweep and phase analyses are carried out in this work to find out the performances of the circuit. The optimization of the current starved VCO circuit, the scale factor for transistor sizing is found out using the LTSpice environment.

Following Design procedure is adopted for the presented design
1. VCO Design
2. PFD Loop Design
3. Frequency Divider Circuit
4. Loop Filter and Charge Pump Design
5. Assembling all subunits in a single design
6. Carry out transient analysis
7. FFT analysis
8. Tabulation for simulation parameters
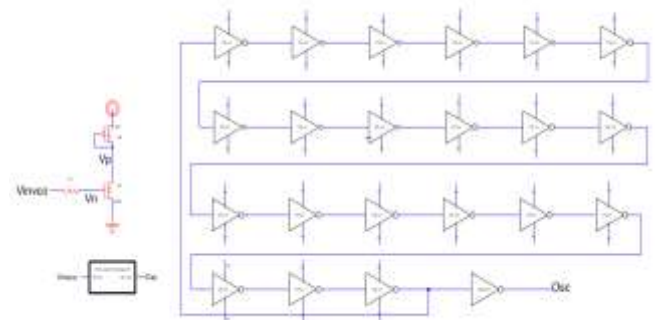
V. SIMULATION RESULTS

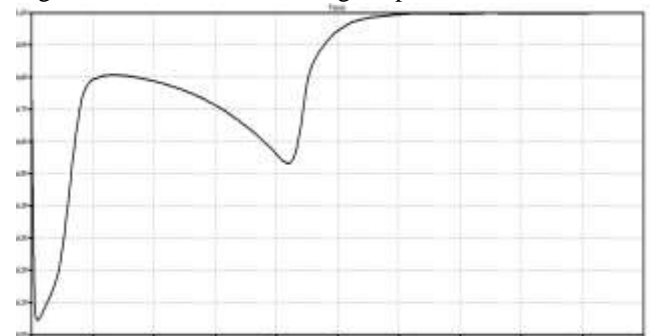Fig.8 Schematic for VCO using simple CMOS inverter

Fig.9 Transient plot for VCO using simple inverter
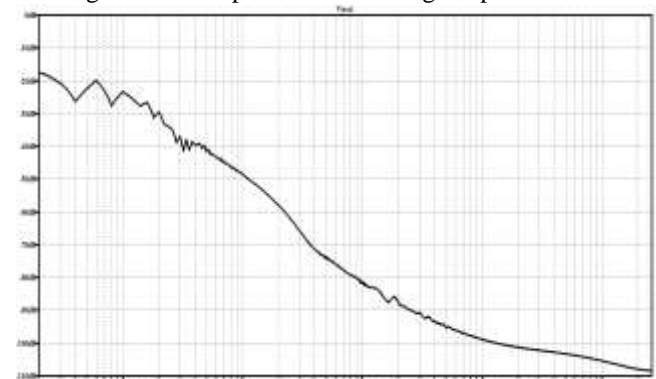

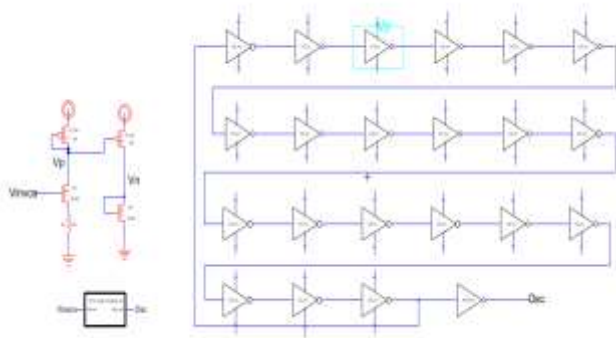Fig.10 FFT plot for VCO using simple inverter

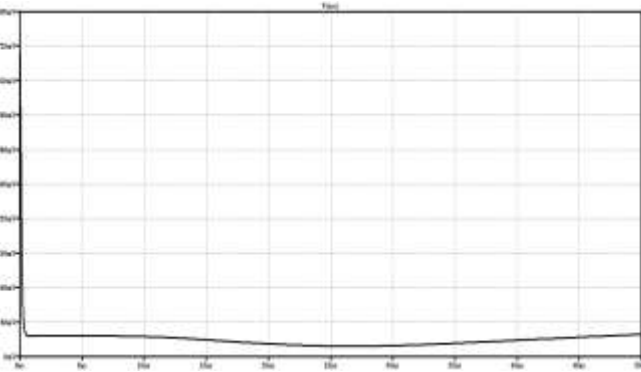Fig.11 Schematic for VCO using current starved CMOS inverter

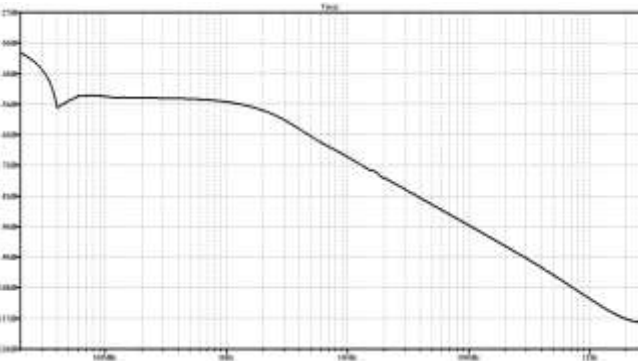Fig.12 Transient plot for VCO using current starved CMOS inverter

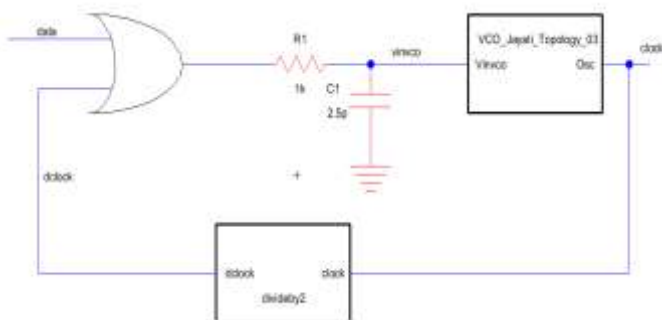Fig.13 FFT plot for VCO using current starved CMOS inverter

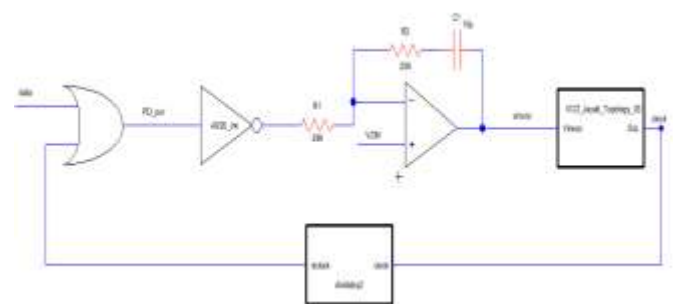Fig.14 DPLL topology 1 using RC as loop filter and Charge pump
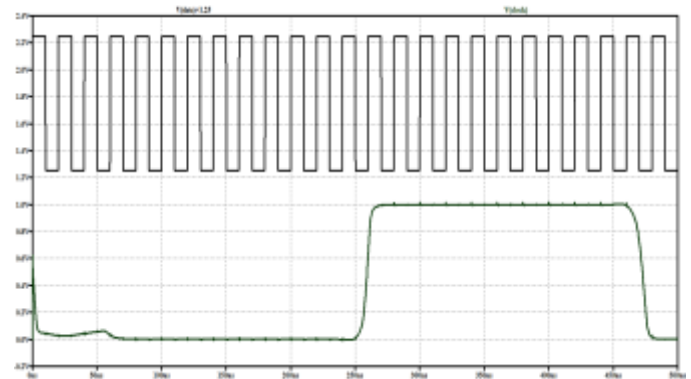

Fig. 15 Transient plot for Vdata and Vclock for DPLL topology1
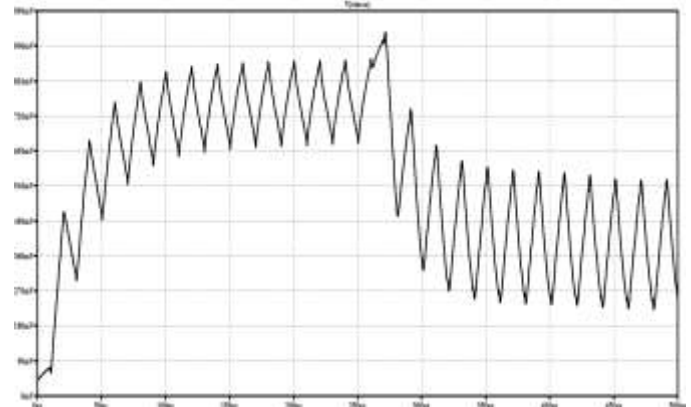

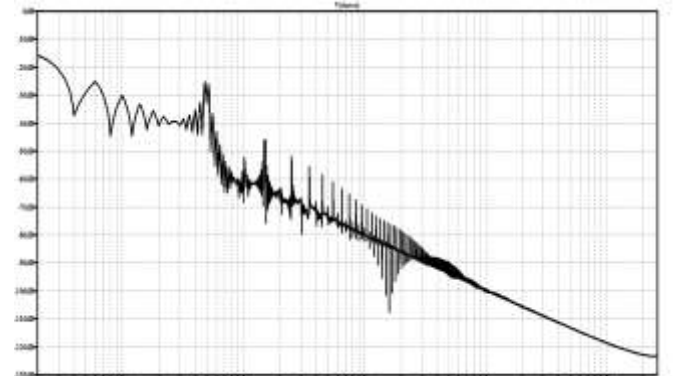Fig.16 Transient plot for oscillator output DPLL topology 1

Fig.17 FFT plot for oscillator output DPLL Topology 1

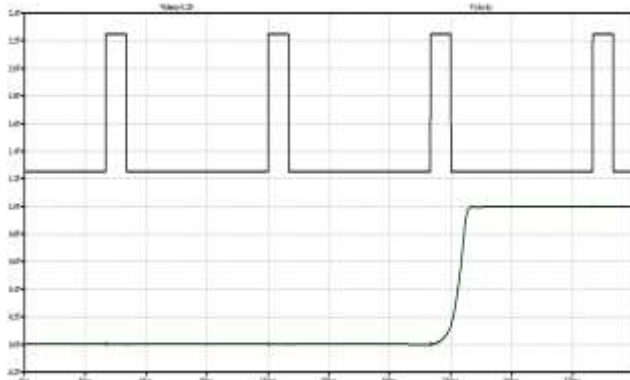Fig.18 DPLL topology 2 using Opamp as loop filter and Charge pump

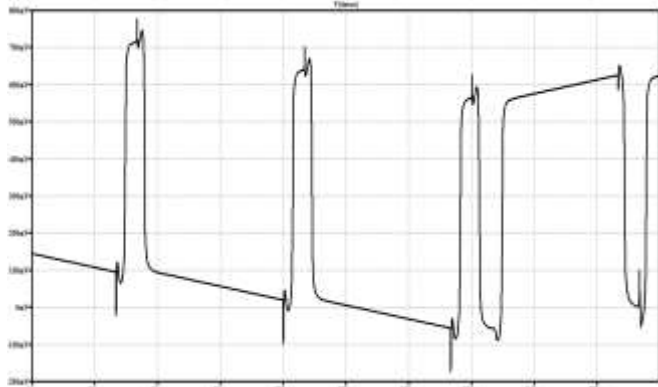Fig.19 Transient plot for Vdata and Vclock in
DPLL topology 2

Fig. 20 Transient plot for Oscillator output DPLL topology 2
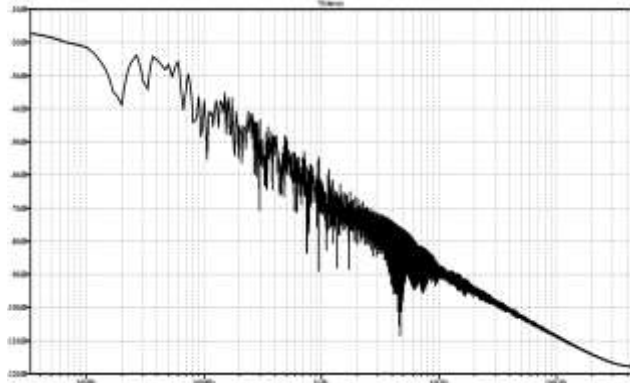

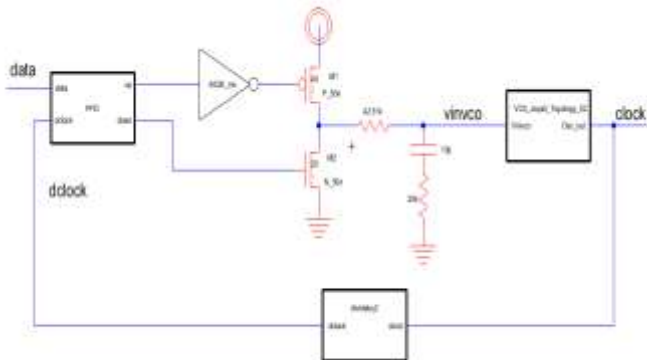Fig.21 FFT Plot for Oscillator output DPLL topology 2

Fig.22 DPLL topology 3 using Opamp PFD and RC loop
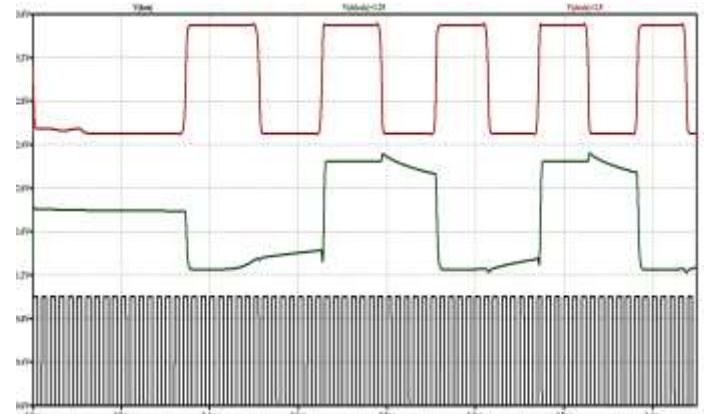filter and Charge pump

Fig. 23 Transient plot for Vdata and Vclock in
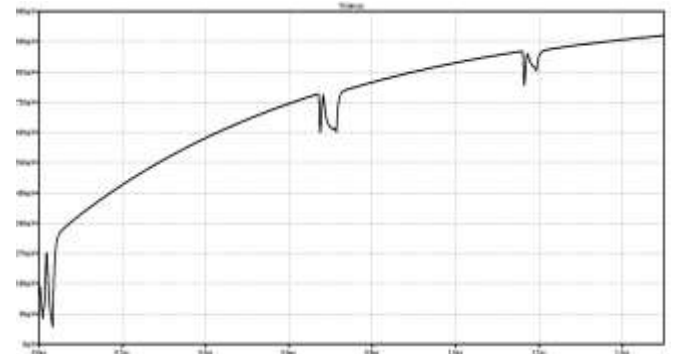DPLL topology 3

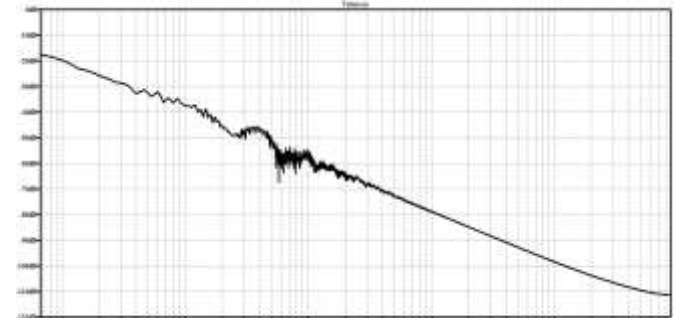Fig.24 Transient plot for Oscillator output
in DPLL topology 3
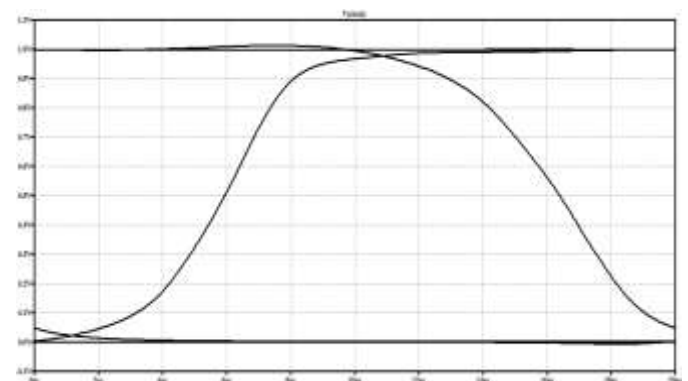

Fig. 25FFT Plot for Oscillator output DPLL topology 2

Fig.26 Transient Plot or Eye Diagram for Vclock in
DPLL Topology 3

VI. FFT RESULTS

Table 1
FFT analysis for DPLL Topology 1

Frequency	Magnitude	Phase	Group Delay
1MHz	-15.61 dB	158.17°	45.25 ns
10 MHz	-36.76 dB	96.91 °	-25.45 ns
100 MHz	-45.09 dB	94.21°	85.44 ns
1 GHz	-66.73 dB	98.16 °	550.24 ns
10 GHz	-76.53 dB	111.66 °	148.57 ps
100 GHz	-511.58 dB	126.58 °	12.33 ps

Table 2
FFT analysis for DPLL Topology 2

Frequency	Magnitude	Phase	Group Delay
1MHz	-27.26 dB	33.9°	-135.37 ns
10 MHz	-31.528 dB	-142.89 °	75.07 ns
100 MHz	-35.77dB	74.83°	-34.17 ns
1 GHz	-68.43 dB	14.72°	-304.721 ns
10 GHz	-86.74dB	52.15°	-10.594ns
100 GHz	-118.80dB	81.30°	52.79ps

Table 3
FFT analysis for DPLL Topology 3

Frequency	Magnitude	Phase	Group Delay
1MHz	-29.82 dB	19.74°	17.85 ns
10 MHz	-37.42 dB	14.85°	48.54 ns
100 MHz	-66.21 dB	90.41°	-36.17 ns
1 GHz	-98.79 dB	96.68°	-30.14 ns
10 GHz	-98.53 dB	15.14°	-88.45ns
100 GHz	-110.30 dB	18.99 °	-30.620 ns

VII. CONCLUSION

In this paper presented DPLL works with better locking times, the digital PLL consumes low power as designed with 50 nm CMOS technology, the transient analysis mainly depends on the type of the PFD architecture used and parasitic parameters utilized for charge pumps and loop filters. So by properly choosing VCO architecture, PFD design and adjusting the charge pump configurations. The efficiency of the overall design also depends on the reduction of transistor sizes which is 50nm.

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