DEDICATED SHORT RANGE COMMUNICATION TECHNIQUES

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Abstract-- **DSRC if implemented efficiently in India reduces the risks of vehicle accidents due to mismanagement of traffic and delays due to traffic congestion by a large amount. The DSRC protocols generally adopt FM0 and; Manchester; codes to enhance the signal reliability and achieve dc-balance. The disadvantages of using the conventional FM0 and Manchester techniques individually is that area utilization is less as compared to the similarity-oriented logic simplification (SOLS) technique. SOLS technique combines the FM0 and Manchester encoding techniques to overcome these disadvantages and implement DSRC.Another disadvantage that we face with FM0 and Manchester is that the output that we get is unbalanced dc logic in comparison to a balanced DC logic with SOLS that is easier to implement. In this project we have implemented all the basic elements of SOLS, FM0, and Manchester & SOLS circuitry using Verilog Xilinx in order to understand basic functionality of these blocks. Further, we have implemented the SOLS technique in Orcad PSpice using Resistor Transistor Logic (RTL), Domino Logic, Transmission Gate, Transistor Transistor Logic (TTL) and CMOS logic.**

Keywords—**Intelligent transportation system**

I. INTRODUCTION

A technology that allows us to design vehicles in the intelligent transportation system to interact with other vehicles and surrounding infrastructure technology wirelessly. Dedicated Short Range Communication or commonly known as DSRC is based on IEEE802.11p standard. FCC has authorized 75MHz of spectrum (5.5850-5.925 GHz) for DSRC which is basically a short to medium range communication service. It was aimed as a replacement to the 802.11 wireless standards. Data can be transmitted in a broadcast; mode wherein, 300m is the LOS range distance. Peer-to-peer vehicle data; exchanges take place in this technology. DSRC is engineered to ;work correctly in traversing; vehicle surroundings. The vehicle and surrounding infrastructure transmit different types of messages as explained below in order to communicate under DSRC.BSM and PVD messages are transmitted by the vehicle and are thus used in the Vehicle to vehicle environment (V2V). The Basic Safety Message (BSM) has an average message size of 320 bytes. The default transmission rate of BSM is 10 Hz. BSM is responsible for various V2V applications to take place. Traveller Information Message (TIM), Map Data Message (MAP) and Signal Phase and Timing (SpaT) are the message types that exist in the V2I communication that is the infrastructure to vehicle transmission. TIM provides the timing information ahead wherein it tells about any possible accident or traffic queue to be encountered in the route to be travelled by the vehicle. MAP will have the coordinates of the road especially the cross-section and intersection of the roads to be provided to the vehicle. The unique benefits of DSRC communication include a dedicated 75 MHz of spectrum at 5.9 GHz which consists of 7 listed channels. Low latency in communication that gives quite less than 50 MS delay. High data transfer rates of 3-27 Mbps and low power message reception that is less than -90dBm are other benefits of DSRC communication. The DSRC spectrum along with its channel divisions and respective applications has been shown below in fig.1

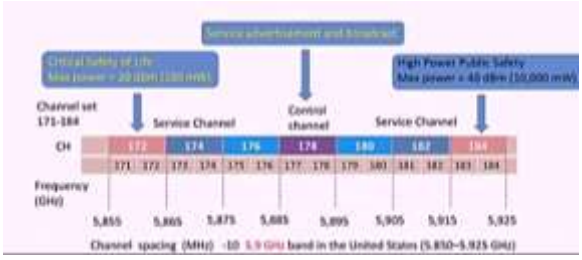

Fig. 1 DSRC Spectrum

DSRC spectrum is about 75MHz and there are 7 channels which are 10MHz each.Channel 172 is used for basic safety message changes. The maximum power is 20dbm and is reserved for critical safety of life,Channel 184 is used for high power public safety. RSE use that channel and will be able to

communicate for longer and cover more vehicles. Channel 174 and 182 are service channels. The channel 178 is control channel. They are used for both private and public safety. The control channel is used for service advertisement and broadcast. Bothe the service and control channels share the same structure.

The DSRC architecture is shown below in figure 2. It consists of the GPS antenna that is present on the vehicle that transmits the messages which is received by the DSRC antenna and then transmitted to the main computing system which also receives information from the internal sensors of the vehicle and the surrounding infrastructure to decide on the further message to be transmitted to other vehicles' driver interface.

Fig. 2 DSRC Architecture

II BACKGROUND

A. *The SOLS Techniques*

DSRC-encoders makes use of FM0 and the Manchester encoding together. So to form a reusable encoder, both these-encoders can be combined together. Furthermore, the circuit architecture-can also be abridged by means of the SOLS methodology. For the SOLS technique, two methods are chosen: the balance logic simplification and area compact retiming.

Primarily, to simplify the FM0 encoder-this method is used. The state-code of each state A(t) and B(t) is stored into discrete flip flops for FM0 encoder. Since-the state code transition is merely depends on B(t), the encoder-only needs a lone bit flip flop. Hence the-block diagram is rearranged as shown:

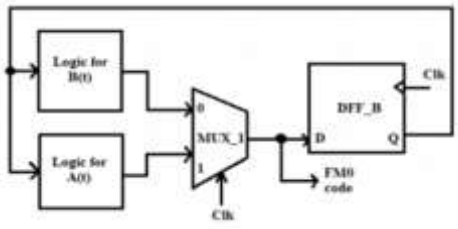

Fig.3 area compact retiming

B. *Manchester encoding*

Manchester code is a line code. In this code, each data bit is encoded high then low or low then high, for equivalent times. It is also known-as phase encoding code (or PE). It is used in telecommunication-and data storage. It is applied by the physical-layer of the Open System Interconnection, i.e. OSI to encode the-data and clock of a synchronous bit stream. Manchester coding is a self-clocking signal with no-DC component. Electrical networks making use of this code are simply galvanically-isolated due to this feature. Manchester encoding is a data-modulation technique which-can be applied in many applications. It is extremely helpful in binary-data transfer based on analog, RF, optical, high-speed-digital, or long-distance-digital signals. The basic idea which led to Manchester encoding-is that- we can use voltage transitions, instead of voltage levels, -to represent ones and zeros. Manchester encoding is a-synchronous clock-encoding technique.

C. *FM0 encoding*

The encoding which-is a type of NRZ code is FM0 encoding. This-encoding is applied to characterise the binary waveforms in a digital system. In FM0-encoding, the encoded signal familiarities a transition for each clock cycle although the data stream doesn't meet transition. FM0 encoding is also-called as Biphase space encoding. The FM0-encoding contains the following three rules:

1. If input data X is the logic-0, the-FM0 code must demonstrate a transition between former half cycle of CLK and later half cycle of CLK, i.e. for-every logic zero input there should be transition within a clock cycle.
2. If X is the logic-1, no transition is-permitted between half cycles of CLK, i.e. For logic one input there should be no transition.
3. The transition billed among each-FM0 code, no affair what the X is, i.e. afterward each clock cycle regardless of the input data there must be a transition.The-FM0 encoding can be realized by the use of multiplexers and of two flip-flops. As-shown in the block-diagram, the FM0 encoding can be realised. A(t) and B(t) specify the two states.

D. *Dflipflop*

The basic D flip flop has a data input and a clock input. It has outputs Q and Q' (inverse of Q). Occasionally it may include CLR' (Clear) and PR' (Preset) control inputs. The D Flip Flop is also called a Delay Flip Flop as it can be use to introduce a delay in the circuit, this is done so by changing the propagation delay of the flip flop.

TABLE I
TRUTH TABLE OF DFLIPFLOP

TRUTH TABLE

INPUTS				OUTPUTS	
PR	CLR	CLK	D	Q	Q̄
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	X	X
1	1	↑	1	1	0
1	1	↑	0	0	1
1	1	0	X	Q_n	$\bar{Q}_n$

input data must be stable for a period before and after the rising edge of the clock. Specifically, the data must have reached its correct value at least a setup time ts before the clock reaches its 50% point, and the data must be held stable at this value until a hold time the after the clock has reached its 50% point. However, it must remain stable with the input value during the setup- and hold-intervals for the flip-flop to sample the input value correctly.

If the input meets its setup- and hold-time constraints, the flip-flop will update the output with the sampled value x. The previously stored value, which was sampled on the previous clock edge, will remain stable on the output until a contamination delay tcCQ after the rising edge of the clock. At a propagation delay tdCQ after the rising edge of the clock, the output is guaranteed to have the value x sampled from the hold this value stable until tcCQ after the next rising edge of the clock.

E. T-FLIP FLOP

The T (toggle) flip-flop is a complementing flip-flop and can be obtained from a JK flip-flop when inputs J and K are tied together. T flip-flop is used to define only toggle and no change conditions. When T=0 (J= K =0), a clock edge does not changethe output. When T=1 (J= K= 1), a clock edge complements the output. A T Flip Flop may be contructed using a D Flip- Flop and an XOR gate.When T = 0, D = 0 and there is no change in the output. When T = 1. D=Q' and the output complements.

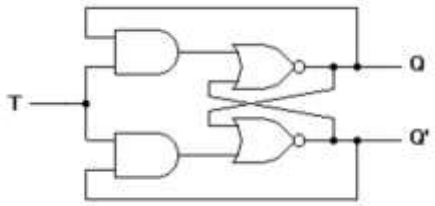

Fig 4. Logic diagram

TABLE II
TRUH TABLE OF T-FLIP FLOP

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

III. IMPLIMENTATION

A. SOLS TECHNIQUES

The figure given below illustrates the hardware architecture and the waveform of the FM0/Manchester encoder implemented using the SOLS technique which itself has the advantages of providing the 100% area utilization and output waveform of the balanced logic which are easier to implement with electronic circuitry.

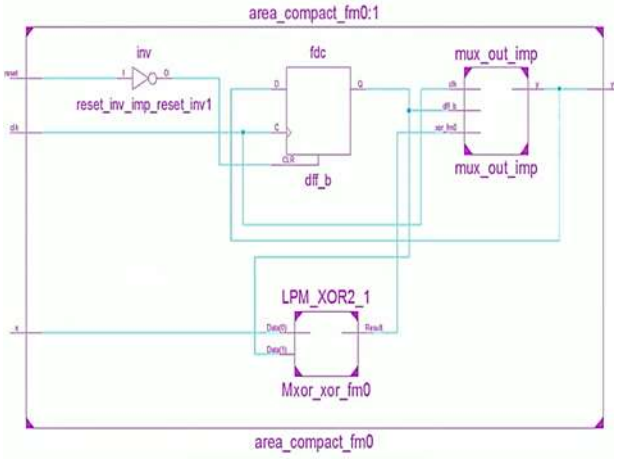

Fig.5 Verilog Implementation of SOLS technique depicting area compactness

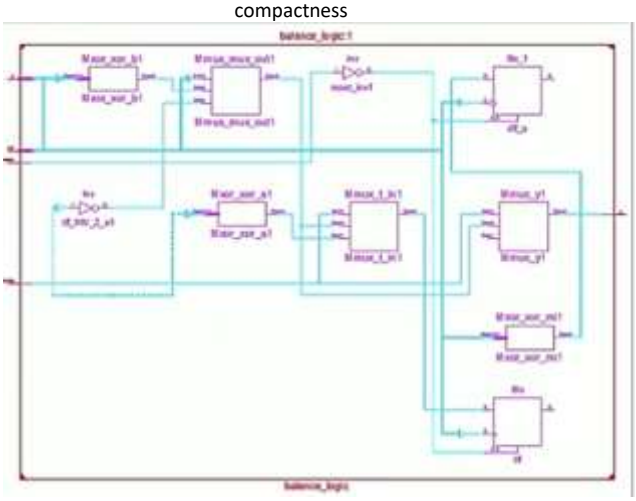

Fig.6 Verilog Implementation of SOLS technique depicting balance logic

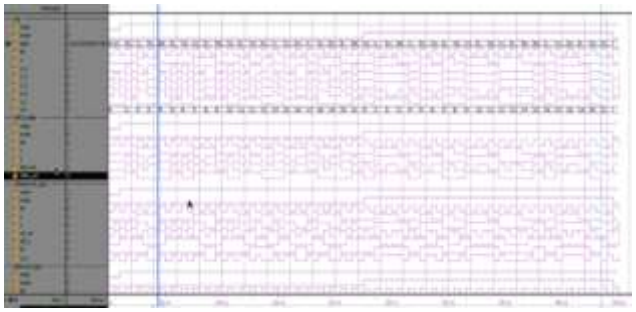

Fig7. Output waveform for Tflipflop

B. SOLS USING TTL

The following figure shows the hardware implementation of the Sols circuit using TT`L logic family and its output waveform which is then used to find out the propagation delay of the circuit and its power consumption and hence the figure of merit

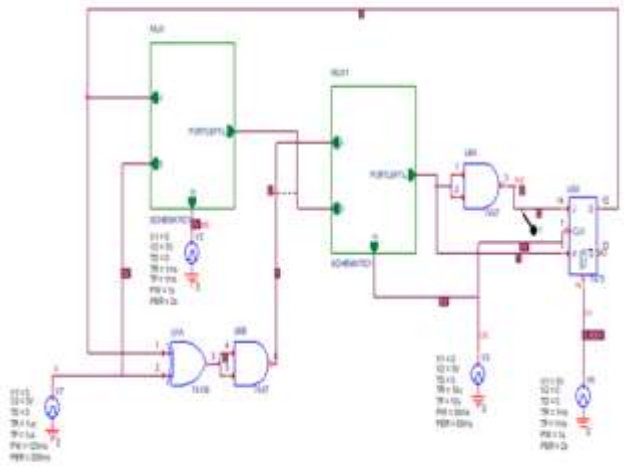

Fig.8 Implementation of Sols using TTL logic

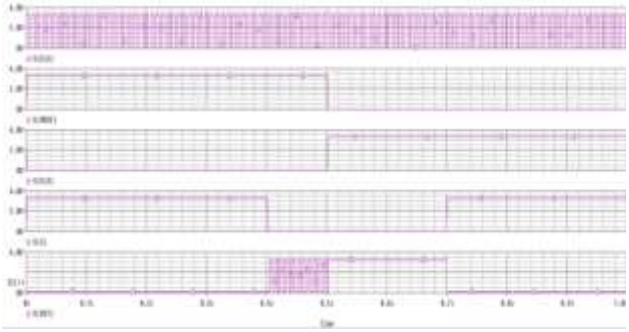

Fig.9 Output waveform

C. SOLS USING CMOS

CMOS stands for complementary metal-oxide-semiconductor. This technology is generally used for creating digital circuits. The basic elements of CMOS circuits are PMOS and NMOS transistors. A PMOS could be used as a switch which is closed if the input voltage is low (0 V) and open if the input voltage is high (5 V). An NMOS could be used as a switch that is closed if the input voltage is high (5 V) and open if the input voltage is low (0 V). The basic idea behind CMOS technology is to use both PMOS and NMOS such that there is never a path which conducts from the supply voltage (5 V) to ground. Consequently, CMOS circuits use very less energy. CMOS technology uses two types of transistor namely n-channel and p-channel. Both of them differ in the characteristic features of the semiconductor materials used in their operation and in the phenomenon controlling the conduction of a current through them. We will use this behaviour making use of switches which are controlled by voltages associated to logic 0 and logic 1. This kind of a model ignores complicated electronic devices and only captures logical behaviour.

The following figures shows the hardware implementation of the sols circuit using CMOS logic family and its waveform from which it can be concluded that it has least power consumption but then we have to compromise with the speed of operation

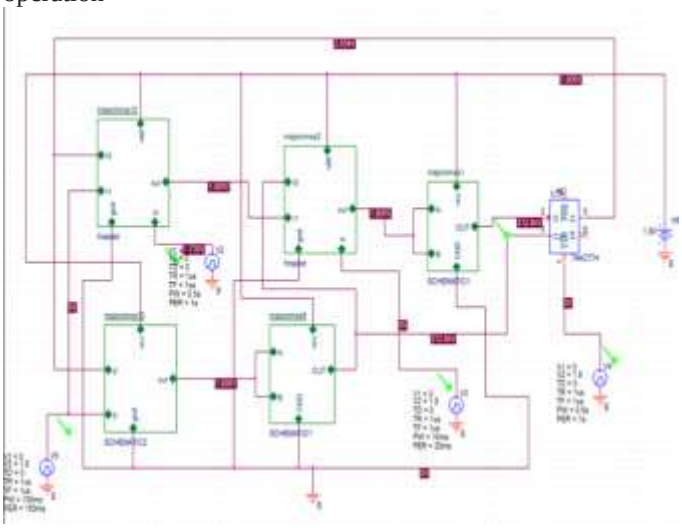

Fig.10 Implementation of Sols using CMOS logic

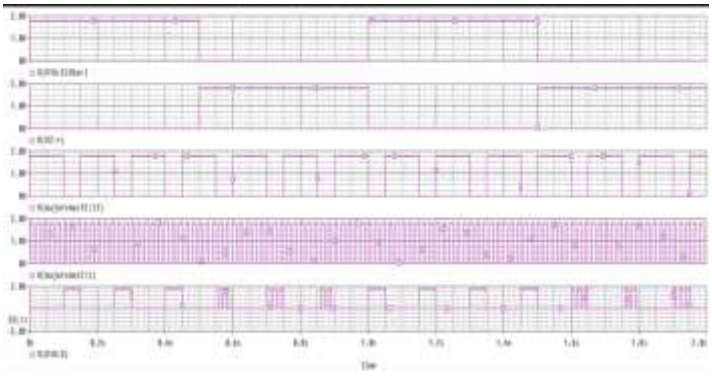

Fig.11 Output waveform

D. SOLS USING RTL

Resistor–transistor logic (RTL) is made up of resistors and bipolar junction transistors (BJTs). The resistors are the input network and the BJT is used as the switching device. RTL is also known as Transistor-Resistor Logic, i.e. TRL. It is an outdated technology which is used for the fabrication and deign of circuits that are digital in nature and those that use logic gates which consist only resistors and

transistors. RTL circuits are not very commonly used now and if used, only in digital electronics design due to its several limitations like poor noise margin, limited fan-out, low speed and bulkiness. It is one of the oldest digital circuit used which is built using transistors. The other classes to use the same are transistor–transistor logic (TTL) and diode–transistor logic (DTL). RTL logic family's basic circuit of NOR.

The following figures shows the implementation of the Sols circuit using RTL logic family and its output waveform (advantage is that minimum amount of hardware is used so very beneficial for the discrete component designing)

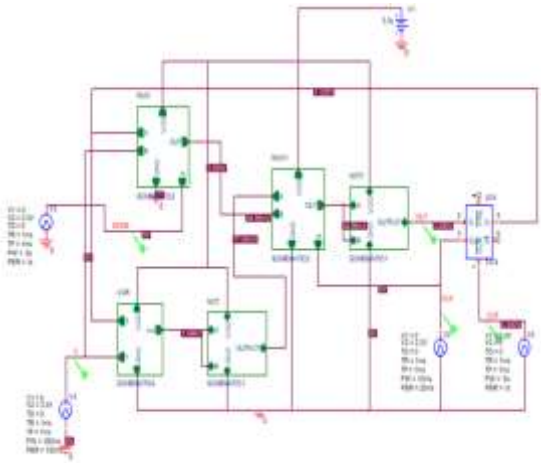

Fig.12 Implementation of Sols using RTL logic

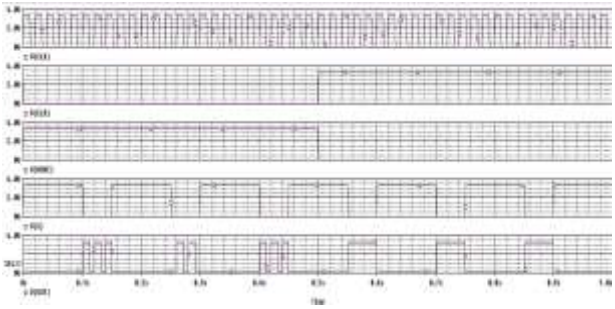

Fig13.Output waveform

E. SOLS USING DOMINO LOGIC

In static CMOS, static outputs are connected always to either the supply or the gnd as the name suggests. Through the circuit, the static current is zero. The number of MOS required will go higher if we increase the number of inputs in static CMOS.Whereas in dynamic CMOS, the output is taken across a capacitor. The output is not always connected to a supply or a gnd. The main issue in dynamic CMOS is the charge loss on capacitor. It needs a refresh timely to store the charge on capacitor. In IC design, dynamic logic is a design technique in combinatory digital logic circuits, mainly those realised in MOS technology. It is differentiated from the so-called static logic by take advantage of brief storage of information in gate and stray capacitances. Dynamic Logic is also sometimes called as clocked logic. Dynamic logic reduces the number of transistors and at the same time, keeps a check on the static power consumption.

The following figures shows the implementation of the Sols circuit using Domino logic family and its output waveform

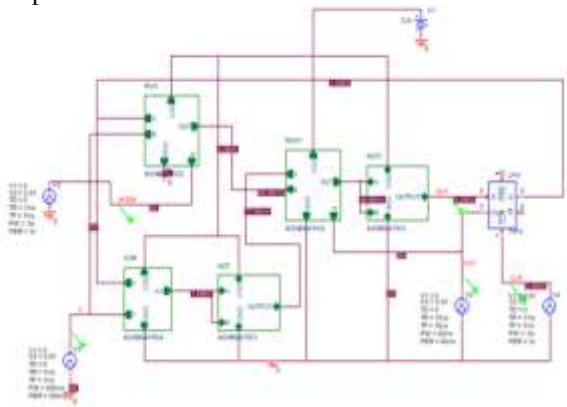

Fig.14 Implementation of Sols using Domino Logic

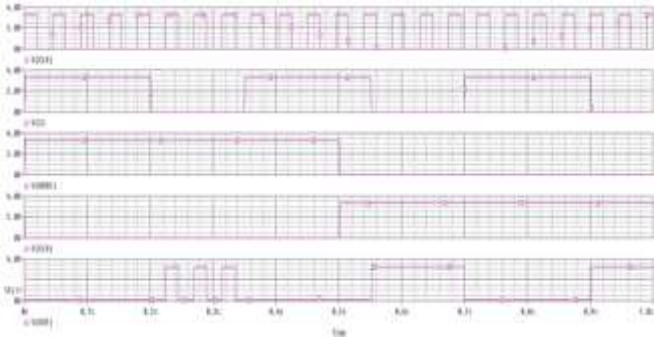

Fig.15. Output waveform

F. SOLS USING TRANSMISSION GATE

A transmission gate, or an analog switch, is an electronic element that selectively blocks or passes a waveform from its input to its output. This solid-state switch comprises of an nMOS transistor and a pMOS transistor. The control gates biasing is in such a complementary manner that both the transistors are either in an off state or an on state.

When the voltage on the input is a high, the opposite voltage low is applied to the node active-low A, letting both the transistors to pass and conduct the pulse from node IN to node OUT. If the voltage on active low input is high and voltage on active high input is low, both the transistors are off leading to high impedance state which signifies the "third state".

Transmission gates are characteristically applied as basic blocks of logic circuits, such as a D FF or D Latch. A transmission gate can also separate a component or components from live signals during removal or hot insertion. They can selectively stop acute signals or data from being communicated without appropriate hardware-controlled permission in a security application. A transmission gate (TG) is comparable to a relay which can conduct in both directions and block by using a control signal with nearly any voltage potential. Transmission Gate is a CMOS-based switch, wherein PMOS permits a strong 1 and poor 0, and NMOS permits a strong 0 and poor 1. The PMOS and NMOS both work simultaneously.

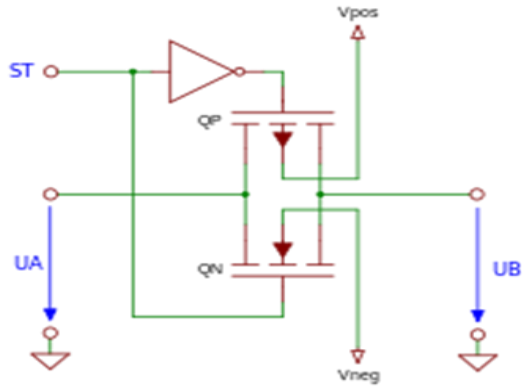

Fig16. Structure of Transmission Gate

The functioning that we observe of a transmission gate is explained below.

Once the control input is a logic low, the gate of the nMOS is at low potential and the gate of pMOS is at high potential. Irrespective on which terminal of the TG (A or B) a voltage is applied, the gate-source potential of the nMOS is permanently negative, and the pMOS is permanently positive. Thus, TG will turn off.

Once the control input is a logic high, the gate of the nMOS is at high potential and the gate of pMOS is at low potential. As the body terminal is not connected to the source, the drain and source terminals are nearly identical and the transistors start at a potential difference amid the gate terminal and thus, one of these conducts.

One of the switching terminals of the TG is raised up to a potential nearby the negative supply potential, a positive gate source potential, i.e. gate to drain potential would occur at the NMOS, and the transistor initiates to conduct, and the TG conducts. The potential at one of the switching terminals of the TG is now elevated continuously up to the positive supply voltage, therefore the gate source potential is lessened on the nMOS, and this initiates to turn off. At a similar time, the pMOS has a negative gate source potential and the gate to drain potential builds up, whereby the transistor begins to conduct and the TG switches.

Thus it is realised that the TG passes over the full potential range. The transition resistance of the TG differs depending upon the potential to be switched, and resembles to a superposition of resistance curves of both transistors.

IV. CONCLUSION

In this project, the circuit for DSRC using SOLS technique were studied & was implemented using different logic families to observe the variations in the output power consumption, propagation delay and the operating temperature range.Each logic family has its own advantages over the other as they are used for their specific applications. We observed the outputs of our simulations to find out which implementation of technology fit in which situation as desired by the communication networks. Our observations lead to the following results:

TABLE III
OBSERVATION

LOGIC FAMILY	PROPAGATION DELAY(ns)	POWER CONSUMPTION (mW)	FIGURE OF MERIT (pJ)	OPERTING TEMERATURE RANGE(C)
TTL(Transistor Transistor Logic)	10	10	100	80
RTL(Resistor Transistor Logic)	12	12	144	70
CMOS Logic Family	70	0.025-1.01	70	-55 to 125
TRANSMISSION GATE	38	2.4	91.2	-55 to 125
DOMINO LOGIC	50	0.025-1.01	50	-55 to 125

If the speed of the device is our major concern with better noise immunity in the communication then ECl logic family is supposed to be used. But this has its own limitations as it requires high power consumption therefore it's very costly. For the military grade applications where the operating temperature ranges are very high and conditions are also harsh then in those cases domino logic has to be used as it has higher operating temperature range apart from having the high noise immunity. It also gives the utility of having a low power consumption level.But if we have a power limited channel where power consumption is of the utmost importance then in those cases CMOS logic family is to be used. But in that case we have to compromise with the speed of operation due to its higher propagation delay.

TTL logic family is used because of its simplicity of design and easily available ICs which can easily be interfaced with the other ICs. It also has one of the

smallest amount of propagation delays among other families.

V. ACKNOWLEDGMENT

This work was supported in part by International Journal of Research and Technology

VI. REFERENCES

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