Optimization of transients and FFT of SCMOS Memory Sense Amplifiers for DRAM using 300nm

Sarvesh Tripathi[#1], Dr. Neetesh Raghuwanshi[#2], Dr. Bharti Chourasia[#3]
Research Scholar, Assistant Professor, Professor
Department of Electronics and Communication Engineering,
Sarvepalli Radhakrishnan University,
Bhopal, Madhya Pradesh,
India

Abstract— **This paper presents incorporates reference designs of Sense amplifiers and detailed FFT output plots in terms of amplitude or magnitude, phase and delay for scalable CMOS sense amplifiers using 300nm VLSI technology for scalable MOSFET transistor. Sensing defined as determination and detection of data contents in a particular or directed memory cell or binary bit . Sense amplifier circuits are used parallely with semiconductor memories namely DRAM SRAM and are main elements in defining the price, power and most importantly evaluation or appraisal of scalable CMOS semiconductor circuits or memories. The presented circuit topologies in this paper are made by using 0.3µm library model process technology using BSIM4 SPICE models. The presented paper also incorporates circuits operational descriptions, timing analysis, plots of FFT, also tabulation of amplitude, phase, and delay is done at range frequency range from few MHz to 10 THz. Here a layout view or backend design and connection logic for DRAM arrays to SCMOS Sense circuits amplifiers. DRC and NCC checks are also performed on the same.**

Keywords— **Sense Amplifiers, DRAM, FFT, CMOS memories, Bitlines, wordlines**

INTRODUCTION

Sense amplifiers in association with memory cells are key elements in defining the performance and environmental tolerance of CMOS memories. Because of their great importance in memory designs sense amplifiers became a very large circuit class. In the design of the sense amplifier the operation margins are of fundamental importance and these in combination with the requirements for speed power and reliability determine the complexity and layout area of the sense circuit. In the sense circuit, which influence the internal operation which include the following

(a) Power Supply voltage
(b) Threshold supply or boundary voltage drops
(c) Currents mostly leakage
(d) Charge Couplers
(e) Imbalances in supply or reference voltages
(f) Variations in the Precharge Levels
(g) Other second order effects

Sensing definition wise is the identification and finding out values of of data contents of corresponding cells in memory. [2]. Sensing shall be destructive and nondestructive , also is mostly dependent on close or open book architectural design of scalable CMOS memory cells are being in layout form . The meaningful data contents of the corresponding memory cells may be not represented properly or not changed. Dynamic RAMs, Static RAMs, EPROMs, EEPROMs etc uses non-destructive sensing and Dynamic RAMs uses destructive sensing.

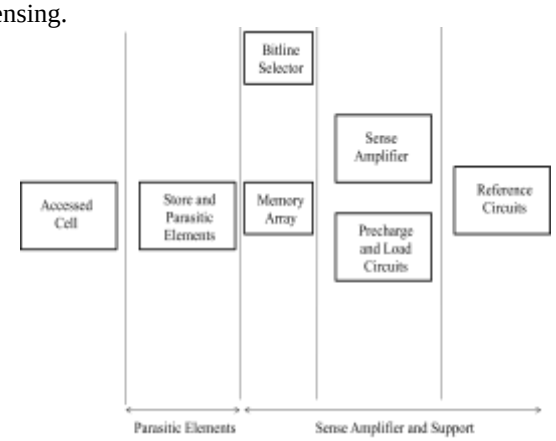

Figure 1 Sensing Amplifier Circuit Topology 1[2]

Sensing circuits mostly consisting of sense amplifiers, precharge, references and load lines, Bitlines decoupler, an accessed memory cells and other required memory control circuits.

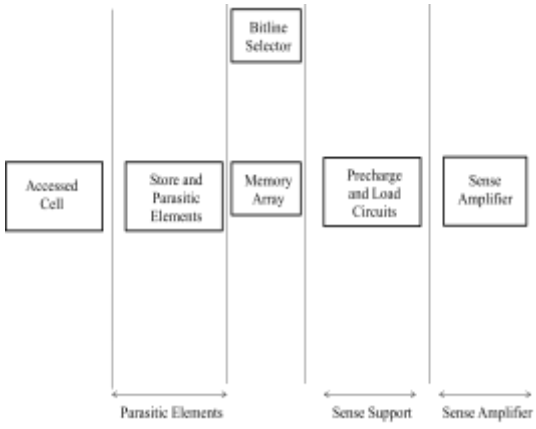

Figure 2 Sense Amplifier Circuit Topology 2[2]

Moreover though the variations of the above, the function margins are also the function of parameter ups and downs caused by

(a) Semiconductor Process Tech
(b) Variations of the Temperature
(c) Voltage input and sourcing conditions
(d) Others second order conditions for VLSI circuits

A sensing amplifier is a circuitry that decreases the duration of the signal travel from an accessing part of the semiconductor cell of the memory to the equivalent value logic circuit placed at the nearby memory cell array and converts the desired input output logic levels coming to or on the bitline to the digital peripheral logic levels of the mapping to Boolean equivalents. The sense circuit amplifier has to function inside the circumstances that are situated around operating margins.

The control circuits in the semiconductor memory are parasitics elements coupled to array bit lines generate collective Z i.e. impedance which significantly effects the function of static and dynamic RAMs.

These memory control circuits signalling had a long delay and related timing signalling also gives incomplete magnitudes to constrain the logic levels in the semiconductor memory. Sense circuit amplifiers are mostly used to develop and supply signals which authenticate the requirements of driving peripheral memory circuitries. The given front end design or schematics for sense circuit amplifier will check for two output numbers or values and further giving a larger value and corresponding sensing is carried out by clocking the sense circuit amplifier. [2, 6]

SENSING CIRCUITS OR SENSING AMPLIFIER DESIGN

Design sense amplifiers and its interfaces was one the tedious tasks in scalable CMOS design. Essential conclusions that defines the internal operational margin of the sense amplifier circuit ,Scalable MOS in the "0" low or "1" high .Operational margin of a sense amplifier circuit considers the worst possible cases operational levels, the named terminology related to voltage are listed or obtained as follows:

- Voltage supply
- Threshold Voltages or Drops
- Leakage Currents in Design
- Charge Couplings
- Imbalances in circuits
- Variations in Precharge Levels

PROJECT CONSIDERATIONS &METHODS

Frontend schematics design considerations and related methods are very much important to implement designs and sense amplifier topologies or dynamic memory sense amplifier circuits. Their design mostly of circuits changes by the corresponding count of scalable components used and sensing circuits implemented with NMOS, or with CMOS sensing circuits, smallest bit cell parasitics wordline and bitline connections.

Below Figure 3 shows ideal design guidelines or paths that has been followed for the projects related to CMOS Sense amplifier or Memory circuits

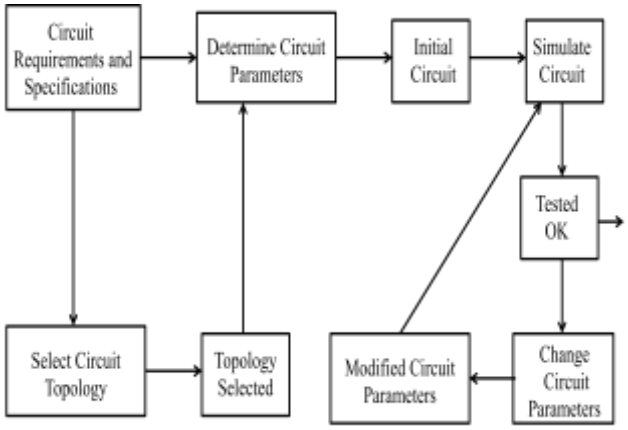

Figure 3 Guideline adopted for designing circuit topologies of sensing amplifiers

Firstly memory circuits are put up using std cells, parasitics are decided, the VLSI library here 0.3 micrometer is selected

SCHEMATICS FOR SIMULATION & FFT DATA OBTAINED

Following Sense amplifier topologies are designed using Electric CAD 9.07 and are simulated using LTSPICE XVII.[3]

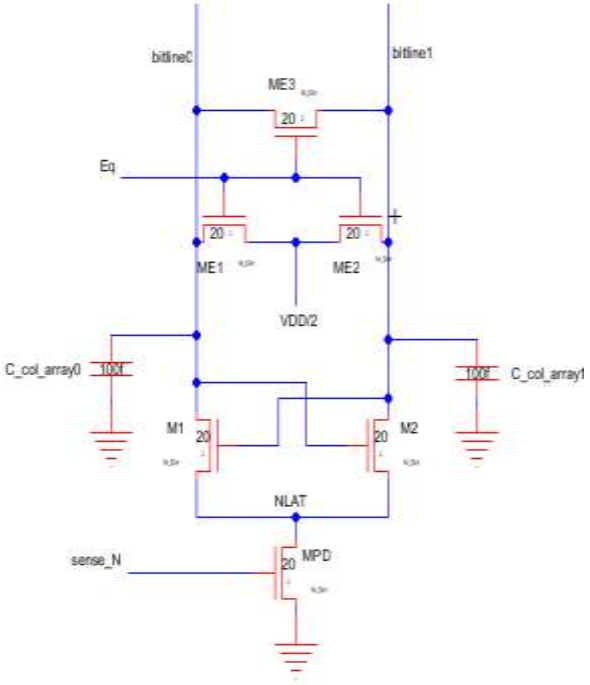

Figure 4 Sense amplifier circuit design topology type – 1 schematic front end view [3]

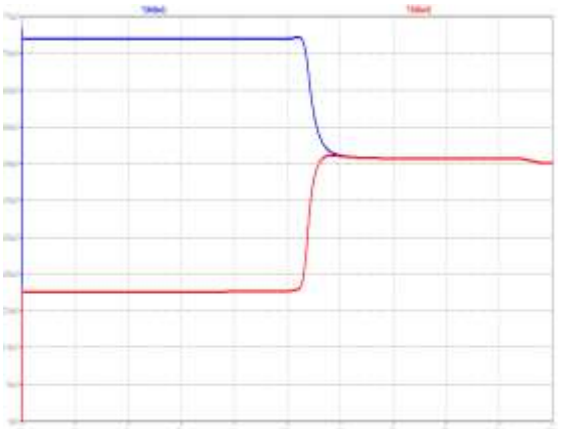

Figure 5 Timing analysis plot for bitline1 and bitline0

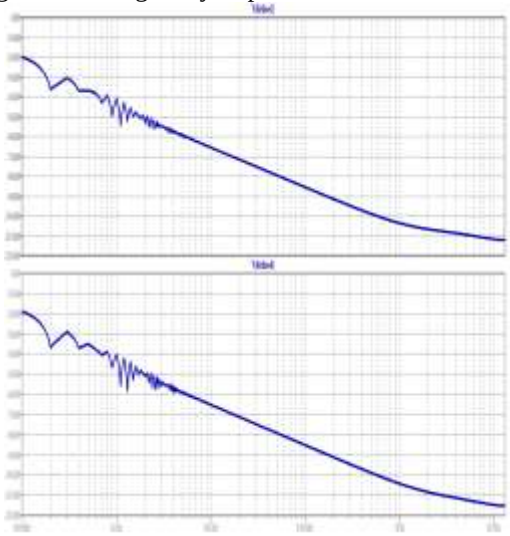

Figure 6 FFT output plot topology1 bitline1 bitline0

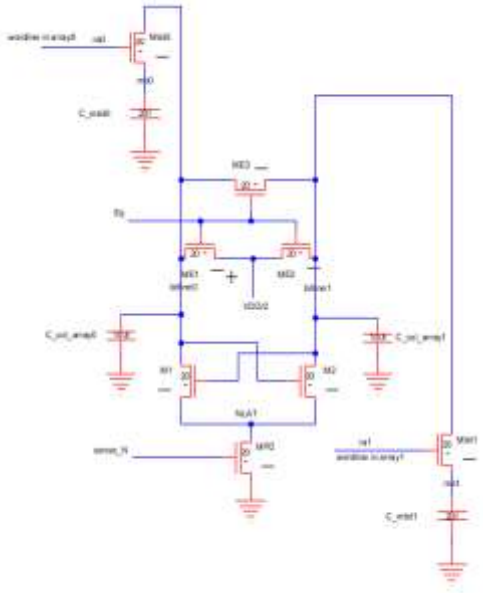

Figure 7 Sense amplifier circuit design topology type – 2 schematic front end view [3]

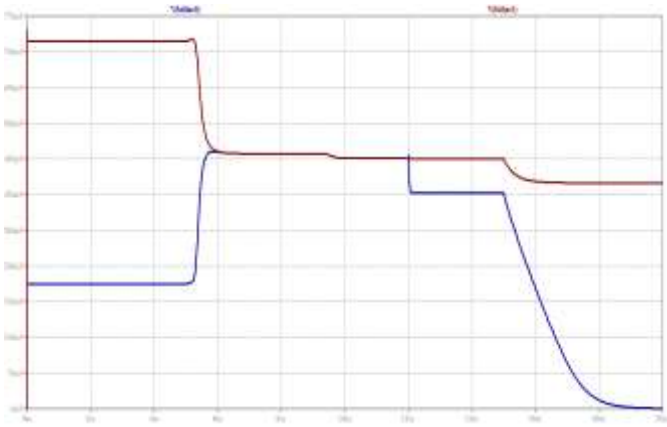

Figure 8 Timing analysis plot for bitline1 and bitline0

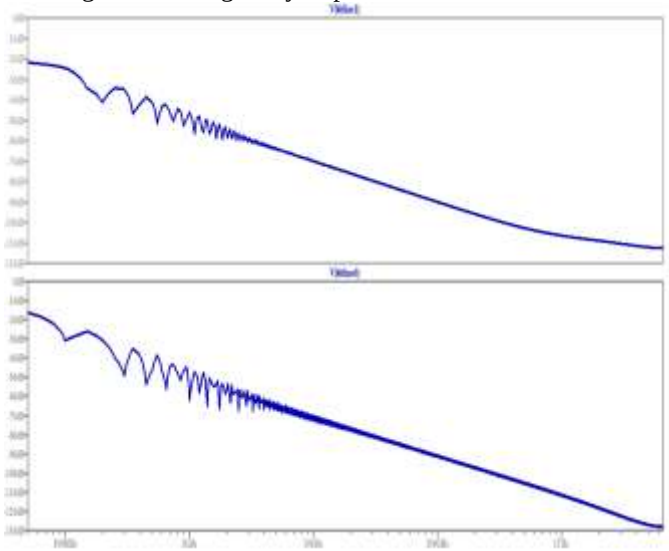

Figure 9. FFT output plot topology 2 bitline1 bitline0

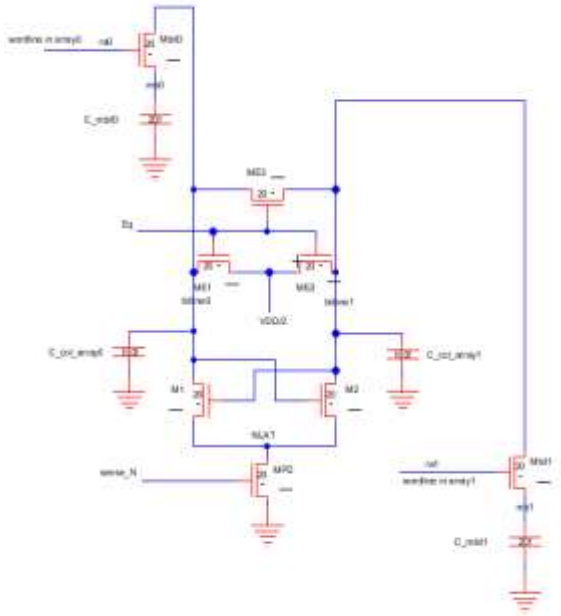

Figure 10 Sense amplifier circuit design topology type – 3 schematic front end view [3]

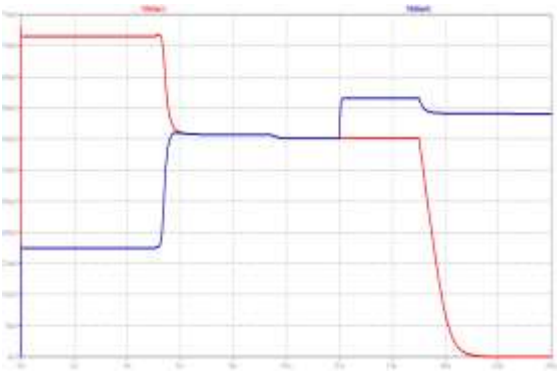

Figure 11 Timing analysis plot for bitline1 and bitline0 topology 3

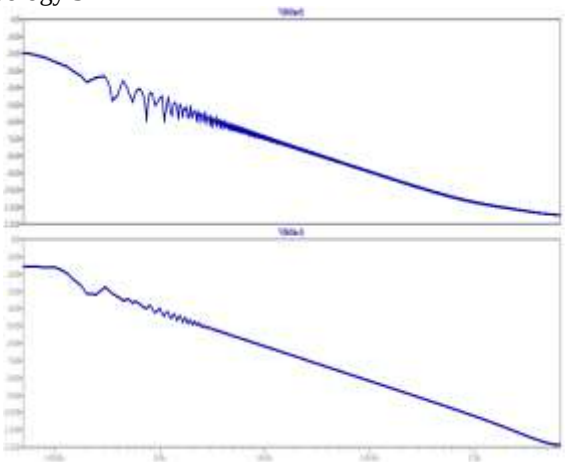

Figure 12 FFT output plot topology 3 bitline1 bitline0

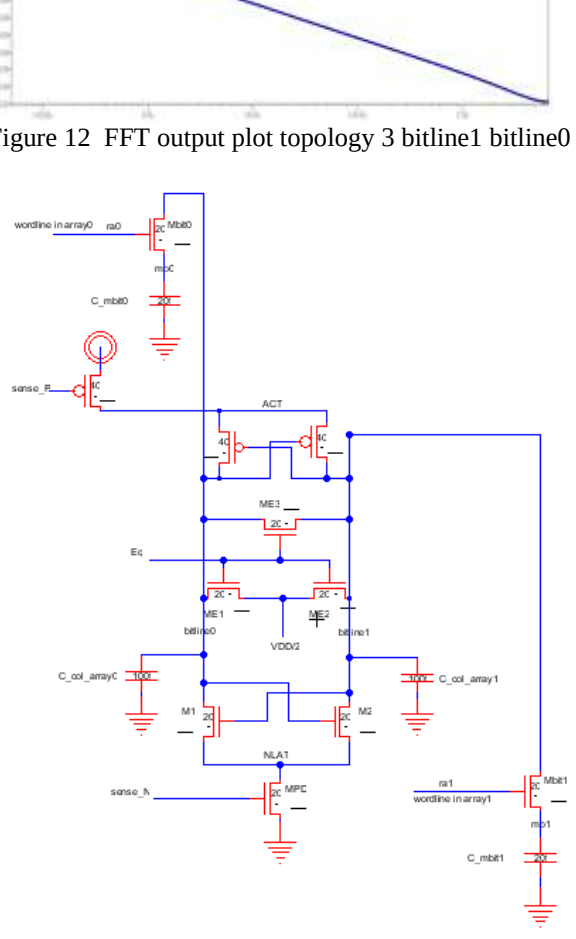

Figure 13 Sense amplifier circuit design topology type – 4 schematic front end view [3]

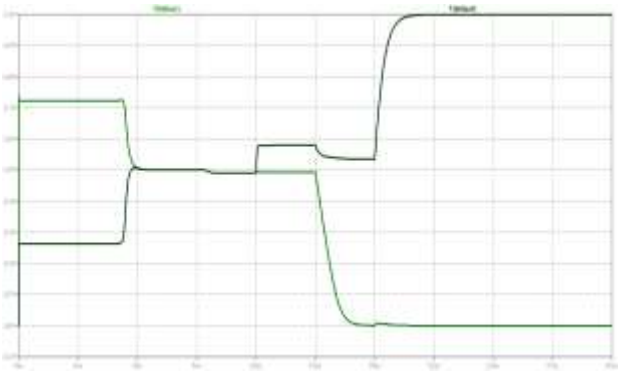

Figure 14 Timing analysis plot for bitline1 and bitline0 topolog4

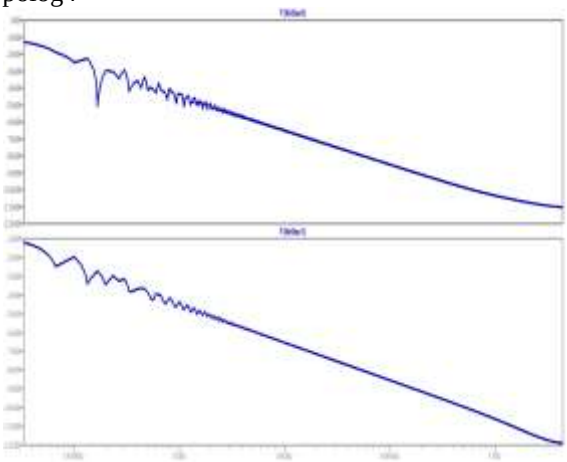

Figure 15 FFT output plot topology 4 bitline1 bitline0

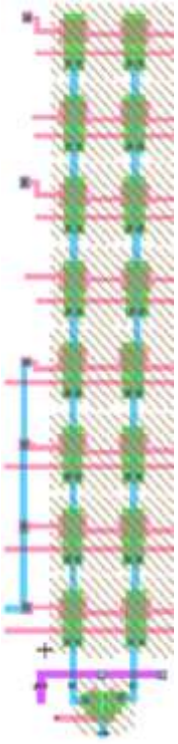

Figure 16 sense amplifier interfacing with DRAM memory bit – Layout view

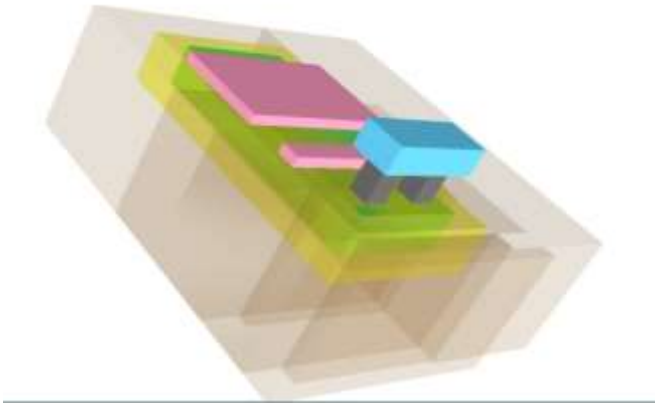

Figure 17-- 3 D view of DRAM memory cell

RESULTS

FFT analysis is done for the all the sense amplifier topologies and is tabulated in table 4.1.a, table 4.1.b, table 4.2.a, table 4.2.b, table 4.3.a, table 4.3.b, table 4.4.a, table 4.4.b

Sense amplifier topologies shown above are simulated for supply reference value 1.3 volts to 1.8 volts with a reference signal is also supplied as a pulsate and timing analysis is carried out for ten or fewer nanoseconds . The bit lines are equilibrated first to half of VSS and any one of them will be pull up to VSS for entire sense procedure.

Table 4.1.a
FFT parameters for sense Amplifier topology 1 for bitline1

Frequency	Amplitude	**Ø**	Delay
100 MHz	-18 dB	-77°	-300ns
1 GHz	-42 dB	-88°	-506ns
10 GHz	-66 dB	-93°	130 ps
100 GHz	-88 dB	-70°	-101ps
1THz	-153 dB	-152°	115 fs
10THz	-131dB	85°	-103fs

Table 4.1.b
FFT parameters for sense Amplifier topology 1 for bitline0

Frequency	Amplitude	Phase	Delay
100 MHz	-17dB	65°	-2ns
1 GHz	-47dB	53°	203ps
10 GHz	-67dB	25°	-91ps
100 GHz	-87dB	35°	-42ps
1THz	-174 dB	65°	13 fs
10THz	-174dB	17°	-105 fs

Table 4.2.a
FFT parameters for sense Amplifier topology 2 for bitline1

Frequency	Amplitude	**Ø**	Delay
100 MHz	-216 dB	-96°	129 ns
1 GHz	-462 dB	-167°	26 ns
10 GHz	-654 dB	-98°	962 ps
100 GHz	-962 dB	-99°	-245 ps
1THz	-444dB	-163°	264 fs
10 THz	-288 dB	186°	156 ps

Table 4.2.b
FFT parameters for sense Amplifier topology 2 for bitline0

Frequency	Amplitude	**Ø**	Delay
100 MHz	-30 dB	-109°	-24 ns
1 GHz	-50 dB	-106°	260 ns
10 GHz	-702 dB	-80°	91 ps
100 GHz	-90 dB	-90°	-9 ps
1 THz	-120 dB	.102°	61 ps
10 THz	-150 dB	-120°	51ps

Table 4.3.a
FFT parameters for sense Amplifier topology 4 bitline 1

Frequency	Amplitude	**Ø**	Delay
100 MHz	-1066 dB	-20°	-38 ps
1 GHz	-400 dB	-86°	58 ps
10 GHz	-627 dB	-228°	65ps
100 GHz	-810 dB	96°	-67ps
1 THz	-452 dB	-22°	-237ps
10 THz	-357 dB	-57°	-205fs

Table 4.3.b
FFT parameters for sense Amplifier topology 3 bitline 0

Frequency	Amplitude	**Ø**	Delay
100 MHz	-208 dB	908°	280 ns
1 GHz	-408 dB	880 °	230 ns
10 GHz	-680 dB	908°	508ps
100 GHz	-808 dB	980°	108 ps
1 THz	-109 dB	104°	-506ps
10 THz	-148 dB	178°	156ps

Table 4.4.a
FFT parameters for sense Amplifier topology 4 bitline 1

Frequency	Amplitude	**Ø**	Delay
100 MHz	-170dB	-150°	12 ns
1 GHz	-470 dB	-90°	174 ns
10 GHz	-675dB	-84°	312ps
100 GHz	-870 dB	-96°	-130ps
1 THz	-176 dB	-142°	-606ps
10 THz	-170 dB	-187°	212ns

Table 4.4.b
FFT parameters for sense Amplifier topology 4 bitline 0

Frequency	Amplitude	**Ø**	Delay
100 MHz	-220 dB	65°	106ns
1 GHz	-420 dB	85°	240ns
10 GHz	-620 dB	85°	-170ps
100 GHz	-84 dB	95°	39ps
1 THz	-160 dB	130°	150ps
10 THz	-145 dB	149°	-70ns

CONCLUSION

With Process technology or library available, DRAM sense amplifiers are implemented, verified and tested interfacing of DRAM sense amplifier circuits. Taking into scalable CMOS library or models; here C5 or 0.3 micrometer four sense Amplifier circuits topologies are implemented [3]. This paper has presented DRC and NCC design matrices and simulation with respect to time using suitable capacitances for bitlines and wordlines. Fast Fourier Transforms are applied for all the sense amplifier design topology and amplitude, phase and respective delays are tabulated for bitline0 , bitline1 for frequency ranges from 10MHz to 10 THz.

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