Implementation of High Speed 16 x 16 Multiplier Using Vedic Mathematics

Indu Turaha[1], Dr. G. Kumar[2] , Rita Jain[3]

[1] *MTech Scholar, Department of VLSI Design, LNCT, Bhopal, turaha.indu@gmail.com, India;*

[2,] *Prof. Department of Electronics & Communication Engineering, LNCT, Bhopal, seetharam.kumar03@gmail.com, India;*

[3] *Prof. Department of Electronics & Communication Engineering, LNCT, Bhopal, ritajain_bpl@yahoo.com, India;*

Abstract *– The need of low area and high speed Multiplier is increasing as the need of high speed processors are needed. Vedic arithmetic is that the traditional system of arithmetic which has a novel technique of calculations supported sixteen Sutras that are discovered by Sri Bharti Krishna Tirthaji. Any processor's performance depends on 3 vital factors specifically speed, space and power. In this paper a multiplier is implemented based on Nikhilam sutra with binary excess unit. The ripple carry adder in the multiplier architecture increases the speed of addition of partial products. The proposed architecture of this paper analysis the logic size, area and power consumption using Xilinx 14.2. The proposed architecture of this paper analysis the logic size, area and power consumption using Xilinx 14.2.*

Keywords*: Vedic multiplier, Array Multiplier, Vedic Mathematics, Urdhva-Tiryagbhyam*

I. Introduction

Arithmetic is the oldest and most elementary branch of Mathematics. The name Arithmetic comes from the Greek word άριθμός (arithmos). Arithmetic is used by almost everyone, for tasks ranging from simple day to day work like counting to advanced science and business calculations. As a result, the need for a faster and efficient Arithmetic Unit in computers has been a topic of interest over decades. The work presented in this thesis, makes use of Vedic Mathematics and goes step by step, by first designing a Vedic Multiplier, then a Multiply Accumulate Unit and then finally an Arithmetic module which uses this multiplier and MAC unit. The four basic operations in elementary arithmetic are addition, subtraction, multiplication and division. Multiplication basically is the mathematical operation of scaling one number by another. Talking about today's engineering world, multiplication based operations are some of the frequently used Functions, currently implemented in many Digital Signal Processing (DSP) applications such as Convolution, Fast Fourier Transform, filtering and in Arithmetic Logic Unit (ALU) of Microprocessors. Since multiplication is such a frequently used operation, it's necessary for a multiplier to be fast and power efficient and so, development of a fast and low power multiplier has been a subject of interest over decades. A N × N bit parallel overlay multiplier factor design is intended for top speed DSP operations. The design relies on the vertical and crosswise algorithmic rule of ancient Indian Vedic arithmetic. So the performance of the multiplier factor may be a key component in crucial the presentation of the complete system. This can be because; the multiplier factor is that the slowest and most time intense considers the system. So the optimization of the multiplier factor speed and space may be a most significant challenge for the structure designers. In his challenge is also successfully overcome by the utilization of ancient Vedic arithmetic. Vedic arithmetic is one of the foremost ancient methodologies used by the Aryans therefore on perform mathematical computation [2]. It consists of algorithm rule that ought to boil down large arithmetic operations to simple mind calculations. The efforts place by Jagadguru swami Sri Bharati avatar Tirtha maharajah to introduce Vedic arithmetic to the commoners additionally as contour Vedic Algorithms into Sixteen classes [1] or Sutras must be acknowledged and appreciated. Sri Bharti Krishna Tirthaji (1884-1960) planned the idea of Vedic arithmetic when his eight years of analysis on Atharva Vedas [1]. This branch of arithmetic depends on sixteen Sanskrit literatures. Vedic arithmetic may be a terribly fascinating field and presents some effective algorithms which will be applied to a range of division of engineering like estimate and digital signal processing. Associating multiplication with Vedic arithmetic methodology would lead to the buildup of procedure time.

Proposed work uses Vedic-mathematics based mostly approach to cut back the quantity of partial merchandise for multiplication, that in-effect reduces the quantity of adders. Vedic arithmetic is that the ancient Indian system of arithmetic that relies on sixteen sutras and its sub-sutras mentioned in Atharva-Veda, and deals with numerous branch of arithmetic like arithmetic, algebra,

geometry, trig, conics, astronomy, calculus etc.

II. Theory

II.1. Multiply Accumulate Unit (MAC)

The Multiply-accumulate operation is one of the basic arithmetic operations extensively used in modern digital signal processing (DSP). Most arithmetic, such as digital filtering, convolution and fast Fourier transform (FFT), requires high-performance multiply accumulate operations. The multiply-accumulator (MAC) unit always lies in the critical path that determines the speed of the overall hardware systems. Therefore, a high-speed MAC that is capable of supporting multiple precisions and parallel operations is highly desirable.

II.2. Basic MAC architecture

Basically a MAC unit employs a fast multiplier fitted in the data path and the multiplied output of multiplier is fed into a fast adder which is set to zero initially. The result of addition is stored in an accumulator register. The MAC unit should be able to produce output in one clock cycle and the new result of addition is added to the previous one and stored in the accumulator register. Fig 1, below shows basic MAC architecture. Here the multiplier that has been used is a Vedic Multiplier built using Urdhva Tiryakbhyam Sutra and has been fitted into the MAC design.

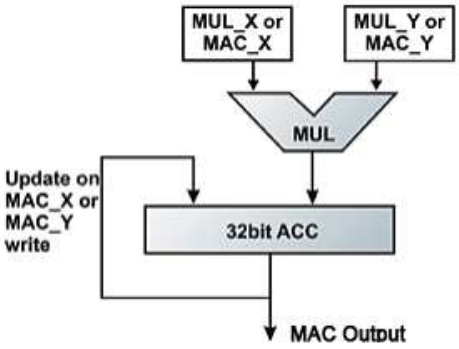

Fig.1 Basic MAC unit

II.3. Arithmetic Module

Full Arithmetic Logic Unit can be considered to be the heart of a CPU, as it handles all the mathematical and logical calculations that are needed to be carried out. Again there may be different modules for handling Arithmetic and Logic functions. In this work, an arithmetic unit has been made using Vedic Mathematics algorithms and performs Multiplication, MAC operation as well as addition and subtraction. For performing addition and subtraction, conventional adder and subtractor have been used. The control signals which tell the arithmetic module, when to perform which operations are provided by the control unit, which is out of the scope of this thesis. It is shown in fig.2.

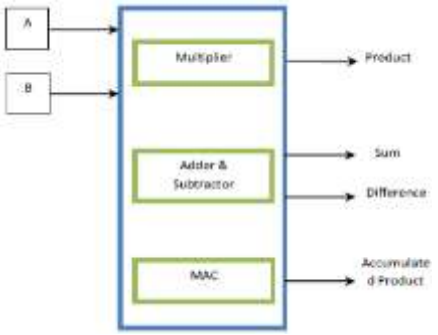

Fig.2 Basic block diagram of Arithmetic unit

III. Method

*III.1. Methodology for 4*4 Vedic multiplier*

The dot representation for 4x4 Vedic multiplier is shown below. Here the first row represents the multiplicand bits (a3a2a1a0) and the 2nd row represents the multiplier bits (b3b2b1b0). In this Vedic multiplication process addition of bits takes place which are of equal weights. In the 1st case 0 weights are added i.e., only a0b0. In 2nd case weights equal to one are added by using half adder i.e., a0b1 +a1b0. In the 3rd case Partial products of weight equal to 3 are added by using full adder i.e., a0b2+a2b0+a1b1. If any carry is generated during addition process, it will be added to the next step of addition. The maximum weight for 4 bit multiplication is 6.The same procedure is followed until we get the output as 8 bits including carry.

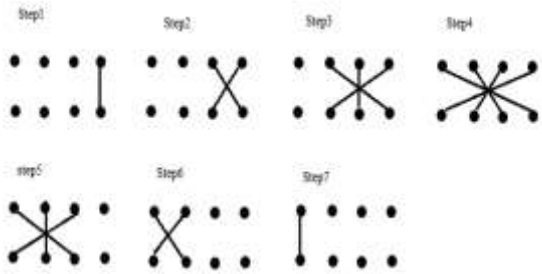

Fig.3 Dot representation of 4x4 Vedic multiplier

The design of 4x4 Vedic multiplier is used as a basic building block diagram for design of 8x8 Vedic multiplier. Further design of 16x16 is implemented by using 8x8 Vedic multiplier as basic building block. The aim of using BEC is to reduce the usage of gates compared to normal Vedic multiplier which in turn reduces the power consumption.

It has 4 groups of same size i.e. each group consists of 8*8 Vedic multiplier whose inputs are partitioned according to Urdhva-tiryagbhyam sutra. Outputs from Vedic multiplier are given as inputs to BEC adders of different sizes.

III.2. Urdhva Tiryakbhyam sutra

The multiplier is based on an algorithm Urdhva

Tiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". It is based on a novel concept through which the generation of all partial products can be done and then, concurrent addition of these partial products can be done. Thus parallelism in generation of partial products and their summation is obtained using Urdhava Tiryakbhyam. The algorithm can be generalized for n x n bit number. Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. Thus the multiplier will require the same amount of time to calculate the product and hence is independent of the clock frequency. The net advantage is that it reduces the need of microprocessors to operate at increasingly high clock frequencies. While a higher clock frequency generally results in increased processing power, its disadvantage is that it also increases power dissipation which results in higher device operating temperatures. By adopting the Vedic multiplier, microprocessors designers can easily circumvent these problems to avoid catastrophic device failures. The processing power of multiplier can easily be increased by increasing the input and output data bus widths since it has a quite a regular structure. Due to its regular structure, it can be easily layout in a silicon chip. The Multiplier has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other multipliers. Therefore it is time, space and power efficient. It is demonstrated that this architecture is quite efficient in terms of silicon area/speed.

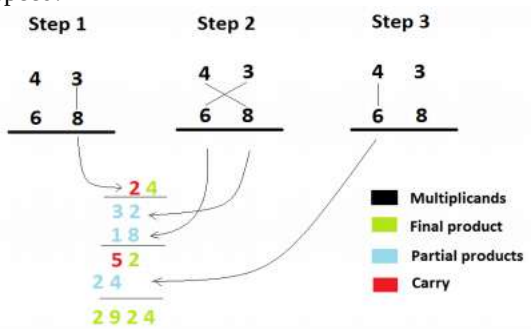

Fig.4 Multiplication of 2 digit decimal numbers using Urdhva Tiryakbhyam Sutra

III.3. Nikhilam Sutra

Nikhilam Sutra literally means "all from 9 and last from 10". Although it is applicable to all cases of multiplication, it is more efficient when the numbers involved are large. Since it finds out the compliment of the large number from its nearest base to perform the multiplication operation on it, larger is the original number, lesser the complexity of the multiplication. We first illustrate this Sutra by considering the multiplication of two decimal numbers (96 * 93) in Fig 4.6. Where the chosen base is 100 which is nearest to and greater than both these two numbers.

The right hand side (RHS) of the product can be obtained by simply multiplying the numbers of the Column 2 (7*4 = 28). The left hand side (LHS) of the product can be found by cross subtracting the second number of Column 2 from the first number of Column 1 or vice versa, i.e., 96 - 7 = 89 or 93 - 4 = 89. The final result is obtained by concatenating RHS and LHS (Answer = 8928).

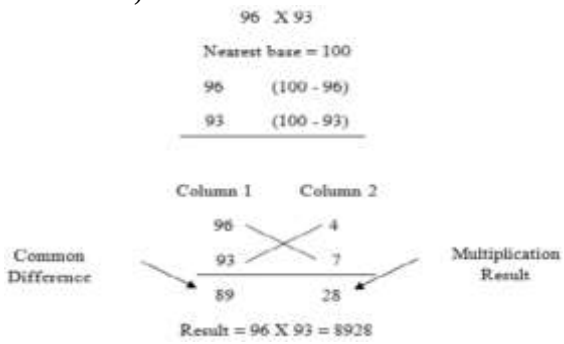

Fig.5 Multiplication Using Nikhilam Sutra

IV. Result

All simulation result and circuitry are presented for the proposed model is in this chapter, in high speed multiplier code was synthesized using XILINX and simulation results are shown below:

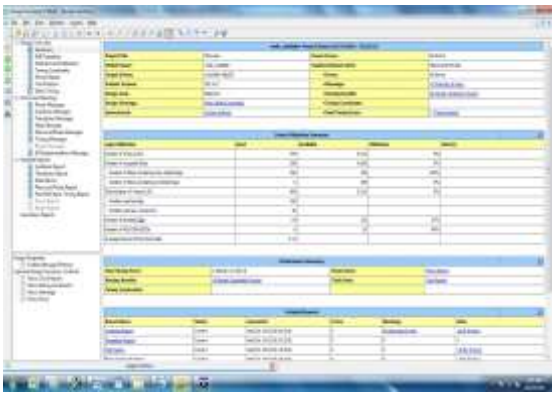

Fig.6 Synthesize report of proposed system

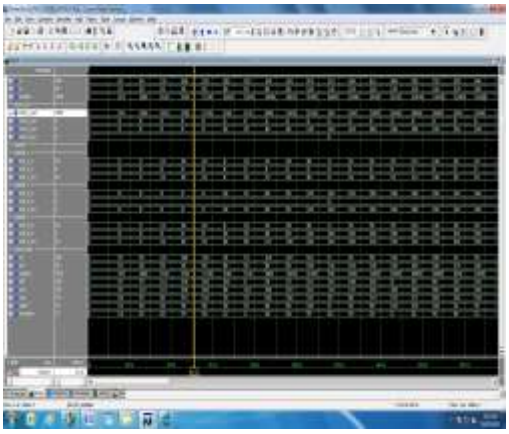

Fig.7 Simulation output of proposed system

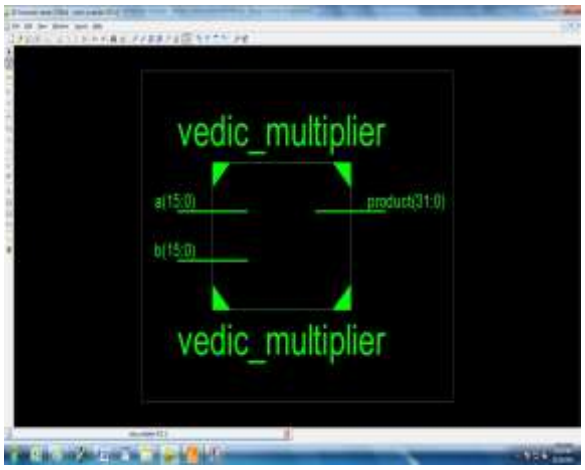

Fig.8 RTL view of vedic multiplier

Fig.9 Power report of proposed system

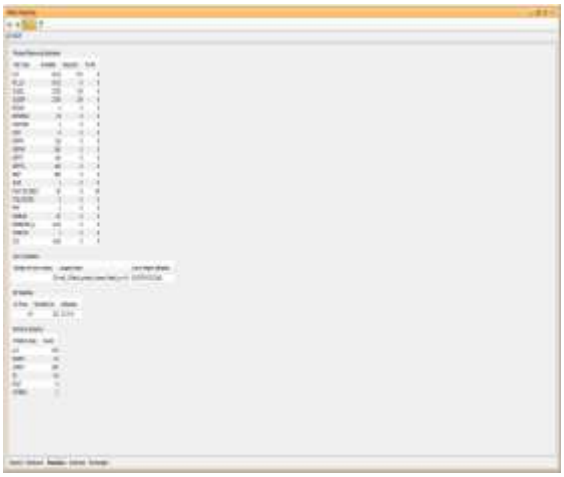

Fig.10 Area report of proposed system

V. Conlusion

The proposed multiplier provides higher performance for higher order bit multiplication. This is mainly due to memory constraints. Effective memory implementation and deployment of memory compression algorithms can yield even better results in terms of area and speed which improves the overall performance of the design. Nikhilam Sutra based Vedic multiplier with BEC is highly efficient algorithm for multiplication. This is mainly due to memory constraints. Effective memory implementation and deployment of memory compression algorithms can yield even better results.

References

[1] S.P.Pohokar, R.S.Sisal, K.M.Gaikwad, M.M.Patil, Rushikesh Borse “Design and Implementation of 16 x 16 Multiplier Using Vedic Mathematics” International Conference on Industrial Instrumentation and Control (ICIC)College of Engineering Pune, India. May 28-30, 2015

[2] Sudeep. M. C, Sharath Bimba. M, Mahendra Vucha, “Design and FPGA Implementation of High Speed Vedic Multiplier”, International Journal of Computer Applications, Volume 90-No. 16, March 2014.

[3] G.Vaithiyanathan, K.Venkatesan, S.Sivaramakrishnan, S.Siva, and S. Jayakumar, “Simulation and Implementation of Vedic Multiplier Using VHDL Code” International Journal of Scientific & Engineering Research Volume 4, January-2013

[4] R.Sridevi, Anirudh Palakurthi, Akhila Sadhula, Hafsa Mahreen,”Design of High Speed Multiplier(Ancient Vedic Mathematics Approach)”, Internationan Journal of Engineering Research, Volume No.2,pp:183-186, July 2013.

[5] Chilton Fernandes, Samarth Borkar, “Application of Vedic Mathematics in Computer Architecture”, International Journal of Research in Engineering and Science (IJRES), Volume 1, September 2013.

[6] Jagadguru Swami Sri Bharti Krishna Tirthaji Maharaja,”Vedic Mathematics or Sixteen Simple Mathematicle Formulae from the Veda, Delhi(1965)”, Motilal Banarsidass, Varanasi,India.

[7] C. Sheshavali, K. Niranjan Kumar, “Design and Implementation of Vedic Multiplier”, International Journal of Engineering Research and Development, Volume-8, PP.23-28, September 2013.

[8] Premananda B.S.Samarth S.Pai, ShashankB.,”Design and Implementation of 8-Bit Vedic Multiplier”, International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Volume 2, December 2013.

[9] G.Ganesh Kumar, V.Charishma, “Design of High Speed Vedic Multiplier using Vedic Mathematics Techniques” International Journal of Scientific and Research Publications, Volume 2, Issue 3, March 2012.

[10] Manoranjan Pradhan, Rutuparna Panda, Sushanta Kumar Sahu, “Speed Comparison of 16x16 Vedic Multpliers”, International Journal of Computer Applications, Volume 21-No.6, May 2011.

[11] H. S. Dhillon and A. Mitra,”A Digital Multiplier Architecture using Urdhava Tiryabhyam Sutra of Vedic Mathematics”, IEEE Conference Proceeding, 2008.

[12] Purushottam D. Chidgupkar Mangesh T. Karad,”The Implementation of Vedic Algorithms in Digital Signal Processing” Global J. of Engng. Educ., Vol.8, No.