# A DETAILED REVIEW OF ARCHITECTURE FOR RADIX-8 BOOTH MULTIPLIER ALGORITHM

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*ABSTRACT:* **Approximate computing applied in software and hardware, has been considered as a new approach to saving area in terms as memory and power in terms as power consumption for circuit, as well as increasing performance. Multiplier is a key arithmetic circuit in many error-tolerant applications such as digital signal processing (DSP). In this paper we review the various scheme for multiplier with performed function such as addition, subtractions, and multiplications for the less power consumption and required less memory area.**

## I. INTRODUCTION

In the Digital world the Booth multiplier techniques has been widely used for high performance signed and unsigned data addition, subtraction and multiplication by encoding and thereby in the terms of results are reducing the number of partial products. A multiplier using the radix-4 (or modified Booth) algorithm is very efficient due to the ease of partial product generation [1]. Logic circuits for binary arithmetic (referred to as arithmetic circuits throughout this thesis) have been studied for many decades. BINARY multipliers are a widely used building block element in the design of microprocessors and embedded systems [4].

A Digital multiplier is the fundamental component in general purpose microprocessor and in DSP. With Comparing the Booth multiplier techniques

with many other arithmetic operations like addition, subtraction and multiplication, the multiplication is more time consuming and power hungry than other operations. Therefore the design of multiplier which reduce the power and increase

the performance is a more challenging task for the researches. If we reduce the count of partial product so we can increase the speed of multiplier [9]. By encoding a number into a binary format,

Arithmetic circuits perform arithmetic operations on the binary numbers, such as addition/subtraction, multiplication and division.

Arithmetic circuits such as adders and multipliers are key components in an arithmetic logic unit (ALU), which is a fundamental building block in microprocessors. The speed and power consumption of the arithmetic circuits highly influence the performance of a processor. Multipliers are more complex than adders and Subtractor, so the speed of a multiplier usually determines the operating speed of Digital processing systems. [1].

On synchronous VLSI designs, synthesis tools employ a significant volume of logic- and gate-level optimizations to minimize the critical path. For example, the circuit re-structuring method reduces the logic depth, thereby decreasing the circuit delay, whereas the gate-sizing approach replaces the critical path cells with those of high driving strength. Although these techniques effectively reduce the critical path, they require an additional overhead of silicon area that inherently increases the energy dissipation [3].

Radix-4 modified Booth is a widely used recoding method, that recodes a binary operand into radix-4 signed digits in the set {−2, −1, 0, 1, 2}. This is a popular recoding since the digit multiplication step to generate the partial products only requires simple shifts and complementation. The resulting number of partial products is about n/2 [4]. Higher radix signed recoding is less popular because the generation of the partial products requires odd multiples of the multiplicand which cannot be achieved by means of simple shifts, but require carry-propagate additions. Fast multiplication uses CSA, (Carry Save Adder), to add the output partial products [8]. A CSA specifically has a delay of about (1.5 – 2)FO4 inverters does not depend on the size of obtained partial product, whereas CPA-Carry Propagate Adder have a delay which can be given as4-15+ FO4 inverters depending on the circuit family, size and architecture.

The rest of this paper is organized as follows in section II we describe a introduction of about booth multiplier and accumulator, in section III we discuss about the rich literature survey for the booth multiplier for radix 4, 8 16 bit. In section IV we discuss about the problem

formulation and statement as we getting from the rich literature survey, finally in section V we conclude the about our paper which is based on the literature survey and specify the future scope.

## II. BOOTH MULTIPLIER AND ACCUMLATOR

In many real-time DSP applications, high performance is a critical concern. In the real world applications addition, subtraction, multiplication and division the multiplication is the basic arithmetic operation which used in the most of the signal processing algorithms. But mainly it's have larger area, larger delay and generally consume more power. However, achieving this may be done at the cost of area, on chip power consumed and delays. Firstly the basic operation of MAC is introduced. A multiplier unit can be divided into three basic steps. For the high speed multiplication and other operations select Modified Booth Algorithm. It is the most commonly used, in which partial product is generated from Multiplicand (A) and Multiplier (B). Although the partial product rows are reduced by using higher radix number such as (4, 8, 16, 32) Booth Encoder but it increases the complexity structure and improves the performance enhancement [6].

## III RELATED WORK

[1] In this paper author discuss the issue regarding application of approximate designs. The details of the paper as follows, An approximate 2-bit adder is deliberately designed for calculating the sum of 1× and 2× of a binary number. This adder requires a small area, a low power and a short critical path delay. Subsequently, the 2-bit adder is employed to implement the less significant section of a recoding adder for generating the triple multiplicand with no carry propagation.

[5] In this paper the main focus of the author are to give a brief review of about VLSI architectures, this review paper discuss the implementation of radix-4 Modified Booth Multiplier and this implementation is compared with Radix-2 Booth Multiplier. Modified Booth's algorithm employs both addition and subtraction and also treats positive and negative operands uniformly. Parallel MAC is frequently used in digital signal processing and video/graphics applications.

[9] This paper focused on a combined process of multiplication and accumulation based on radix-4 & radix-8 booth encodings. In this Paper, we investigate the method of implementing the Parallel MAC with the smallest possible delay. Parallel MAC is frequently used in digital signal processing and video/graphics applications. A new architecture of multiplier and accumulator (MAC) for high-speed arithmetic.

[2] This study developed a high accuracy dynamic error-compensation circuit for fixed-width Booth multipliers based on probability and computer simulation (PACS). PACS begins by generating several potential solutions based on both conditional and expected probability, whereupon the accuracy of the solutions is verified using computer simulation and the solution with the highest accuracy is selected. In addition to being highly accurate, the proposed PACS approach is area-effective.

[7] This brief proposes an accuracy-adjustment fixed-width Booth multiplier that compensates the truncation error using a multilevel conditional probability (MLCP) estimator and derives a closed form for various bit widths L and column information w. Compared with the exhaustive simulations strategy, the proposed MLCP estimator substantially reduces simulation time and easily adjusts accuracy based on mathematical derivations.

[6] In this paper, new hardware architecture of multiplier and accumulator (MAC) for high speed arithmetic was designed. The performance was improved by merging multiplication with accumulation and organize a hybrid type carry save adder (CSA).The proposed CSA tree uses 1's complement based radix-4 and radix-8 modified booth algorithm(MBA). The CSA propagates the carries to the least significant bits of the partial products and generates the least significant bits in advance to reduce the number of the input bits of the final adder.

[8] This paper introduces the configuration and execution of Enhanced Modified Booth multiplier for both signed and unsigned numbers augmentation. Generally the booth encoding method is used to generate the partial products for implementation of large parallel multiplier for all unsigned and some signed bits only, on by adopting the parallel encoding scheme. The necessity of the current circuit framework is a devoted and high speed exceptional multiplier unit for signed and unsigned numbers.

## IV PROBLEM STATEMENT

In this section we describe about the problem formulation and statement as we face the challenges and issues regarding the booth multiplier and accumulator

during the experimental process. In this paper we focus on the rich literature survey of the booth multiplier for partial product to decrease low power and less memory. In the journey of literature survey we getting some issues they are following:-

- There is also requiring additional bit for store partial product bit.
- Need more area to implement adder design.
- Existing design multiplier performance was good but need more power consumption.
- The Multiplier faces the challenges about more power consumption and more required memory area for additional bits.

## V CONCLUSIONS AND FUTURE WORK

This review paper describes the implementation of radix-8 Modified Booth Multiplier to increase the performance enhancement of Booth techniques in the terms of low memory area requires for the operation and less power consumption for these operations. In future we introduce the architecture of pre-encoded multipliers for Digital Signal Processing system based applications on off-line encoding of coefficients. To this extend we used the Non Redundant radix-8 Signed-Digit (NR4SD) encoding technique for our proposed architecture of system

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## REFERENCES

[1] Honglan Jiang, Jie Han, Fei Qiao, Fabrizio Lombardi "Approximate Radix-8 Booth Multipliers for Low-Power and High-Performance Operation" IEEE Transactions on Computers, 2016. Pp 1-8.

[2] Wen-Quan He, Yuan-Ho Chen, Shyh-Jye Jou "High-Accuracy Fixed-Width Booth Multipliers Based on Probability and Simulation" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 62, NO. 8, AUGUST 2015. Pp 2052-2061.

[3] Shin-Kai Chen, Chih-Wei Liu, Tsung-Yi Wu, An-Chi Tsai "Design and Implementation of High-Speed and Energy-Efficient Variable-Latency Speculating Booth Multiplier (VLSBM)" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 60, NO. 10, OCTOBER 2013. Pp 2631-2642.

[4] Elisardo Antelo, Paolo Montuschi, Alberto Nannarelli "Improved 64-bit Radix-16 Booth Multiplier Based on Partial Product Array Height Reduction" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, IEEE 2016. Pp 1-10.

[5] Hemantkumar H. Nikhare, Ashish Singhadia "A Detailed Review on Architectures for 2-DWT by using Radix-4 Booth Multiplier" INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING Vol. 3, Issue 3, March 2015. Pp 80-85.

[6] Deepika Setia, Charu Madhu "Novel Architecture of High Speed Parallel MAC using Carry Select Adder" International Journal of Computer Applications (0975 – 8887) Volume 74– No.1, July 2013. Pp 32-38.

[7] Yuan-Ho Chen "An Accuracy-Adjustment Fixed-Width Booth Multiplier Based on Multilevel Conditional Probability" IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, 2014. Pp 1-6.

[8] Jani Basha Shaik, Susrutha Babu Sukhavasi, Suparshya Babu Sukhavasi, Sai Nikhil.M.V.S, M.Aravind "PROFICIENT REALIZATION OF ENHANCED BOOTH MULTIPLIER FOR SIGNED AND UNSIGNED BITS" International Journal of Advances in Engineering & Technology, Apr., 2015. Pp 184-192.

[9] S.ANITHA, M.VIDYA, D. MAHESH VARMA "Design of Parallel MAC Based On Radix-4 & Radix-8 Modified Booth Algorithm" International Journal of Research in Computer and Communication technology, IJRCCT, ISSN 2278-5841, Vol 1, Issue 7, December 2012. Pp 446-453.

[10] Dhiraj Sangwan, Mahesh K. Yadav "Design and Implementation of Adder/Subtractor and Multiplication Units for Floating-Point Arithmetic" International Journal of Electronics Engineering, 2(1), 2010, pp. 197-203.

[11] C.M.KALAISELVI, V.P.DHIVYAPRIYA, P.NITHYA "REDUCING THE COMPUTATION TIME IN FAST FLOATING POINT MULTIPLIER UNIT" International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE) Volume 4, Issue 10, October 2015.

[12] Jiun-Ping Wang, Shiann-Rong Kuang, Shish-Chang Liang "High-Accuracy Fixed-Width Modified Booth Multipliers for Lossy Applications" IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 19, NO. 1, JANUARY 2011. Pp 52-60.

[13] Liangyu Qian, Chenghua Wang, Weiqiang Liu, Fabrizio Lombardi, Jie Han "Design and Evaluation of An Approximate Wallace-Booth Multiplier" 2016. Pp 1-4.

[14] Z. Babic, A. Avramovic, P. Bulic "An iterative logarithmic multiplier" Microprocessors and Microsystems, Elsevier ltd. 2011, Pp 23–33.