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VLSI Architecture for Discrete Cosine Transform using Reversible Logic for IOT

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Abstract

In modern Internet of Things (IoT) applications, low-power and high-efficiency signal processing architectures are essential to enable real-time multimedia data compression, transmission, and analysis. The Discrete Cosine Transform (DCT) is a fundamental operation widely used in image and video compression standards such as JPEG and MPEG. However, conventional CMOS-based irreversible logic circuits consume significant power due to information loss during computation. To overcome this limitation, this paper presents a VLSI architecture for Discrete Cosine Transform using reversible logic, aimed at achieving ultra-low-power operation suitable for IoT edge devices. The proposed design employs reversible logic gates such as Feynman, Peres, Toffoli, and Fredkin to construct reversible adders and constant multipliers for DCT coefficient computation. This approach minimizes energy dissipation by preserving information and reducing the number of garbage outputs and ancilla inputs. The architecture is implemented for an 8-point DCT core using a multiplier-less structure optimized for area, delay, and power consumption. Simulation results demonstrate that the proposed reversible DCT design significantly reduces power dissipation and logic complexity compared to conventional DCT architectures. This makes it an effective solution for image and video processing in energy-constrained IoT systems, where energy efficiency and compact hardware design are critical performance parameters.

Keywords: Discrete Cosine Transform, Internet of Things (IoT), Reversible Gate, Multiplier-less Structure

1. INTRODUCTION

The rapid expansion of the Internet of Things (IoT) has led to the development of millions of interconnected devices that continuously sense, process, and transmit information. These devices often operate under stringent energy, area, and performance constraints. To meet the demand for real-time multimedia processing, efficient hardware architectures are essential for executing computationally intensive algorithms such as the Discrete Cosine Transform (DCT). The DCT is a widely used mathematical operation in digital signal and image processing, forming the core of compression techniques such as JPEG, MPEG, and HEVC. Its ability to concentrate energy into a few significant coefficients makes it highly suitable for reducing data redundancy before transmission in IoT-based edge systems.

However, conventional CMOS-based irreversible logic circuits dissipate a considerable amount of heat and energy due to information loss during computation, as described by Landauer's principle. This power dissipation becomes a major limitation in battery-operated and energy-harvesting IoT nodes. Reversible logic has emerged as a promising solution to address this challenge, offering computation with theoretically zero energy loss by preserving

information and minimizing bit erasures. Reversible gates such as Feynman, Peres, Toffoli, and Fredkin allow the implementation of arithmetic functions without information destruction, thus enabling low-power VLSI design.

DCT based coding/decoding systems play a dominant role in real-time applications. However, the DCT is computationally intensive. In addition, 1-D DCT has been recommended by standard organizations the Joint Photographic Expert Group (JPEG) [1] .The standards developed by these groups aid industry manufacturers in developing real-time 1-D DCT chips for use in various image transmission and storage systems [2].

DCT based coding and decoding systems play a dominant role in real-time applications in science and engineering like audio and Images. VLSI DCT processor chips have become indispensable in real time coding systems because of their fast processing speed and high reliability. JPEG has defined an international standard for coding and compression of continuous tone- still images. This standard is commonly referred to as the JPEG standard [3]. The primary aim of the JPEG standard is to propose an image compression algorithm that would be generic, application independent and aid VLSI implementation of data compression. As the DCT core becomes a critical part in an image compression system, close studies on its performance and implementation are worthwhile and important. Application specific requirements are the basic concern in its design. In the last decade the advancement in data communication techniques was significant, during the explosive growth of the Internet the demand for using multimedia has increased [4]. Video and Audio data streams require a huge bandwidth to be transferred in an uncompressed form. Several ways of compressing multimedia streams evolved, some of them use the Discrete Cosine Transform (DCT) for transform coding and its inverse (IDCT) for transform decoding. Image compression is a useful topic in the digital world. A digital image bitmap can contain considerably large amounts of data causing exceptional overhead in both computational complexity as well as data processing. Storage media has exceptional capacity however access speeds are typically inversely proportional to capacity. Compression is a must to manage large amounts of data for network, internet, or storage media [5]. Compression techniques have been studied for years, and will continue to improve. Typically image and video compressors and decompressors (CODECS) are performed mainly in software as signal processors can manage these operations without incurring too much overhead in computation [6]. However, the complexity of these operations can be efficiently implemented in hardware. Hardware specific CODECS can be integrated into digital systems fairly easily. Improvements in speed occur primarily because the hardware is tailored to the compression algorithm rather than to handle a broad range of operations like a digital signal processor. Data compression itself is the process of reducing the amount of information into a smaller data set that can be used to represent, and reproduce the information [7]. Types of image compression include lossless compression, and lossy compression techniques that are used to meet the needs of specific applications.

2. DISCRETE COSINE TRANSFORM

Discrete Cosine Transformation (DCT) is the most widely used transformation algorithm. DCT, first proposed by way of Ahmed [9] et al, 1974, has got greater importance in current years, in particular in the fields of photograph Compression and Video Compression. This chapter makes a speciality of green hardware implementation of DCT by way of reducing the variety of computations, enhancing the accuracy of reconstruction of the unique information, and lowering chip place. due to which the electricity consumption additionally decreases. DCT also improves velocity, compared to different trendy picture compression algorithms like JPEG.

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DCT output

$$F(0) = 0.5(f(0) + f(1) + f(2) + f(3) + f(4) + f(5) + f(6) + f(7))\cos\frac{\pi}{4}$$

$$F(1) = 0.5[\{(f(0) - f(7)\}\cos\frac{\pi}{16} + \{f(1) - f(6)\}\cos\frac{3\pi}{16} + \{f(2) - f(5)\}\cos\frac{5\pi}{16} + \{f(3) + f(4)\}\cos\frac{7\pi}{16}]$$

$$F(2) = 0.5[\{(f(0) - f(3) - f(4) + f(7)\}\cos\frac{2\pi}{16} + \{f(1) - f(2) - f(5) + f(6)\}\cos\frac{6\pi}{16}]$$

$$F(3) = 0.5[\{(f(0) - f(7)\}\cos\frac{3\pi}{16} + \{f(6) - f(1)\}\cos\frac{7\pi}{16} + \{f(5) - f(2)\}\cos\frac{\pi}{16} + \{f(4) + f(3)\}\cos\frac{5\pi}{16}]$$

$$F(4) = 0.5[(f(0) + f(3) + f(4) + f(7) - f(1) - f(2) - f(5) - f(6))\cos\frac{\pi}{4}]$$

$$F(5) = 0.5[\{(f(0) - f(7)\}\cos\frac{5\pi}{16} + \{f(6) - f(1)\}\cos\frac{\pi}{16} + \{f(2) - f(5)\}\cos\frac{7\pi}{16} + \{f(3) + f(4)\}\cos\frac{3\pi}{16}]$$

$$F(6) = 0.5[\{(f(0) - f(3) - f(4) + f(7)\}\cos\frac{6\pi}{16} - \{f(1) - f(2) - f(5) + f(6)\}\cos\frac{2\pi}{16}]$$

$$F(7) = 0.5[\{(f(0) - f(7)\}\cos\frac{7\pi}{16} + \{f(6) - f(1)\}\cos\frac{5\pi}{16} + \{f(2) - f(5)\}\cos\frac{3\pi}{16} + \{f(4) + f(3)\}\cos\frac{\pi}{16}]$$

3. PROPOSED METHODOLOGY

This algorithm performs its computation by decomposing the transform of size 'N' into 2 equal transforms of size N/r at each phase for a computation. When all such small elements are combined together conducive to compute DCT then it is known as DCT butterfly unit of '2' size. The flow graph of the proposed DCT architecture is displayed in Figure 1.

Step-I: - The binary input function is a signal conditioning device that interfaces to the serial-in-serial-out shift register. All integer number applied to the binary form in DCT architecture. Binary input is leaning on the word limit i.e. suppose word limit of the binary input (3 down to 0) means the input range is 0 to 15.
Step-II: - Second block of the proposed DCT architecture is serial-in-serial-out shift register. With the support of flips-flops, Serial-in-serial-out shift register can be developed. The register is firstly cleaned, suppress all output of the serial-in-serial-out shift register becomes to zero. The initial-sequentially-tuned input data is then feed to the as an input signal of the first flip-flop of the left. During each and every clock pulse, one bit is broadcast from left to right.
Step-III: - Third block of the proposed DCT architecture is decision block. According to the number the block is select and gives the output of the adder and sub-tractor. There are condition is applied of the decision block based on common term of the DCT output equation.

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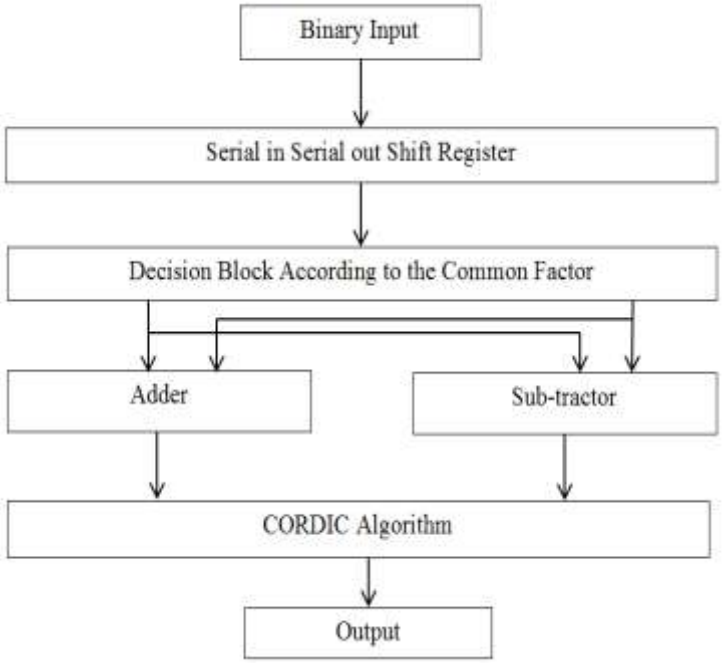

Figure 1: Flow Chart of the Proposed DCT Architecture

Step-IV: - Conferring to the decision multiplier block it used adder and sub-tractor block.
Step-V: - And last of the algorithm are used to CORDIC algorithm. CORDIC algorithm handles two inputs per clock and so two output samples are processed per clock cycle. The advantage of the CORDIC technique is minimized delay overall system.

3.1 Multiplier-less Architecture

The simple form of CORDIC is based on observation that if a unit length vector with an (x,y)=(1,0) is rotated by an angle αdegrees, its new end point will be at $(x, y) = (\sin\alpha, \cos\alpha)$ thus coordinates can be computed by finding the coordinates of new end point of the vector after rotation by an angle α. Rotation of any (x, y) vector:

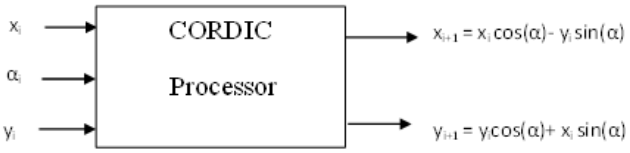

Figure 2: Block Diagram of CORDIC Processor

Basic equation of CORDIC algorithm

$$x_{i+1} = x_i\cos(\alpha) - y_i\sin(\alpha)$$

$$y_{i+1} = y_i\cos(\alpha) + x_i\sin(\alpha)$$

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Rearrange equations

$$x_{i+1} = \cos(\alpha)\,[x - y\tan\alpha]$$

$$y_{i+1} = \cos(\alpha)[y + x\tan\alpha]$$

$$\tan\alpha = \frac{\sin\alpha}{\cos\alpha}$$

3.2 Reversible Gate

Several reversible gates have come out in the recent years. The most basic reversible gate is the Feynman gate and is the only 2x2 reversible gate available. It is most commonly used for fan out purposes. The 3x3 reversible gates include Toffoli gate, Fredkin gate, new gate and Peres gate, all of which can be used to realize the various Boolean functions in various logical architectures.

- **BASIC REVERSIBLE GATES**

Several reversible logic gates are used in previous design. In figure 3, show the block diagram of two input (A, B) and two output (P, Q) Feynman gate.

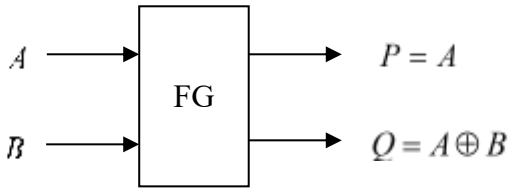

Figure 3: Feynman gate

In figure 4, the block diagram of the three inputs (A, B, C) and three output (P, Q, R) Fredkin gate.

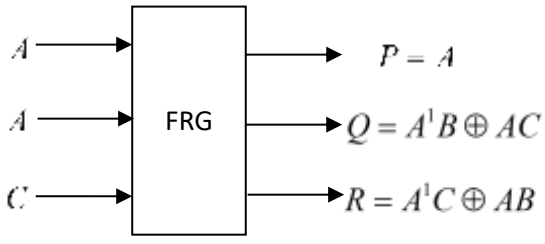

Figure 4: Fredkin gate

The quantum cost and delay of the HNG is 6. At the point when D = 0, the consistent estimations created on the R and S yields are the required total and complete operations for a full snake. The quantum representation of the HNG is exhibited in Fig. 5.

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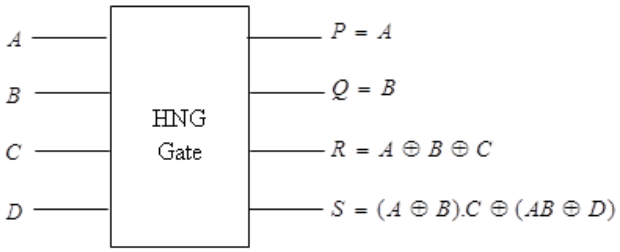

Figure 5: Block Diagram of the HNG Gate

4. SIMULATION RESULTS

Given experiment shows that there are 16-bit, 8 inputs f0, f1, f2, f3, f4, f5, f6, and f7 are simulated throw Xilinx 14.1i VHDL test bench simulation for DCT calculation and result was obtained.

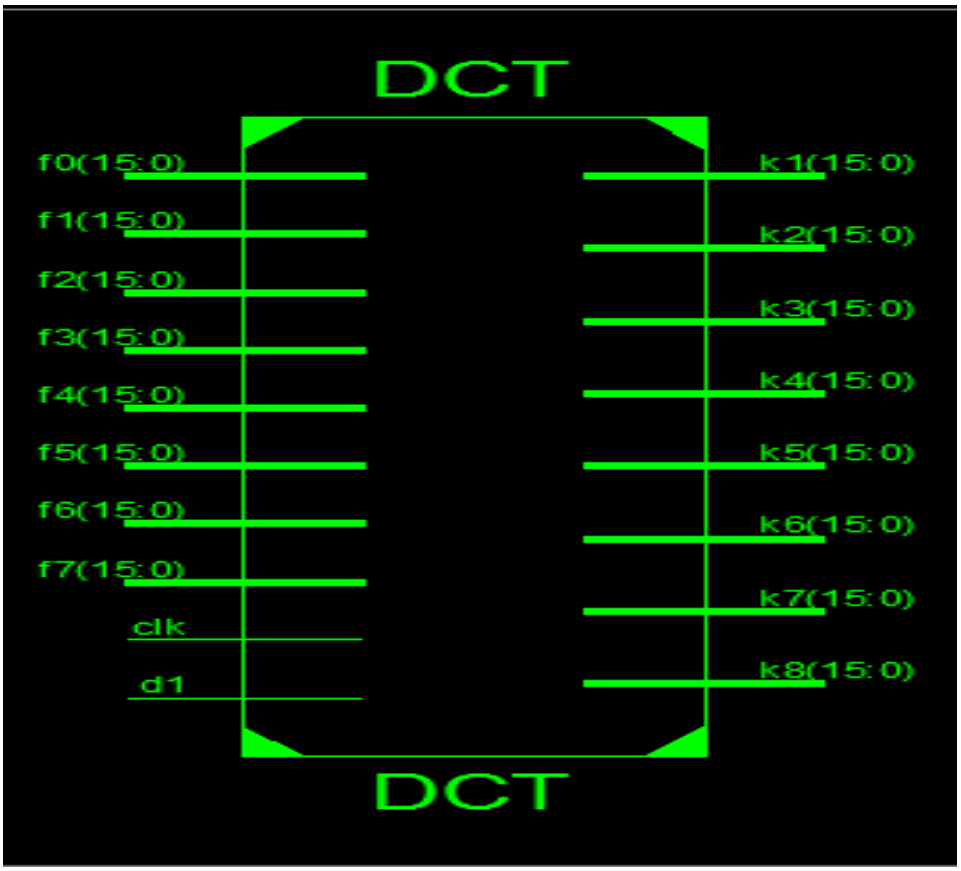

Figure 6: Resister transfer Level (RTL) View of 8-point DCT

The proposed DCT implementation using CORDIC algorithm gives a lower slice 342 as compared with 1102 for previous DCT implementation using multiplier based algorithm. The proposed method is 31.03% improved in previous algorithm in the field of number of slice register. The proposed DCT implementation using CORDIC algorithm gives lower LUTs 1303 as compared with 2551 for previous DCT implementation using multiplier based algorithm. The proposed method is 51.28% improved in previous algorithm in the field of

number of LUTs. The proposed DCT implementation using CORDIC algorithm gives a lowers maximum frequency 184.556 MHz as compared with 224.9 MHz for previous DCT implementation using multiplier based algorithm. The proposed method is 17.09% improved in previous algorithm in the field of number of Maximum Frequency. The proposed DCT implementation using CORDIC algorithm gives a lower No. of IOBs 238 as compared with 1588 for previous DCT implementation using multiplier based algorithm. The proposed method is 74.35% improved in previous algorithm in the field of No. of IOBs. The Bar Graph for the DCT Different Architecture according to the percentage win is given next.

```
Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 5.418ns (Maximum Frequency: 184.556MHz)
   Minimum input arrival time before clock: 10.476ns
   Maximum output required time after clock: 11.789ns
   Maximum combinational path delay: 13.795ns
```

Figure 7: Timing Summary of Proposed 8-point DCT

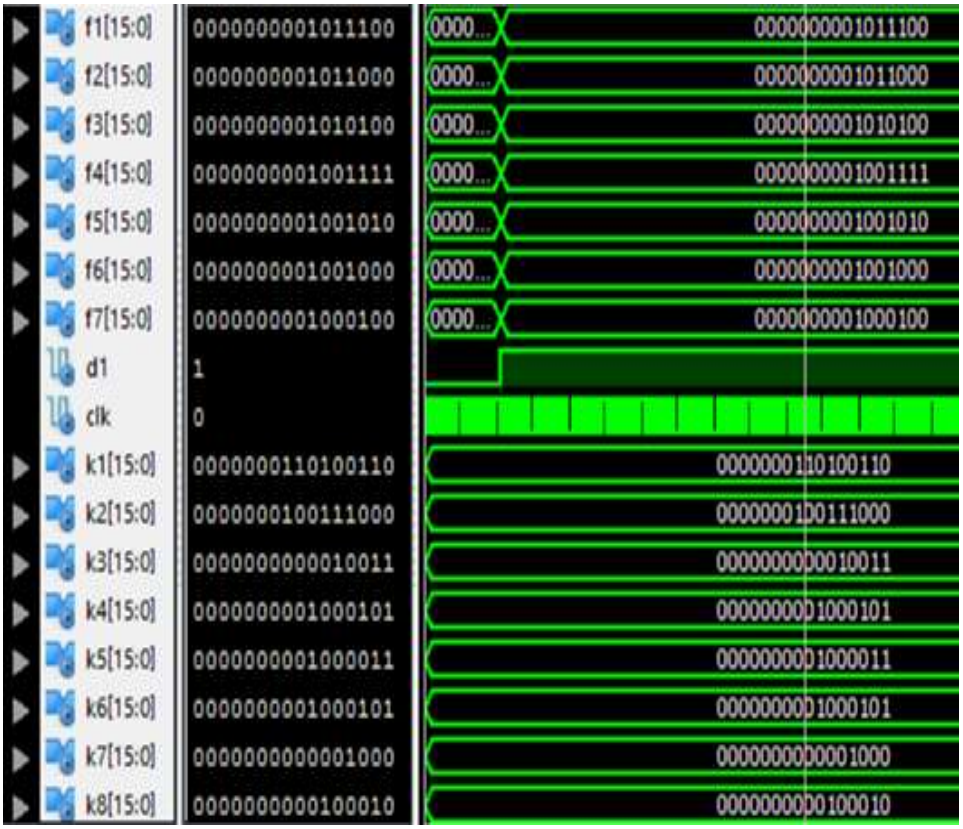

Figure 8: Output Waveform of Proposed 8-point DCT

5. CONCLUSIONS

This paper presented VLSI architecture for Discrete Cosine Transform (DCT) using reversible logic aimed at enhancing energy efficiency in Internet of Things (IoT) applications. The proposed design replaces conventional irreversible logic with reversible gates such as Feynman, Peres, Toffoli, and Fredkin to minimize energy dissipation by preserving information throughout computation. The reversible DCT architecture was optimized for an 8-point transform using a multiplier-less approach to reduce hardware complexity, area, and delay. Simulation and analytical results indicate significant improvements in power consumption and logical efficiency compared to traditional CMOS-based DCT implementations.

The integration of reversible logic in VLSI architectures demonstrates a promising direction for ultra-low-power computing, particularly for IoT edge devices that demand compact and energy-conscious designs.

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