Low Delay and Power of Memory Storage Pulse Trigger Flip Flop using Various Techniques

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***Abstract*—Power consumption plays an import role in any integrated circuit, VLSI design and electronic device. In this paper a literature review of true single phase clocking (TSPC), clock pair shared flip flop (CPSFF) and multi threshold voltage complementary metal oxide semiconductor (MTCMOS) techniques. Among those techniques clocked pair shared flip flop consume least power than true single phase clocking flip flop. MTCMOS technique which reduce the power consumption by approximately 40% to 60% than the original CPSFF**

Keywords: - Flip flop, TSPC, CPSFF, and MTCMOS.

I. INTRODUCTION

A flip-flop or latch is a circuit that has two stable states and can be used to store state information. A flip-flop is a bistable multivibrator. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic. Flip-flops and latches are a fundamental building block of digital electronics systems used in computers, communications, and many other types of systems.

Flip-flops can be either simple (transparent or asynchronous) or clocked (synchronous); the transparent ones are commonly called latches. The word latch is mainly used for storage elements, while clocked devices are described as flip-flops. Simple flip-flops can be built around a pair of cross-coupled inverting elements: vacuum tubes, bipolar transistors, field effect transistors, inverters, and inverting logic gates have all been used in practical circuits. Clocked devices are specially designed for synchronous systems; such devices ignore their inputs except at the transition of a dedicated clock signal (known as clocking, pulsing, or strobing). Clocking causes the flip-flop to either change or retain its output signal based upon the values of the input signals at the transition. Some flip-flops change output on the rising edge of the clock, others on the falling edge. The optimization to minimize area at all costs, has only been secondary to the fixation on increasing circuit speed and again our position is that this should be examined with respect to its effect on power consumption. Some of the techniques that will be presented will come at the expense of increased silicon area and thus the cost of the implementation will be increased.

A cell library includes a number of cells with different functionalities, where each cell may be available in several sizes and with different driving capability. Two central categories of cells included in cell libraries are flip-flops and latches. These are extremely important circuit elements in any synchronous VLSI chip. They are not only responsible for correct timing, functionality, and performance of the chips, but also their clocked devices consume a significant portion of the total active power. Based on the comparison of the power breakdown for different elements in VLSI chips, latches and flip-flops are the major source of the power consumption in synchronous systems. Latches and flip-flops have a direct impact on power consumption and speed of VLSI systems. Therefore study on low-power and high performance latches and flip-flops is inevitable. A universal flip-flop with the best performance, lowest power consumption, and highest robustness against noise would be an ideal component to be included in cell libraries. However, increasing the performance of flip-flops generally involves significant power and robustness trade-offs.

The desirability of this tradeoff can only be determined with respect to a given market situation, but in many cases a moderate increase in area can have substantial impact on the power requirements. It is clear that if power reduction is more important than increasing circuit clock rate, then the area consumed by large clock buffers, power distribution busses and predictive circuit architectures would be better spent to reduce the power dissipation.

The total power consumption per device is the sum of a dynamic component from charging and discharging the capacitance and a static component from the leakage current:

$$P_{tot} = P_{dyn} + P_{stat} \quad (1)$$

$$= arf_c C_L V_{DD}^2 I_{off} V_{DD} \quad (2)$$

In this expression f_c is the clock frequency and ar is the switching probability.

The Clock Divider circuit has found immense application in multiple clock domain (MCD) systems like ASICs, SoC (System on Chip) and GALS (Globally Asynchronous, Locally Synchronous).SoC, which is an IC designed by stitching together multiple stand-alone VLSI designs (called

IPs) to provide full functionality for an application [l] has different IP blocks operating at different clock frequency. Clock generation and clock distribution for these MCD systems are the costliest in terms of power consumption [2].The clock generation system generates different frequencies for the clock domains from the basic crystal oscillator (tens of MHz) using PLLs(as frequency multipliers) followed by Clock Dividers. Hence minimizing the power consumption of the clock divider circuit is a crucial step in the design of Clock generator circuit for MCD systems.

II. DESIGN A PULSE TRIGGERED FLIP FLOP IN VARIOUS TECHNIQUE

Recalling the four circuits reviewed in Section II-A, they all encounter the same worst case timing occurring at 0 to 1 data transitions. Referring to Fig. 1, the proposed design adopts a signal feed-through technique to improve this delay. Similar to the SCDFF design, the proposed design also employs a static latch structure and a conditional discharge scheme to avoid superfluous switching at an internal node. However, there are three major differences that lead to a unique TSPC latch structure and make the proposed design distinct from the previous one. First, a weak pull-up pMOS transistor MP1 with gate connected to the ground is used in the first stage of the TSPC latch. This gives rise to a pseudo-nMOS logic style design, and the charge keeper circuit for the internal node *X* can be saved. In addition to the circuit simplicity, this approach also reduces the load capacitance of node *X* [2], [3]. Second, a pass transistor MNx controlled by the pulse clock is included so that input data can drive node Q of the latch directly (the signal feed-through scheme). Along with the pull-up transistor MP2 at the second stage inverter of the TSPC latch, this extra passage facilitates auxiliary signal driving from the input source to node Q. The node level can thus be quickly pulled up to shorten the data transition delay. Third, the pull-down network of the second stage inverter is completely removed. Instead, the newly employed pass transistor MNx provides a discharging path. The role played by MNx is thus twofold, i.e., providing extra driving to node Q during 0 to 1 data transitions, and discharging node Q during “1” to “0” data transitions. Compared with the latch structure used in SCDFF design, the circuit savings of the proposed design include a charge keeper (two inverters), a pull-down network (two nMOS transistors), and a control inverter. The only extra component introduced is an nMOS pass transistor to support signal feed through. This scheme actually improves the “0” to “1” delay and thus reduces the disparity between the rise time and the fall time delays. In comparison with other P-FF designs such as ep-DCO, CDFF, and SCDFF, the proposed design shows the most balanced delay behaviors.

III. SIMULATION RESULT

The conventional P-FF designs, CDFF, static CDFF, MHLFF, P-FF, CPSFF and MTCMOS circuits could be drawn by using the DSCH tool and verified by the level of the section in the designed circuit. The layout and the compilation could be verified using MICROWIND. DSCH and MICROWIND tools are used to carry out the work for different technologies like 25nm, 65nm and 90nm.

The design of all schematics, input output waveform based on DSCH and layout for all based on MICROWIND are shown below figure 1-3 respectively.

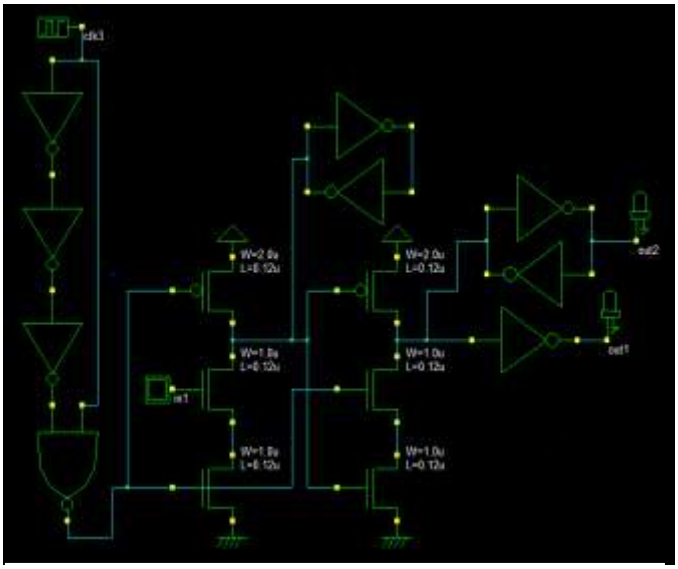
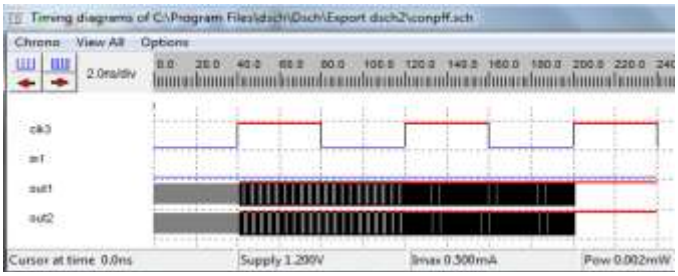
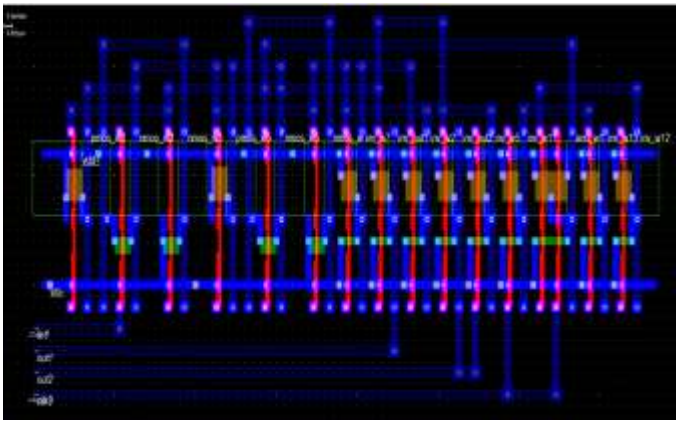


Figure 1: Schematic level for convention P-FF





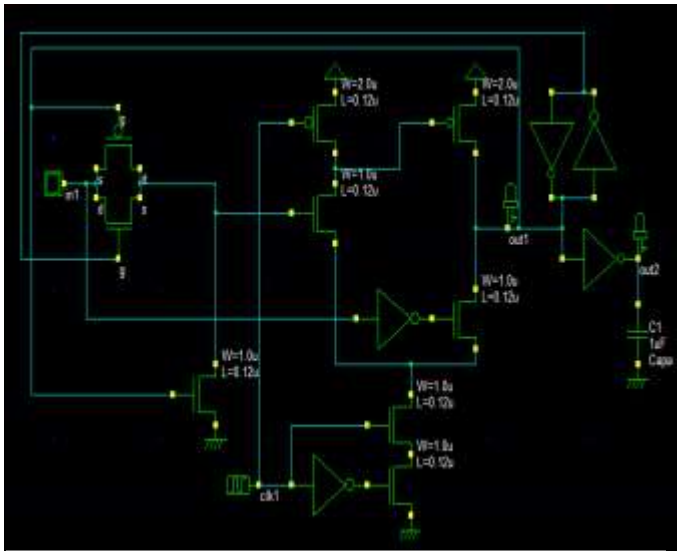
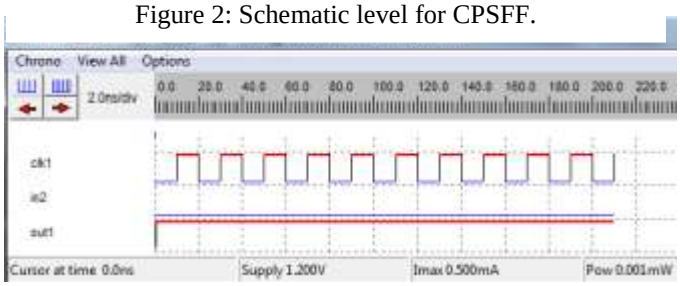
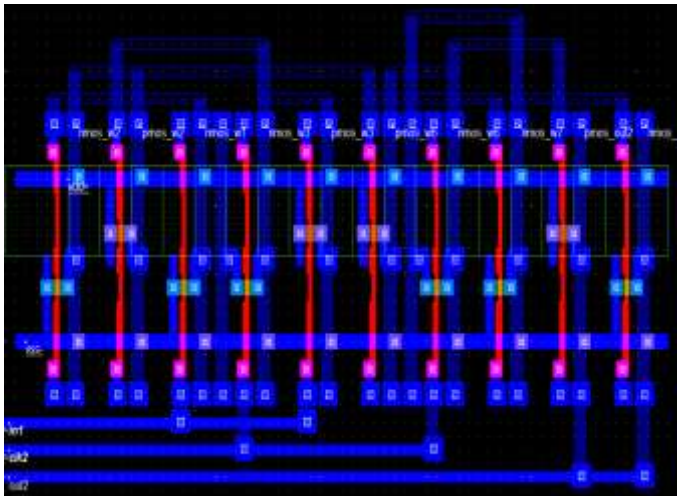


Figure 2: Schematic level for CPSFF.





The target technology is the TSMC 90-nm CMOS process. Since pulse width design is crucial to the correctness of data capture as well as the power consumption [10]–[13], the transistors of the pulse generator logic are sized for a design spec of 120 ps in pulse width in the TT case. The sizing also ensures that the pulse generators can function properly in all process corners. With regard to the latch structures, each P-FF design is individually optimized subject to the product of power and D-to-Q delay. To mimic the signal rise and fall time delays, input signals are generated through buffers.

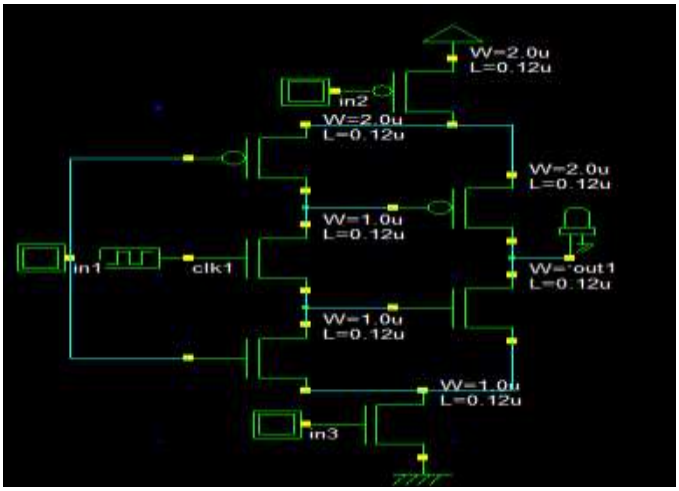
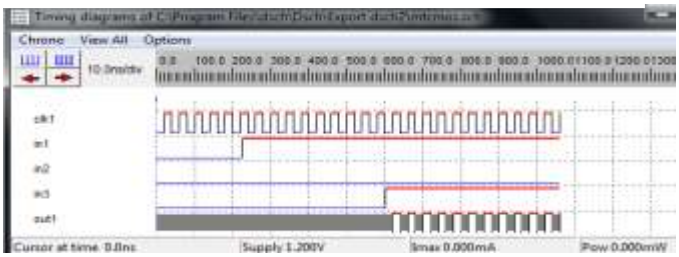
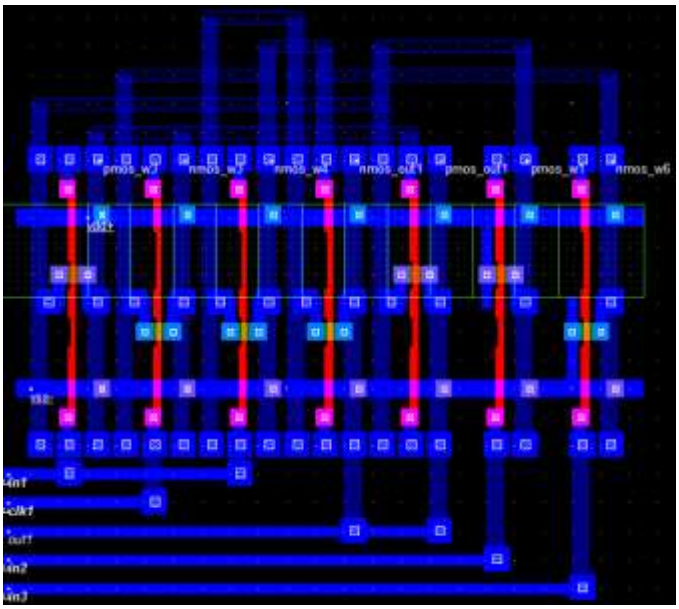


Figure 3: Schematic level for MTCOS.





The latch part is almost same as that CPSFF.The latch consists of transistors. Each transistor is having its own use. Instead of using clock for recharging, a small pull-up pMOS transistor P4 is used whose input is continuously grounded. So, node X will be high most of the time. The evaluation path transistor N6 is controlled by the feedback from the output (q fdbk). Therefore, if the state of input data is same as that of output evaluation path will be turned off preventing the discharge at node X. This results in power saving when input data remains idle for more than one clock cycle. Although P4 is statically

ON, it will not result in static power dissipation because as soon as the data sampling finishes and 'q' obtains the value of 'data', the pull down path get turned off node X is pulled back to high without any static power being dissipated. There are 3 transistors stacked in the evaluation path which less when compared with other flip flops.

Table 1: Power dissipation comparisons for different technologies

Design	Technologies		
	90nm	65nm	25nm
Conventional P-FF	56.466 uW	82.3 uW	5.409 uW
CDFF	1.474 mw	90.416 uw	0.641 mw
CPSFF	0.734mW	51.32uW	0.754mW
MTCMOS	0.111mW	46.308uW	0.437mW

IV. CONCLUSION

This paper simulated CDFF, CPSFF and MTCMOS designed with different transistor is having different power dissipation. The flip flops are simulated for 90nm, 65nm and 25nm nodes using the DSCH and MICROWIND tools.

The key idea was to provide a signal feed through from input source to the internal node of the latch, which would facilitate extra driving to shorten the transition time and enhance both power and speed performance. The design was intelligently achieved by employing a simple pass transistor. Hence from results, as the technologies is scaled down power dissipation increases. MTCMOS are suitable for high performance applications like level converters, microprocessors, clocking system counter etc.

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