Survey on: Reversible Logic Gate Based Design of Binary Comparator

Manish Shrivastava and B.B. Soni

Department of VLSI Design, NRI Institute of Information Science and Technology, Bhopal India

Email: [1]manishiitrn85@gmail.com , [2] brizsoni@gmail.com

***Abstrac*t- In the present time, improvement of some fields like nanotechnology, low power design and quantum computing reversible logic circuit has emerged as a great prospect of research. With she help of using existing reversible gates a 4 bit reversible comparator based on classical logic circuit is represented. This work presents a BIST based architecture of a comparator design has a reduced number of constant inputs, garbage outputs and quantum cost.**

Keywords *- BIST, comparator, quantum cost, reversible gat architecture, garbage output.*

I. INTRODUCTION

The promising practical strategies have been considered for power-efficient computing is Reversible logic. When one bit of information losses, *KTIn2* joules of energy dissipate (K is the Boltzman's constant and T is the operational temperature) this energy could be saved by using reversible logic gate. The issue arises here when the inputs cannot be recovered from circuit's outputs, information loss appears. Reversible logic circuits are there to overcome this issue. And also in future circuit design the reversible circuits provides the solution against the heat dissipation. The principle followed by reversible computing is forced by the Von Neuman Landauer (VNL) he presents a theorem of modern physics effectively irreversible logic operations with belligerently overwrite previous outputs. It requires fundamental minimum energy cost. Typically such operations wasted some amount of the logic signal energy, itself irreducible due to thermal noise. The number of inputs and outputs is equal, one to one mapping exists between the inputs and outputs, So inputs can be recovered from outputs is called reversible logic circuits. The applications like nanotechnology, quantum computing, optical information processing, and quantum dot cellular automata (QCA) utilized by reversible logic circuit. The following points are to be considered for achieving an optimized reversible circuit.

- Fan-out is forbidden.
- Loop and Feedback are not allowed.
- Minimum Delay should be there.
- Optimization parameters should be minimum.

The number of reversible gates, number of constant inputs, garbage outputs, and quantum cost (QC) are the optimization parameters and are defined as: grammar :

A. *Constant Inputs*

The inputs, which are constant inputs, are equal to 0 or I.

B. *Garbage outputs*

The output vectors which do not generate any useful function are garbage outputs I.

C. *Quantum Cost*

In terms of primitive gate (4) the cost of the circuit is refers to Quantum cost.

A 4 bit reversible comparator is designed, in proposed paper. The description of some reversible logic gates, in section II, Which are used in circuit construction. Representation of Classical implementation of comparator in section III. In section IV and V New design of 4 bit reversible comparator and comparing with prior design are presented finally, the conclusion is made in section VI.

II. BASIC REVERSIBLE LOGIC GATES

Reversible logic gates : In an nxn reversible gate, the input vectors are generally abbreviated using (A.B.C.--) and the output vectors are generally abbreviated using (P.Q.R. ...). The performance of the reversible circuit is based on the following parameters.

1) *Garbage output*: The number of unemployed Outputs present in the reversible logic circuit are called garbage output. In other words we can define those supplementary outputs that can be added to make the number of inputs and outputs equal whenever necessary. The numbers of outputs which are not used in the synthesis of a given function are called garbage outputs. In certain cases these become mandatory to achieve reversibility.

2) *Number of Reversible Logic Gates* : It is the total number of reversible logic used in the circuit.

3) *Reversible Logic Function* : A Boolean Function f(x1, x2,x3 .....xN) is said to be reversible if it satisfies the conditions.

(i) The number of inputs is equal to the number of the number of outputs.

(ii) Every output vector has a unique pre-image.

4) *Delay*: Maximum number of unit delay gates in the path of propagation of inputs to outputs.

5) *Constant inputs*: The number of input which the maintained constant at 0 or 1 in order to get the required function.

6) Quantum Cost (QC): Quantum cost present the cost of the circuit in terms of the cost of a primitive gate. It is completed knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit.

7) *Gate levels Logic Depth:* To realize the given logic functions the number of levels in the circuit which are required is presented by gage level.

8) *Flexibility* : This refers to the universally of a reversible logic gate in realizing more functions.

9) *Gate Count*: The number of reversible Gates required realizing the function.

The different types reversible logic gates available are listed in Table-I.

Gate	Block Symbol	Output Equation
Feynman Gate	A, B → FG → P, Q	P = A Q = A xor B
TR Gate	A, B, C → TRG → P, Q, R	P = A Q = A xor B R = A and B'
BJN Gate	A, B, C → BJNG → P, Q, R	P = A Q = B R = (A or B) xor C
Double Feynman Gate	A, B, C → DFG → P, Q, R	P = A Q = A xor B R = A xor C
Toffoli Gate	A, B, C → TG → P, Q, R	P = A Q = B R = (A and B) xor C
Fredkin Gate	A, B, C → FG → P, Q, R	P = A Q = (A' and B) xor (A and C) R = (A' and C) xor (A and B)

III. DESIGN OF REVERSIBLE LOGIC COMPARATOR

In logic comparator of 4 bit, two 4 bit numbers are compared with each other and the result shows that if one number is larger or less than other or if the two numbers are equal with each other. For example, assume A= {A3A2A1 A0}, and B= {B3B2B1} are the inputs then the outputs represents the conditions of comparison and are shown by A<B, A>B with the help of the outputs of several logic

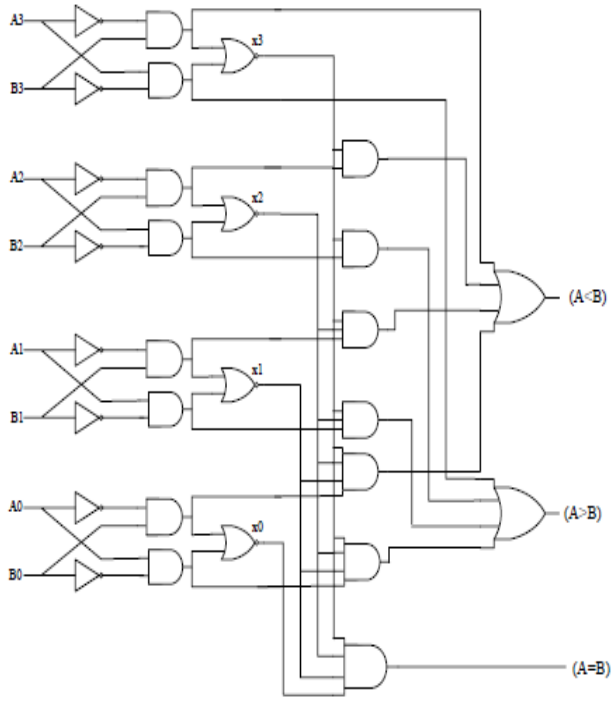

Fig. 1. Classical 4-bit comparator Architecture-I

gate. Fig. I shows the implementation of one of the 4-bit classical comparator and present three different conditions of the comparison.

The equations that the implemented in the shown classical 4 bit comparator are

$X0= A_0' B_0+A_0B_0'$

$X1= A_1' B_1+A_1B_1'$

$X2= A_2' B_2+A_2B_2'$

$X3= A_3' B_3+A_3B_3'$

(A=B) = X0 X1 X2 X3

$(A>B) = A_3 B_3+X3 A_2 B_{2+} X2 A_1 B_{1'+} X1 A_0 B_0'$

$(A<B) = A_3' B_3+X3 A_2' B_{2+} X2 A_1' B_{1'+} X1 A_0' B_0'$

Another architecture [1] of 4-bit comparator is shown in fig. 2. This design uses the following functions.

(A=B) = x3x2x1x0

(A>B) = A3B3' +x3A2B2' +x3 A1B1' +x3x2x1A0 B0'

(A<B) = A3'B3+x3A2'B2+x3x2A1'B1+3x2xA0' B0

xi= AiBi+Ai'Bi' , for i=0,1,2,3.

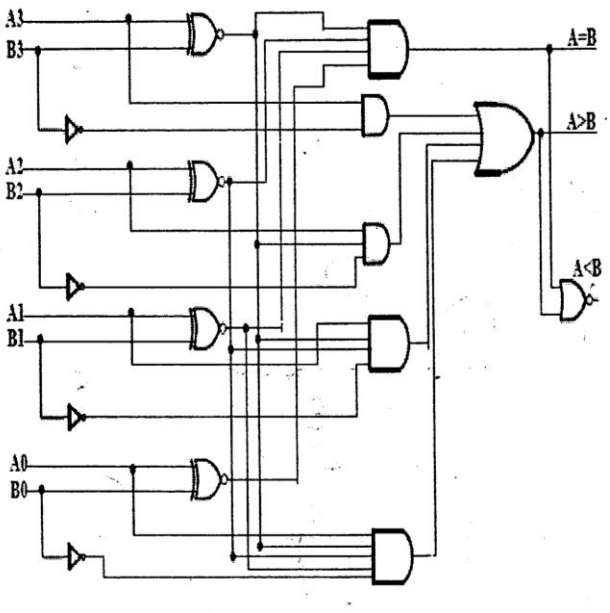

Fig. 2 Classical 4-bit comparator Architecture -2

In the above design 4 bit reversible comparator based on reversible logic gates in designed. Compared with prior designs, proposed circuit is optimized in number of constant inputs, number of garbage outputs and, quantum cost. This reversible circuit is useful for nanotechnology, quantum computing and low power design.

The reference paper (2) aims to design a fault tolerant full adder using the new Parity conserving Toffoli Gate, which can in turn be employed to construct ripple carry address, and other high speed adders. The design has the most optimized performance parameters than its counterparts that are studied in the literature. Full adders like the carry look ahead, carry skip, carry save etc. The full adder must be less complex in nature, and must simultaneously be fault tolerant. Most of the full adders that are encountered in literature address the complexity issue in terms of hardware implementation is quite often neglected nevertheless due care is taken in this paper; this is the crux behind the work.

in [3], the paper shows a design of the reversible comparator based on the quantum gates implementation of the reversible DG gate. The reversible DG gate is designed by using 3x3 quantum gates such as NOT, CNOT, Controlled-V and Controlled-V+ gates. Also, we have used the TR gate and various types of quantum gates in the implementation results. Low power three-bit is designed using DG Gate, New Gate and Fredkin Gate. In order to evaluate the benefit of using the DG gate proposed in this paper, one-bit comparator is constructed. The design is useful for the future computing techniques like quantum computers. The proposed designs

are implemented using VHDL and functionally investigated using Quartos II simulator. Fig 3 and Fig. 4 represents 3-bit comparator circuits that are proposed in [3].

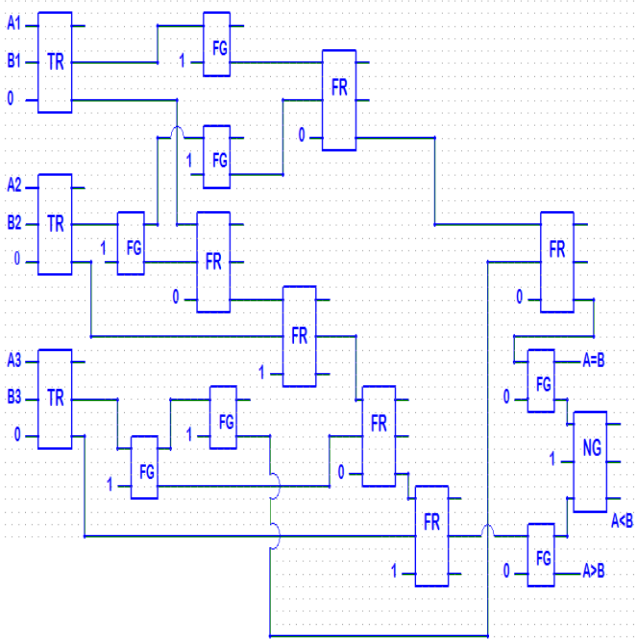

Fig 3 TR Gate based architecture of 3-bit comparator

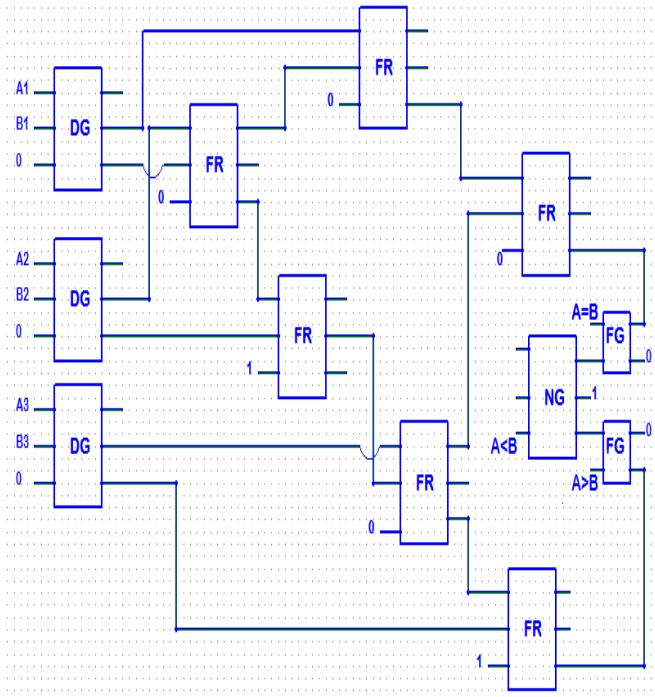

Fig 4 DG Gate based architecture of 3-bit comparator

This paper presents new designs of reversible one and three-bit comparators based on the quantum gates implementation of the reversible TR and DG. The main goal of this paper is optimized in terms of number of garbage outputs, gate count and quantum cost for comparator designs. The proposed DG gate can be combined with TR gate and various types of reversible logic gates to design minimal quantum cost and garbage less reversible circuits. The newly proposed DG gate can be used for implementing concurrent EXOR and EXNOR output functions. Hence, three outputs of DG gate have efficient results for comparator designs. In this paper, one-bit comparator has better performance comparatively.

Reference [4] has introduced and proposed reversible logic gates and reversible circuits for realizing different code converters like BCD to Excess-3, Excess-3 to BCD, Binary to Gray and Gray to Binary using reversible logic gates. The proposed design leads to the reduction of power consumption compared with conventional logic circuits, the design proposed is implemented with FG and URG gates only in near future with the invent of new RLG the power consumption may reduce to little more greater extent, not only that there will be a chance of implementing different logic circuits using reversible logic gates and which intern helps to increase the energy efficiency to the greater extent.

In reference [5] low power built-in-self (BIST) is implemented 32 bit Vedic multiplier. The objective of this fault coverage. Various methods of pattern generation are compared keeping in view of power consumption. In this test pattern generation the seed value is changed every 2 m cycles. For this purpose m bit binary counter & gray code generator is used. Signature analysis is done with the help of Multiple Input Signature Register (MISR). The signature of MISR will indicate whether the circuit under test (CUT), i.e. Vedic multiplier is faulty or not. The results are tabulated and compared. From the implementation results, the low power BIST shows, better power reduction than other methods. Simulation is carried out in Xilinx ISE and the design is implementation using Vertex 5 field Programmable Gate Array (FPGA). Fig. 5 presents the architecture of built-i-self based circuit.

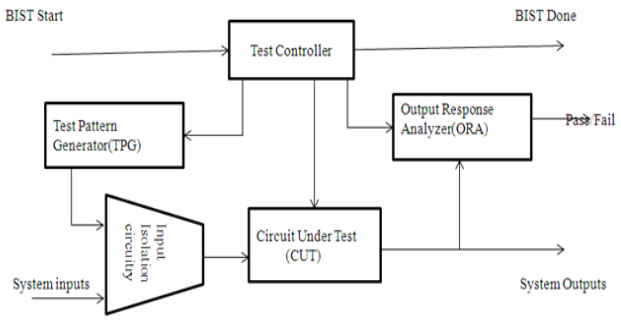

Fig 5 BIST architecture.

IV. CONCLUSION

The circuit proposed in [1] has 10 constant inputs, total number of 15 garbage outputs and 18 gates (consist of TR, BJN, NOT and N-bit Controlled NOT gate). 38 is the quantum cost of this reversible comparator. In future, the optimized circuits can be designed with decreased number of constant inputs; number of garbage outputs and, quantum cost as compared with prior designs. This reversible circuit is useful for nanotechnology, quantum computing and low power design.

REFERENCES

[1] Soolmaz Abbasalizadeh, Behjat Forouzandeh, and Hossein Aghababa, "4 Bit Comparator Design Based on Reversible Logic Gate". Lecture Notes on information Theory Vol. I, No. 3, September 2013.

[2] Rakshith Saligram and Rakshith T.R., "Design of Low Logical Cost Adders using Novel Parity Confirming Toffili Gate". IEEE Conference C2SPCA, 2013.

[3] Bahram Dchghan I, Abdolreza Roozbeh and Jafar Zone "Design of low power comparator using DG Gate", Scientific Research- Circuits and Systems, Vol. 5 p.p. 7-12, January 2014.

[4] Mr.M. Saravanan and Dr. K. Suresh Manic, "Energy Efficient Code Converters using Reversible Logic Gates". IEEE International Conference on Green High Performance Computing March, 2013.

[5] V.K. Kirthi and Dr. G. Mamatha Samson "Design of BIST with Low Power Test Pattern Generator" IOSR Journal of VI.SI and Signal Processing (IOSR-JVSP), Vol.-4 Issue-5. pp.30-39. Sep-Oct. 2014.

[6] Harpreet Singh and Chakshu Goel, "Design of a Power Efficient Reversible Adder-Subtractor", International Journal of Advanced Research in Computer Engineering and Technology, Vol-4 No-4, pp-1305-1308, April 2015.

[7] Dibal P.Y., "Design of a 4-bit Magnitude Comparator using Simulink", Arid Zone Journal of Engineering, Technology and Environment, Vol-9 No-16, pp-9-16, August 2013.

[8] Shivanappa Mantur, Chidanand Murthy M. V., M. Z. Kurian and H.S. Guruprasad, "Design of 4x4 Reversible Square Quantum Circuitry", International Journal of Emerging Technology in Computer Science and Electronics, Vol-14 No-2, pp-886-890, April 2015.

[9] Diganta Sengupta, Mahamuda Sultana and Atal Chaudhuri, "Realization of a Novel Reversible SCG Gate and its Application for Designing Parallel Adder-Subtractor and Matched Logic", International Journal of Computer Applications, Vol-31 No-9, pp-30-35, October 2011.

[10] Sravanth and T. Venkata Lakshmi, "VLSI Implementation of ALU using Reversible Logic with Vedic Mathematics", International Journal of Scientific Engineering and Technology Research, Vol-4, No-1, pp-142-146, January 2015