ENCHANCE DESIGN OF SINGLE PHASE H-BRIDGE MULTILEVEL INVERTER

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Abstract: The power electronics device which converts DC power to AC power at required output voltage and frequency level is known as inverter. The voltage source inverters produce an output voltage or a current with levels either 0 or +ve or-ve V dc. They are known as two-level inverters. Multilevel inverter is to synthesize a near sinusoidal voltage from several levels of dc voltages. Multilevel inverter has advantage like minimum harmonic distortion. Multi-level inverters are emerging as the new breed of power converter options for high power applications. They typically synthesize the stair –case voltage waveform (from several dc sources) which has reduced harmonic content. In this project work hardware model of Three-level single phase cascade H-Bridge inverter has been developed using MOSFETS. Gating signals for these MOSFETS have been generated by designing comparators. In order to maintain the different voltage levels at appropriate intervals, the conduction time intervals of MOSFETS have been maintained by controlling the pulse width of gating pulses by varying the reference signals magnitude of the comparator. The results of hardware are compared with simulation results. Simulation models designed in SIMULINK have been developed up to five levels and THD in all the cases have been identified.

keyword; Multilevel inverter; H-Bridge, MOSFETS; THD.

1. INTRODUCTION

In high power systems, the multilevel inverters can appropriately replace the existing system that uses traditional multi-pulse converters without the need of the transformers . All the three multi-level inverter topologies can be used in reactive power compensation without having the voltage unbalance problem. With the help of a transformer having one primary winding and several secondary windings, the cascade Hbridge configuration can be used in back-to-back intertie application. Also the structure of separate dc sources is well suited for various renewable energy sources such as fuel cell , photovoltaic , biomass etc. It may be easier to produce a high power, high voltage inverter with the multilevel structure because of the way in which device voltage stresses are controlled in the structure. Increasing the number of voltage levels in the inverters without requiring higher ratings on the individual devices can increase the power rating. The unique structure of Multi-level voltages sources inverters allow them to reach high voltages with low harmonics without the use of transformer or series connected synchronized switching devices. As the number of voltage levels increases , the harmonic content of output voltage waveform decreases significantly.

2. MULTI-LEVEL INVERTERS

The last structure introduced in this paper is a multilevel inverter, which uses cascaded inverters with separate dc sources (SDCSs). The general function of this multilevel inverter is the same as that of the other two previous inverters. The multilevel inverter using cascaded-inverter with SDCSs synthesizes a desired voltage from several independent sources of dc voltages, which may be obtained from either batteries, fuel cells, or solar cells. This configuration recently becomes very popular in ac power supply and adjustable speed drive applications. This new inverter can avoid extra clamping diodes or voltage balancing capacitors. A single-phase m-level configuration of such an inverter

The ac terminal voltages of different level inverters are connected in series. By different combinations of the four switches, S_1-S_4, each inverter level can generate three different voltage outputs, $+V_{dc}$, $-V_{dc}$, and zero. The ac output of each of the different level of full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. Note that the number of output phase voltage levels is defined in different way from those of two previous inverters. In this topology, the number of output phase voltage levels is defined by $m = 2s+1$, where s is the number of dc sources.

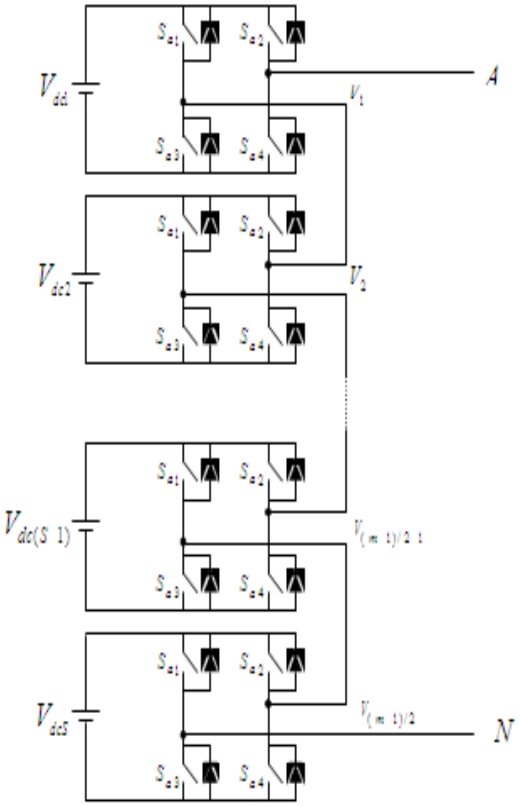

Figure 1.Single-phase structure of a multilevel cascaded inverter.

3. MULTILEVEL INVERTER IMPLEMENTATION

A 7-level cascaded-inverters based inverter, for example, will have three SDCSs and three full-bridge cells. Minimum harmonic distortion can be obtained by controlling the conducting angles at different inverter level, r a three-phase system, the output voltage of the three cascaded inverters can be connected in either wye or delta configuration. For example, a wye-configured m-level inverter using cascaded-inverters with s separated capacitors A 7-level cascaded-inverters based inverter. Minimum harmonic distortion can be obtained by controlling the conducting angles at different inverter level. For a three-phase system, the output voltage of the three cascaded inverters can be connected in either wye or delta configuration. For example, a wye-configured m-level inverter using cascaded-inverters with s separated capacitors.

4.COMPARISON WITH CONVENTIONAL SYSTEMS

	3rdharmonic Content	5thharmonic content	7thharmonic content	9thharmonic content	Total Harmonic Distortion
Single phase Full Bridge	24.4	1.065	10.62	12.59	0.5605
Single phase Three level	-99.69	-99.69	-99.69	-99.69	0.3831
Single phase Four level	4.318e-009	4.318e-009	4.318e-009	4.318e-009	0.3443
Single phase Five level	17	10.66	5.436	9.385	0.2979

Figure 2. The 3rd, 5th , 7th and 9th harmonic

From the above table we can observe that the harmonic content as well as the Total Harmonic Distortion (THD) factors gets reduced as the number of levels increased in a Single phase H-Bridge Multi-level inverter . This leads to a better and sinusoidal voltage waveform. We can also observe the great reduction of harmonic content in three-level HBridge inverter.

4.EXPERIMENTAL VERIFICATION AND RESULTS

To verify the simulating , a multilevel inverter circuit is implemented. The schematic of a 3-phase 7-level cascaded inverter with SDCSs, which is used to verify the simulation results.

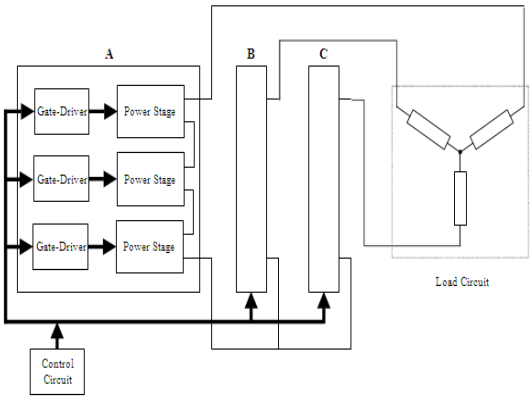

Figure 3. Schematic of a 3-phase 7-level cascaded inverter circuit used to verify the simulated results.

1) The control circuit

An AT89C51 microcontroller is used as the main processor, which provides the gate logic signals. A gate signal is latched by a D-Type Flip-Flops. In the circuit, a 74LS374 is used to latch 8 gate signals.

2) The gate-driver circuit

HP 316J is used as a gate-driver, which receives a TTL logic signal from the microcontroller and provides +15 V for turn on gate single and –5 V for turn off gate signal to drive a switch.

3) The power stage

In a power stage, four IGBT, HGT30N60B, are used as the main switches, which are connected in full-bridge configuration. Each power stage is supplied by a variable dc source. The rated output power is 1.8 kW.

4) The load circuit

In each phase, a 50 resistor and a 10 mH inductor are connected in series. To control gate signals, the command program, which is implemented in assembly language, is generated on a personal computer and then transferred to the microcontroller on the control circuit board.he output waveforms are measured by LeCroy LC534AL. The frequency spectrum are measured by an oscilloscope, HP35665A and are plotted by a graphics plotter, HP7550A.

The output obtained is viewed in the CRO. The cascaded h-bridge model is used for obtaining the three level because of the advantages over the other two designs as discussed before. we also present the pictures of the waveforms obtained. The basic idea of controlling the output voltage magnitude of inverter by using microcontroller technique is, changing the width of pulses by varying a magnitude of reference wave. The multilevel inverter topology can overcome some of the limitations of the standard two-level inverter. Output voltage and power increase with number of levels. Harmonics decrease as the number of levels increase.

In the paper, several multilevel voltage source inverters and their modulation topologies are introduced. The cascaded-inverter with separated dc sources is discussed in detail with experimental results to verify the proposed concepts.

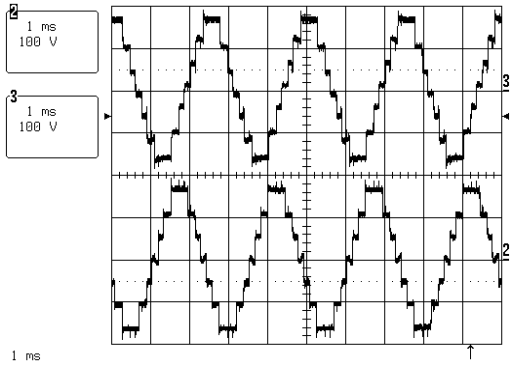

Figure 4. The 3-phase 7-level cascaded inverter with M = 1 and f = 400Hz.

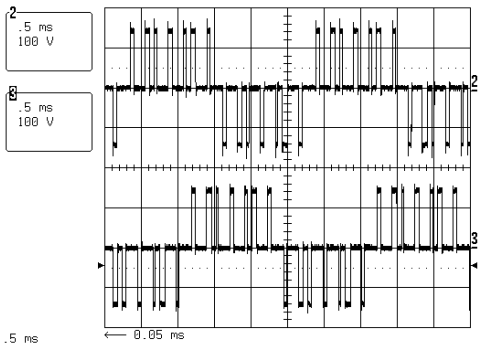

Figure 5. The 3-phase 7-switching angle SHE PWM with M = 0.55 and f = 400Hz.

A high speed digital signal processing need to be used as a processor in future work. In the experimental, the approximated switching angles are programmed instead of the precise ones because of the speed of the

microcontroller is not high enough. Therefore, the asymmetric output waveform is introduced.

5. CONCLUSIONS

We hereby conclude that Multi-level inverters is a very promising technology in the power industry. In this project, the advantages and applications of Multi-Level Inverters are mentioned and a detailed description of different multi-level inverter topologies is presented. Single Phase H-Bridge Inverter & Three Phase H-Bridge Inverters functioning is realized virtually using MATLAB SIMULINK. A detailed Multi-Level Inverter is presented from which we concluded that the harmonic content is greatly reduced in Multi-Level Inverter. A single phase Cascade H-Bridge Inverter is designed and implemented practically. The components used in the practical implementation of H-Bridge Inverter are described in detail.

REFERENCE

[1] "Power Electronics Circuits, Devices & Applications" , Muhamma H. Rashid, Third Edition, Prentice Hall India.

[2] "Linear Integrated Circuits", D.roy Choudary, Shail B.Jain, Second Edition, New Age International Publishers.

[3] "Multi-level Converter-A New Breed of Power Converters**",** Jih-Sheng Lai and Fang Zheng Peng, IEEE Trans. Ind, Applicant Vol.32

[4] "Opamps & Linear Integrated Circuits" , Ramakanth Gayakward, PHI Publications.

[5] "Power Electronic for Technology", Ashfaq Ahmed, PEARSON Education.

[6] R. W. Menzies, P. Steimer, J. K. Steinke, "Five-Level GTO Inverters for Large Induction Motor Drives," IEEE Transactions on Industry Applications, Vol.30, No.4, Jul./Aug., 1994, pp.938-944.

[7] H. Johan, Frederik S. Van Der Merwe, "Voltage Harmonics Generated by Voltage- Fed Inverters Using PWM Natural Sampling," IEEE Transactions on Power Electronics, Vol.3, July, 1988, pp.297-302.

[8] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, G. Sciutto, "A New Multilevel PWM Method: A heoretical Analysis," in Proc. IEEE Power Electron. Specialist Conf. (PESC), June, 1990, pp.363-371.