SIMULATION DESIGN ANALYSIS AND IMPLEMENTATION OF DLL USING SCALABLE C5 CMOS PROCESS FOR CLOCK GENERATION

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Abstract*—PLLs are widely used in modern signal processing and communication systems, and it is expected that PLL will contribute to improvement in performance and reliability of future communication systems. The applications of PLLs include filtering, frequency synthesis, motor speed control, frequency modulation, demodulation, signal detection, frequency tracking and many other applications. The PLL consists of three main blocks VCO, Loop Filter and Phase detector. Most versatile application for digital phase locked loops is for clock generation and clock recovery in any complex computer architecture like a microprocessor or microcontroller, network processors. Digital Phase locked loops are commonly used to generate timingon chip clocks in high performance mixed signal analog and digital systems. Most of the systems employ digital PLL mainly for synchronization, skew and jitter optimization. Because of the need of high speed circuitry there is a need of PLL. Mostly communication, wireless systems, RF Processors operate in Gigahertz range, there is a necessity of PLL that too digital which operate in high order frequencies. Digital PLL is a mixed signal integrated circuit and presented work focuses on design and analysis of efficient digital phase locked loops for clock generation using c5 SPICE models. The presented design Digital PLL performs the function of mainly generatinga clock signal also consists of design of sub circuits and systems like phase detector, loop filters and voltage controlled oscillators. A detailed FFT analysis is also presented with parameters magnitude, phase and group delay calculated for each sub circuits and systems. The results of DPLL designed using proper optimization method is also compared with traditional method.

***IndexTerms*—Digital PLL, SPICE, VCO, Phase Detector, FFT, Loop filters**

INTRODUCTION

The objective of the paper is to present design an All Digital Phase Locked Loop (DPLL) with low power using C5 process technology for CMOS[1]. The design consists of three main blocks: Voltage Controlled Oscillator (VCO), Frequency Phase Detector (PFD) and Loop Filter (LF) or frequency divider network. The VCO is considered as the heart of the DPLL as it consumes the most power for the whole system. The design went through different approaches, standard cells and custom cells based design and simulation for the same .This design can be used in Clock generation and Data Recovery (CDR) system as an application. Digital Phase locked loop is a mixed signal analog integrated circuit. Digital PLL is the heart of many communication as well as electronic systems. Mostly a higher lock PLL range with lesser locking time and should have tolerable phase noise. The most versatile application of a digital PLL is for clock generation or synchronization, clock recovery, communication systems and frequency synthesizers. In high performance digital systems like processors digital PLL or DPLL are commonly used to generate well timed on chip clock signals[4,5]. Modern RF circuits or wireless mobile communication systems use PLL for synchronization, timing based synthesis, skew and jitter reduction. Digital PLL is extensively used in advanced communication systems, electronic and medical instrumentation systems. The PLLs are an integrated part of larger circuits on a single chip.

A simple PLL consists of namely four to five integrated blocks. They are phase frequency detector, charge pump, Loop filters, voltage controlled oscillator and frequency dividing circuits.

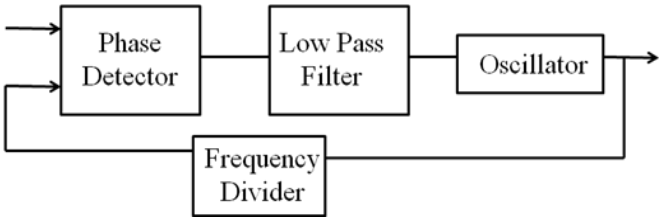

Figure 1 : Basic Block diagram of a Digital Phase locked loop

Today in terms of high frequency usage in mixed signal analog integrated circuits deploy PLLs of faster locking abilities. In this paper the faster locking of PLL is particularly concentrated with respected to 50 nm process technology[4]. The design and simulation results are based on cmos models using the same process technology. Digital PLL takes in to account suitable circuit architectures and associated parameters. The optimization of the Voltage controlled oscillator is also carried out using simple CMOS and current starved CMOS inverters to get a better frequency precision.

DESIGNING A DIGITAL PLL

A PLL is a closed-loop feedback system that sets fixed phase relationship between its output clock phase and the phase of a reference clock. A PLL is capable of tracking the phase hanges that falls in this bandwidth of the PLL. A PLL also multiplies a low-frequency reference clock CKref to produce a high-frequency clock CKout this is known as clock synthesis. A PLL has a negative feedback control system circuit. The main objective of a PLL is to generate a signal in which the phase is the same as the phase of a reference signal. This is achieved after many iterations of comparison of the reference and feedback signals. In this lock mode the phase of the reference and feedback signal is zero. After this, the PLL continues to compare the two signals but since they are in lock

mode, the PLL output is constant. A basic PLL is a negative feedback system that receives an incoming oscillating signal and generates an output waveform that exerts the same phase,frequency relationship as the input signal. This is achieved by constantly comparing the phase of output signal to the input signal with a phase frequency detector (PFD)[12,13].

The Phase frequency Detector (PFD) is one of the main parts in PLL circuits. It compares the phase and frequency difference between the reference clock and the feedback clock. Depending upon the phase and frequency deviation, it generates two output signals UP and DOWN. The Charge Pump (CP) circuit is used in the PLL to combine both the outputs of the PFD and give a single output. The output of the CP circuit is fed to a Low Pass Filter (LPF) to generate a DC control voltage. The phase and frequency of the Voltage Controlled Oscillator (VCO) output depends on the generated DC control voltage. If the PFD generates an up signal, the error voltage at the output of LPF increases which in turn increase the VCO output signal frequency. On the contrary, if a Down signal is generated, the VCO output signal frequency decreases. The output of the VCO is then fed back to the PFD in order to recalculate the phase difference, and then we can create closed loop frequency control system[4,5,12].

PLL ARCHITECTURE[6,8]

Following is the description of basic components of PLL
1. Phase Detector or Phase Frequency Detector (PD or PFD)
2. Charge Pump (CP)
3. Low Pass Filter (LPF)
4. Voltage Controlled Oscillator (VCO)
5. Divide by N Counter

Phase Detector
A phase detector or phase comparator used within a PLL phase locked loop produces an error voltage between the reference signal and VCO to keep the VCO on the required frequency. The phase detector is the core element of a phase locked loop, PLL. Its action enables the phase differences in the loop to be detected and the resultant error voltage to be produced.
Pass Filter
A LPF is a filter that passes signals with frequency lower than a certain cuttoff frequency and attenuates signals with frequencies higher than the cutoff frequency. The amount of attenuation for each frequency depends on the filter design.
Voltage Controlled Oscillator
In PLL applications, the VCO is treated as a linear, time-invariant system. Excess phase of the VCO is the system output. The VCO oscillates at an certain angular frequency, Its frequency is set to a nominal frequency when the control voltage is zero. Frequency is assumed to be linearly proportional to the control voltage with a gain coefficient.
Frequency Divider
A frequency divider, also called a clock divider or scaler or prescaler, is a circuit that takes an input signal of a frequency, and generates an output signal of a frequency: where is an integer.

Types of PLL
The three types of PLL circuit are there as shown in below figure

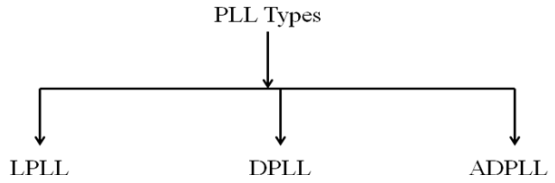

Figure 1.2 PLL Types

There are many types of PLL according to the internal blocks and designing techniques as following:
1. LPLL: Linear Phase Locked Loop which contains a VCO and RC circuit for the Loop Filter block and uses a multiplier to detect the phase difference between the reference frequency and the VCO output frequency.
2. DPLL: Digital Phase Locked Loop was the very first digital PLL; it was in effect a hybrid device ONLY the phase detector was built as a digital block like EXOR.
3. ADPLL: All Digital Phase Locked Loop in which all the blocks are built as digital blocks.

PLL in general has its own parameters such as:
The operating frequency range: the range of frequencies that PLL can lock on them. The lock time: the time which PLL needs to lock on the reference frequency. The Jitter: undesired deviation from the true periodicity of an assumed periodic signal. In general a PLL consists of five main blocks:

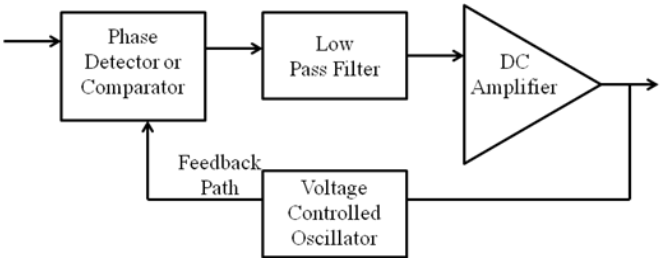

Figure 2 A generic architecture of Digital PLL

3.1 Phase frequency Detector
The phase frequency detector is one of the main integral parts of PLL circuits. It compares the phase and frequency difference between the reference clock and feedback clock. Depending upon the phase and frequency deviation it generates two output signals Up and Down. If there is a phase difference between the two signals, it will generate UP or DOWN synchronized signals. When the reference clock rising edge leads the feedback input clock rising edge UP signal goes high while keeping “DOWN” signal low. On the other hand if the feedback input clock rising edge leads the reference clock rising edge “DOWN” signal goes high and “UP” signal goes low. Fast phase and frequency acquisition PFDs are generally preferred over traditional PFD.

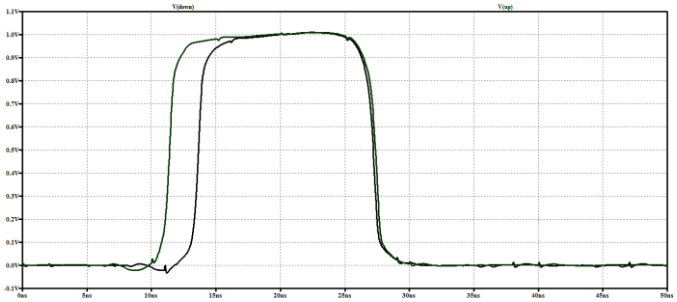

Figure 3 Simulation plot for Up and Down signals in PFD

3.2 Charge Pump and Loop Filter

Charge pump circuit is an important block of the whole PLL system.It converts the phase or frequency difference information into a voltage, used to tune the VCO. Charge pump circuit is used to combine both the outputs of the PFD and give a single output which is fed to the input of the filter.

3.3 Voltage Controlled Oscillator

An oscillator is an autonomous system which generates a periodic output without any input.The most popular type of the VCO circuit is the current starved voltage controlled oscillator (CSVCO). Here the number of inverter stages is varied, generically used with 21 stage with simple inverter or current starved configurations

3.4 Frequency Divider

The output of the VCO is fed back to the input of PFD through the frequency divider circuit. The frequency divider in the PLL circuit forms a closed loop. It scales down the frequency of the VCO output signal. A simple flip flop (FF) acts as a frequency divider circuit. The schematic of a simple divider based divide by 2 frequency circuit is shown in the Figure

DESIGN AND SYNTHESIS OF DPLL

The schematic level design entry of the circuits is carried out in the Electric CAD VLSI Design Environment. The structure of the DPLL is designed in Electric CAD using C5 SPICE models for CMOS provided by MOSIS. In order to analyze the performances, these circuits are simulated in the LTSPICE simulator of Level 3 or 4 BSIM SPICE CAD . Different performance indices such as phase,group delay and corresponding magnitude are measured in this environment. Transient parametric sweep and phase analyses are carried out in this work to find out the performances of the circuit. The optimization of the current starved VCO circuit, the scale factor for transistor sizing is found out using the LTSpice environment.

Following Design procedure is adopted for the presented design[6,8]

1. VCO Design
2. PFD Loop Design
3. Frequency Divider Circuit
4. Loop Filter and Charge Pump Design
5. Assembling all subunits in a single design
6. Carry out transient analysis
7. FFT analysis
8. Tabulation for simulation parameters

SIMULATION RESULTS

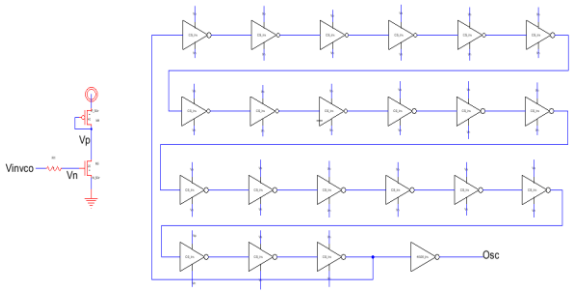

Figure 4 Schematic for VCO using simple CMOS inverter using c5 process

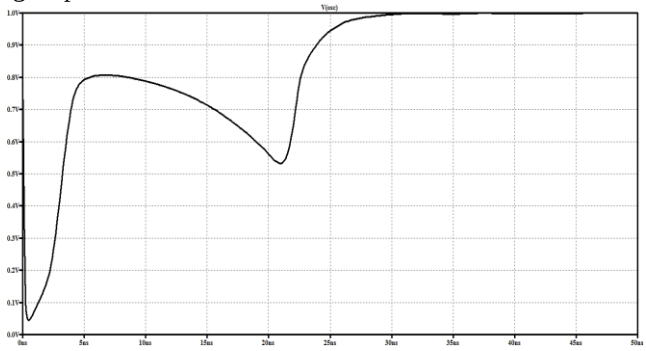

Figure 5Transient plot for VCO using simple inverter for C5 process

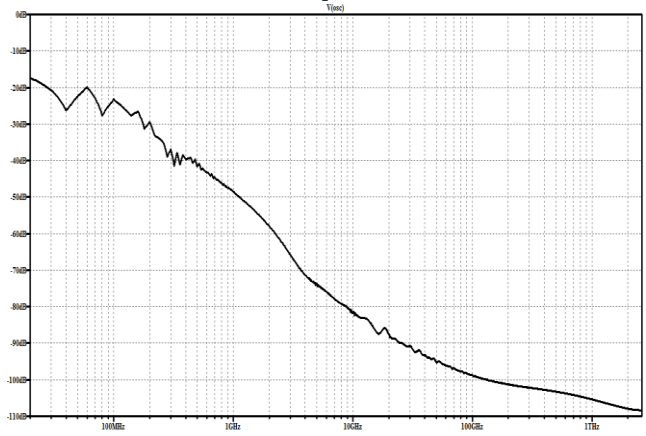

Figure 6FFT plot for VCO using simple inverter

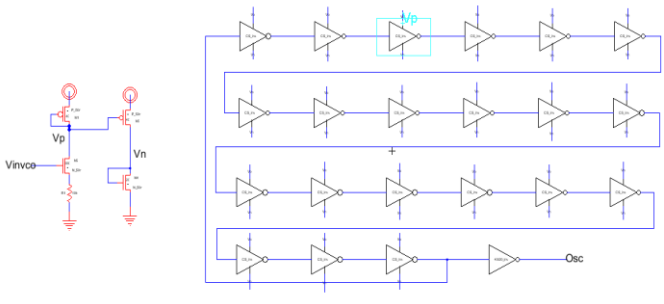

Figure 7 Schematic for VCO using current starved CMOS inverter using C5 process

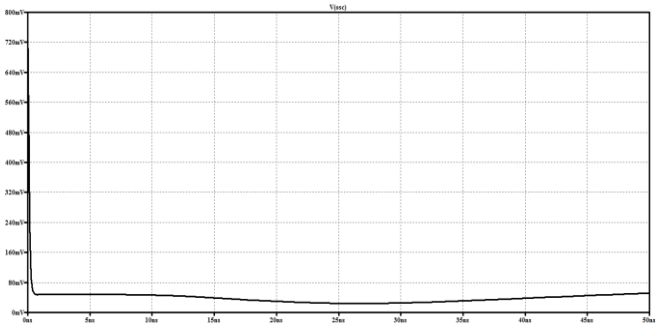

Figure 8 Transient plotfor VCO using current starved CMOS inverter

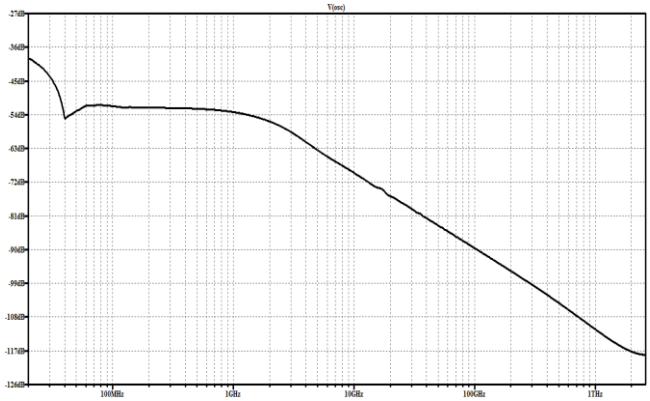

Figure 9 FFT plot for VCO using current starved CMOS inverter

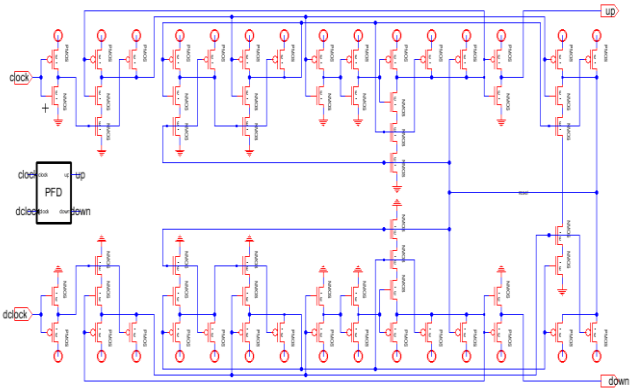

Figure 10 schematic for PFD

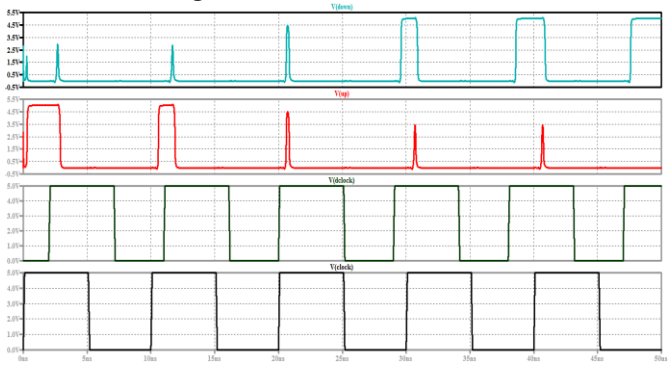

Figure 11 Simulation plot for Vclock, data up and Down for PFD

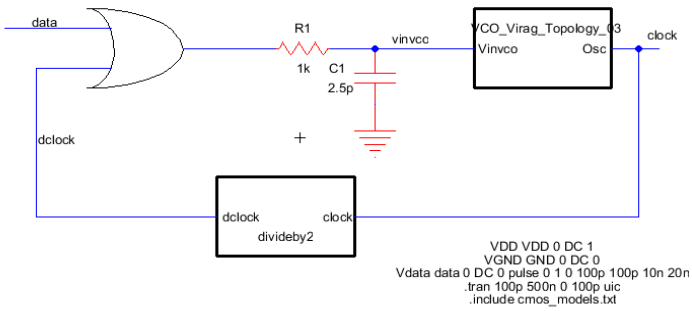

Figure 12 Schematic plot for DPLL topology 1

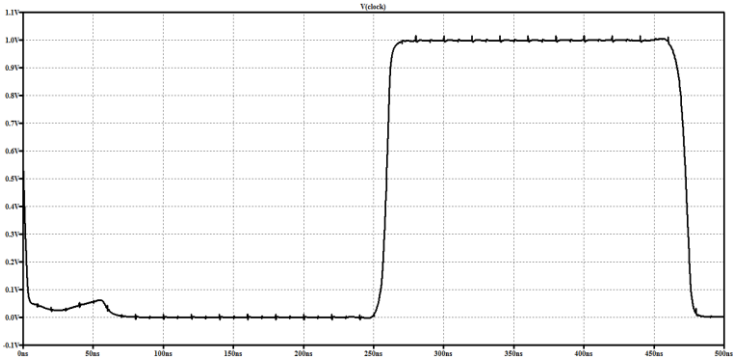

Figure 13 Transient simulation plot for Vclock

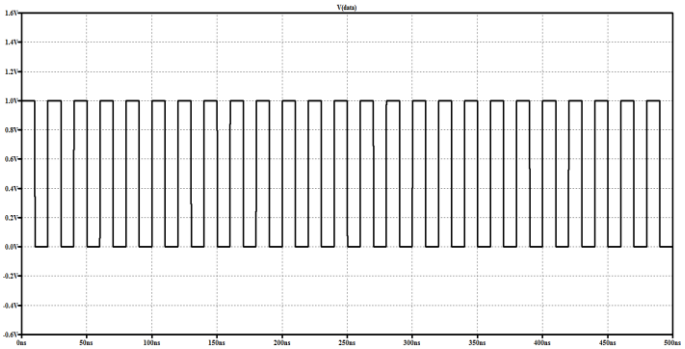

Figure 14 Transient simulation plot for Vdata

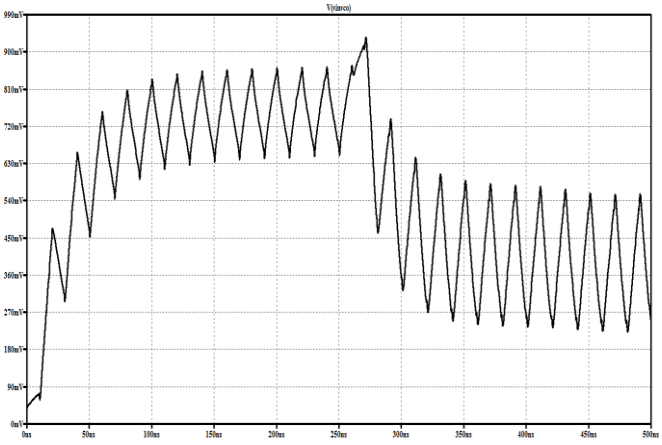

Figure 15 Transient simulation plot for Vinvco

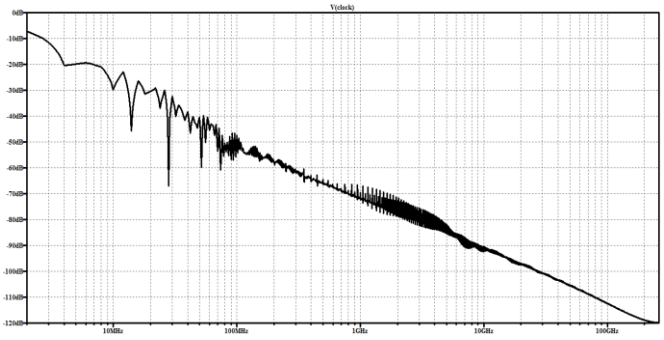

Figure 16 FFT plot for Vclock in VCO Topology1

The presented designs Digital PLL performs the function of mainly generating a clock signal also consists of design of sub circuits and systems like phase detector, loop filters and voltage controlled oscillators. A detailed FFT analysis is also presented with parameters magnitude, phase and group delay calculated for each sub circuits and systems. The results of DPLL designed using proper optimization method is lsocompared with traditional method.

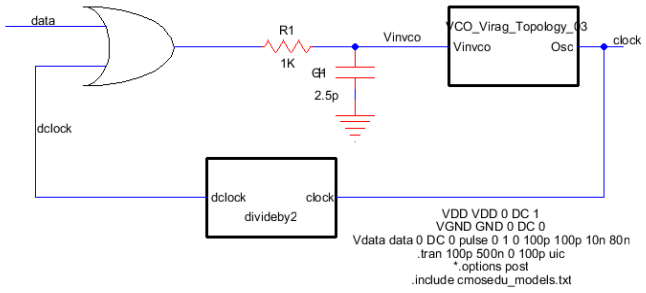

Figure 17 Schematic plot for DPLL topology 2

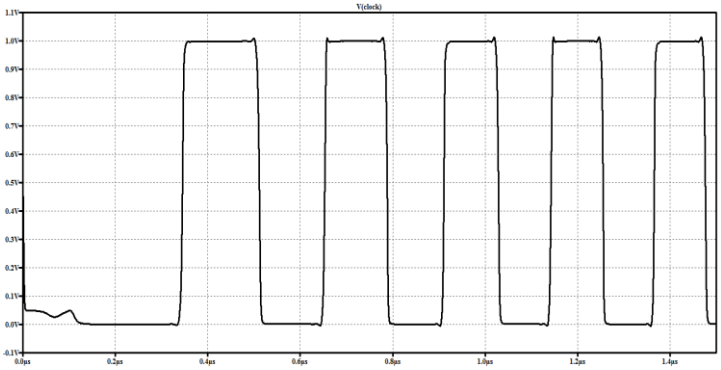

Figure 18 Transient simulation plot for Vclock

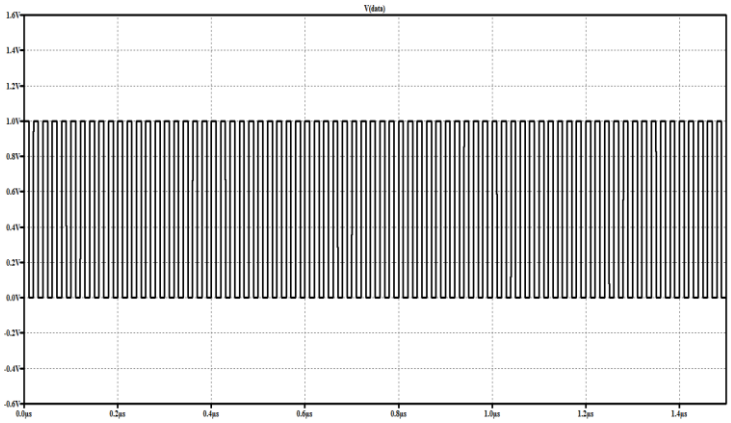

Figure 19 Transient simulation plot for Vdata

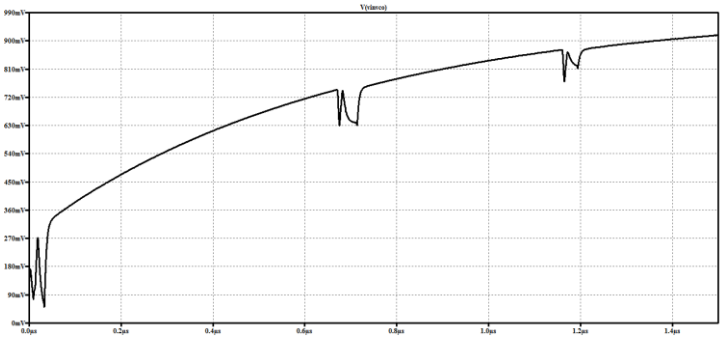

Figure 20 Transient simulation plot for Vinvco

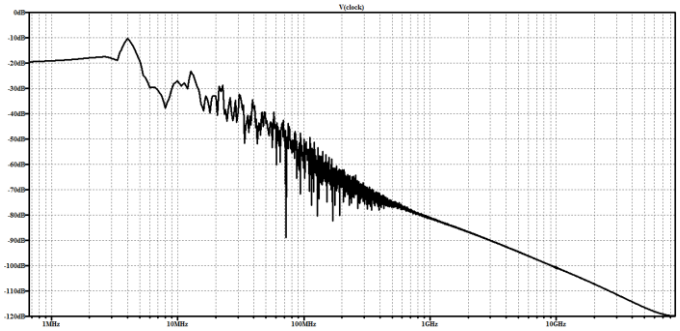

Figure 21 FFT plot for Vclock in DPLL topology 2

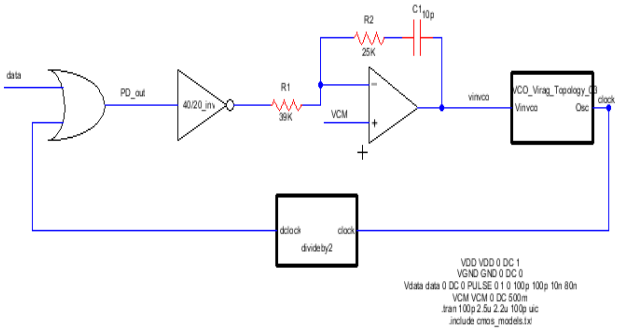

Figure 22 Schematic view for DPLL 3

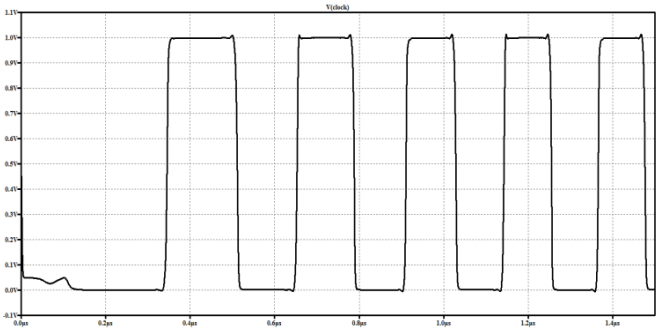

Figure 23 Transient simulation plot for Vclock

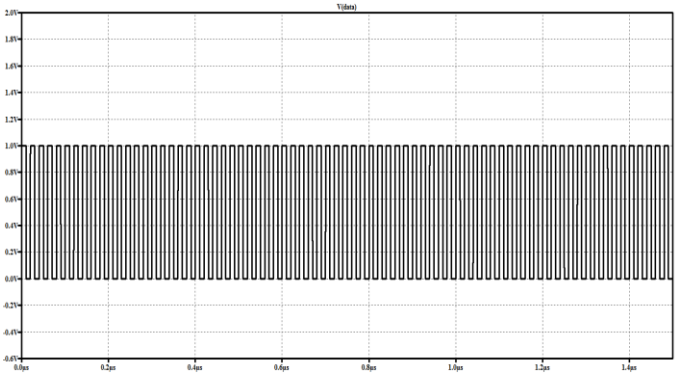

Figure 24 Transient simulation plot for Vdata

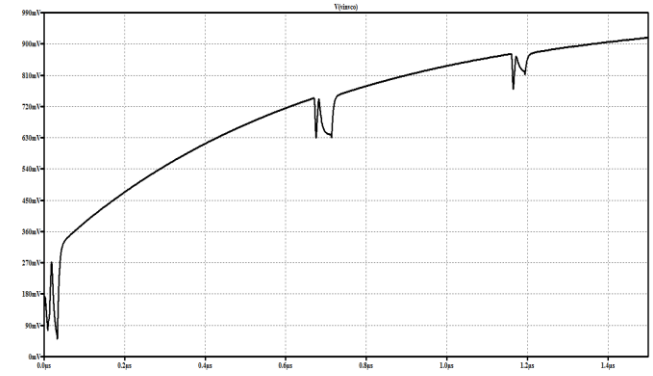

Figure 25 Transient simulation plot for Vinvco

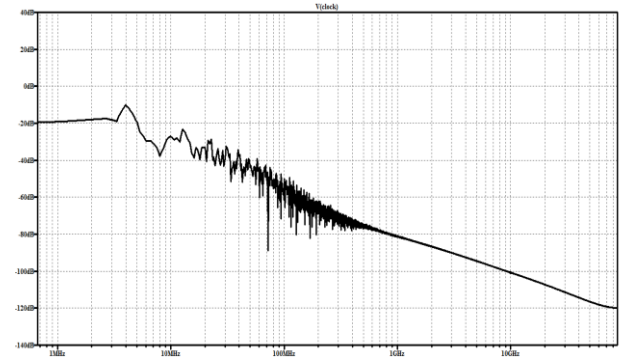

Figure 26 FFT plot for Vclock in DPLL topology 3

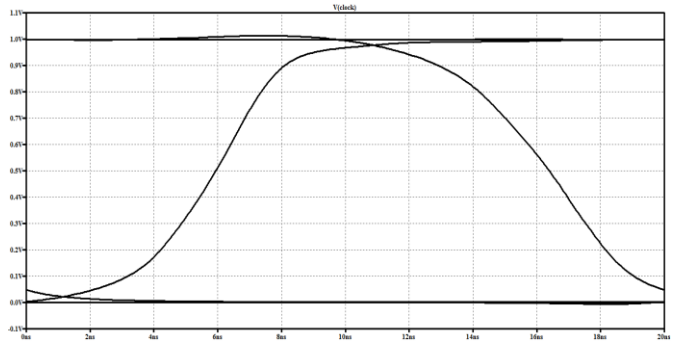

Figure 27 Transient Plot or Eye Diagram for Vclock in DPLL Topology

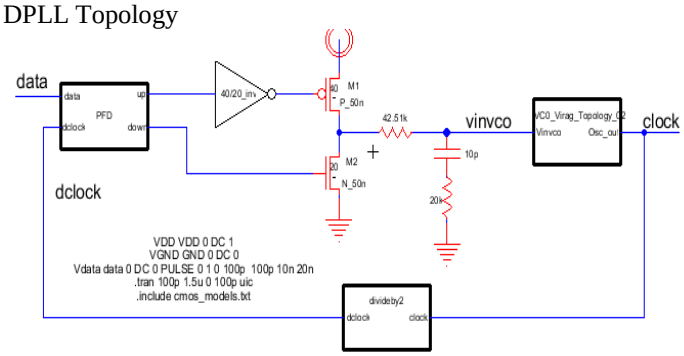

Figure 28 Schematic view for DPLL Topology 4

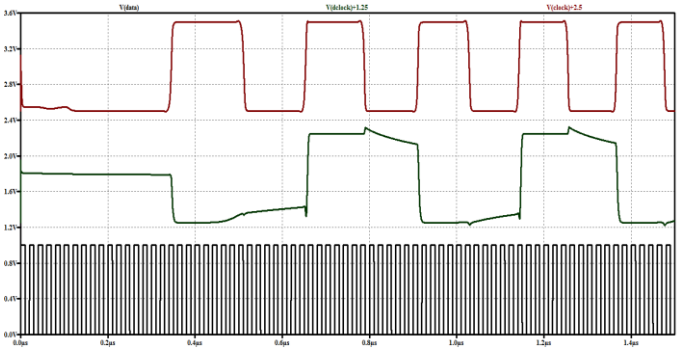

Figure 29 Transient plot for Vdata and Vclock in DPLL topology 4

FFT RESULTS

Table 1

FFT analysis for DPLL Topology 1

Frequency	Magnitude	Phase	Group Delay
1MHz	-18.61 dB	108.17°	45.00 ns
10 MHz	-33.76 dB	97.91 °	-23.47 ns
100 MHz	-56.09 dB	84.21°	25.44 ns

1 GHz	-76.73 dB	91.16 °	410.24 ns
10 GHz	-96.53 dB	101.66	138.57ps
100 GHz	-111.58 dB	166.58	1.33 ps

Table 2
FFT analysis for DPLL Topology 2

Frequency	Magnitude	Phase	Group Delay
1MHz	-17.26 dB	33.049°	-135.37 ns
10 MHz	-21.528 dB	-162.89	70.007 ns
100 MHz	-37.77dB	70.83°	-34.17 ns
1 GHz	-62.43 dB	104.72°	-3.721 ns
10 GHz	-89.74dB	92.15°	-1.594ns
100 GHz	-108.80dB	111.30°	552.79ps

Table 3
FFT analysis for DPLL Topology 3

Frequency	Magnitude	Phase	Group Delay
1MHz	-19.82 dB	109.74°	17.85 ns
10 MHz	-37.42 dB	104.85°	48.016 ns
100 MHz	-56.21 dB	92.41°	-37.87 ns
1 GHz	-78.79 dB	91.68°	-3.414 ns
10 GHz	-98.53 dB	105.14°	-78.45ns
100 GHz	-111.30 dB	179.99°	-3.620 ns

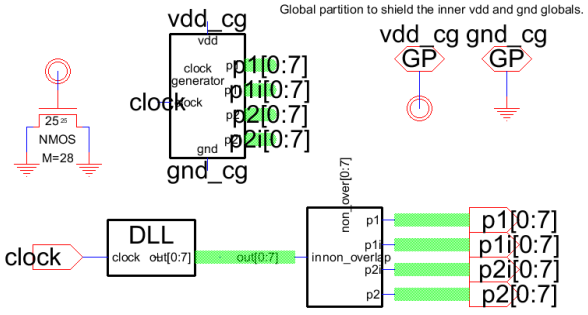

Figure 30 Schematic of DLL Clock generator

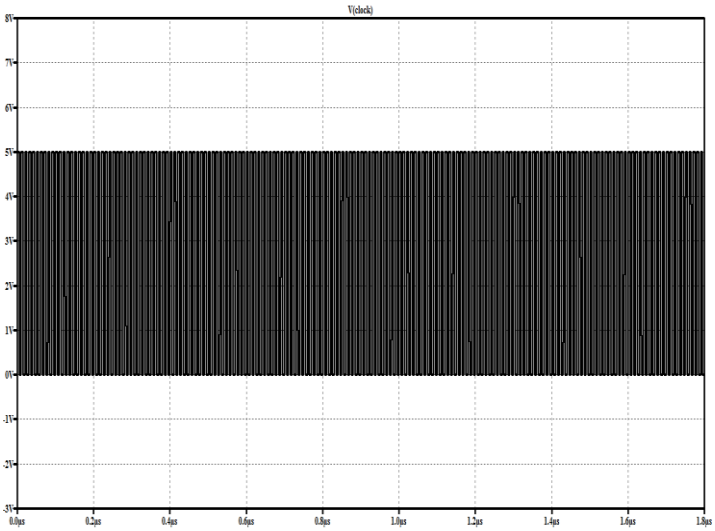

Figure 31 Simulation Plot for Vclock Signal in DLL Clock generator

I. CONCLUSION

In this paper In this work presented DPLL works with better locking times, the digital PLL consumes low power as designed with 50 nm CMOS technology, the transient analysis mainly depends on the type of the PFD architecture used and parasitic parameters utilized for charge pumps and loop filters. So by properly choosing VCO architecture, PFD design and adjusting the charge pump configurations. Designing Phase locked Loops consisting of determining specifications selecting device sizes and relatively biasing conditions. The DPLL can be compensated for stability by simulating various properties. For this first a selection is made for the active device used. Four different topologies of different voltage controlled oscillators are analyzed for various transients and FFT responses are calculated for frequencies ranging from 1MHz to 25 MHz . For mentioned topologies of DPLL the integrated units such as Phase frequency detector, Loop filter operational amplifier are designed The development of a design procedure provides a quick, well integrated and effective mechanism for estimation and calculation of various parameters. The steps highlighted make it easy to redesign the circuit for various set of specifications. The simulated results of the DPLL are in compliance with the theoretical values. Significant effort has been made in these designs has been put into integrating theory and practical illustrations using actual numbers and not just symbolic representations. A equivalent Netlist is also generated and the design can be ported to other simulation engines for better results and can be modified as well with respect to given process technology. While the presented work involved discrete circuit's components which won't provide an exact representation of the actual integrated circuit, they can provide actual insight to limitations of a particular design. The presented work can also be used to get acquainted with the test equipment and possible loading might be introduced into circuit at the time of testing and verification as well.

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