ADDER DESIGN METHODOLOGIES AND LIMITATIONS USING CMOS CIRCUITS : STUDY AND REVIEW

[1]Ashutosh Kumar Singh,[2]Dr. Manish Jain

[1]Research Scholar, VLSI Design,Department of Electronics and Communication Engineering, Sarvepalli Radhakrishnan University, Bhopal, Madhyapradesh, India
[2]Professor and Head, Department of Electronics and Communication Engineering,Sarvepalli Radhakrishnan University Bhopal, Madhya Pradesh, India
Email: [1]ashutosraj4ec@gmail.com, [2]manish_jain18@rediffmail.com

Abstract: **In this review paper different design techniques of multi bit adder are deliberate using linear parameters logic gates. The comparison is carried by several parameter mainly focus on a number of linear threshold gates, a number of CMOS transistor, power dissipation, power delay product (PDP), average power dissipation time delay and size of the full adder circuit. Adder circuits basically implemented using basic logic gates namely XOR and AND gates. Half Adders or Full adders may be realized in various ways depending on the various process technologies and design methodologies deployed for making these digital integrated circuits design. The Full adder, 14T, pseudo-nMOS, MULTIPLEXER-BASED FULL ADDER , 8T, Inverter-based full-adder with pass transistors, Conventional CMOS (C-CMOS), 20T,10Twith 4T-XNOR, 6T, 16T, 9T, Double gate MOSFET and hybrid 1-bit full adder full adders etc**

Keywords: CMOS, Adders, VLSI Design, CAD, process technology, delay analysis

I. Introduction

In this paper, a full adder designemploying both complementary metal–oxide–semiconductor(CMOS) logic and transmission gate logic is reported. The designwas reviewed firstly implemented for 1 bit and then extended for 32 bit also.The circuit was implemented using many professional VLSI CAD such as Cadence Virtuoso tools in 180-and 90-nm technology. Performance parameters such as power,delay, and layout area were compared with the existing designssuch as complementary pass-transistor logic, transmission gateadder, transmission function adder, hybrid pass-logic with staticCMOS output drive full adder, and so on. For low power voltage supply at process technology below 180-nm technology, the average power consumption few µWless than 10 µWwas found to be extremely low with moderately low delay less than 200 psresulting from the deliberate incorporation of very weak CMOSinverters coupled with strong transmission gates. Correspondingvalues of the same were 1.17664 µW and 91 The design wasfurther extended for implementing 32-bit full adder also, and wasfound to be working efficiently with only variable and contant delay logic styles and power tabulated at 180-nm (90-nm) technologyfor 1.8-V (1.2-V) supply voltage. In comparison with the existingfull adder designs, the present implementations were found to offersignificant improvement in terms of power and speed and overall performance as well.

With the advent of Very Large Scale Integration (VLSI), rapid advances took place in circuit integration technologies; the electronics industry has achieved a phenomenal growth overthe last two decades. Various applications of VLSI CMOS circuits in high-performance computing,telecommunications, and consumer electronics has been expanding progressively, and at avery hasty pace.Steady advances in semi-conductor technology and in the integration levelof Integrated circuits (ICs) have enhanced many features, increased theperformance,improved reliability of electronic equipment, and at the same time reduce the cost, powerconsumption and the system size.With the increase in the size and the complexity of the analog and digital systems, Computer Aided Design (CAD) tools are introduced into the hardwaredesign process.Design Methodologies are necessary for a systematic design. [1,8]The chip design process enforced the automation of process, automation of simulation based verification i.e. replacing of traditional breadboard techniques through HDL (hardware description language) development. The various modular hierarchical techniques of design created the scenario that CAD tools are inevitable [11].

II. VLSI Technology and Design

A VLSI System integrates millions and millions of electronic components in a small area. The main objective is to make the analog or digital system as compact as possible with the required functionalities. Tens and thousands of transistors are fabricated on a small piece of wafer. The circuits are tested and fabricated becauseonce an error is created the whole design is waste and it costs million and millions of dollars. Therefore CAD tools came into the picture. CAD tools are inevitable.[9] This chip design forced automation of process, automation of simulation based verification. This CAD assistance has lead to Electronic Design Automation.

III. Design Methods

Systematic design methods or the design methodologies are necessary for successfully designing complex digital hardware.
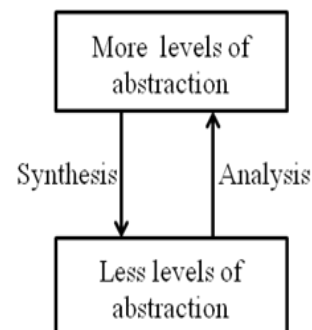

Figure 1 Abstraction Hierarchy for VLSI Adders 1

Our design methods usually differ by the number of abstraction levels and the complexities involved.
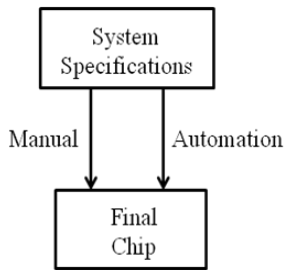
Figure 2 Abstraction Hierarchyof VLSI Adders 2

Comparing structurally different views of a VLSI Design include divide and conquer techniques which includes sorting by structure and sorting by issues. The design hierarchy that uses existing techniques has an unacceptable restriction that they use identical hierarchies. Structurally hierarchy transformation is the first step and hierarchy base comparison is the last step.
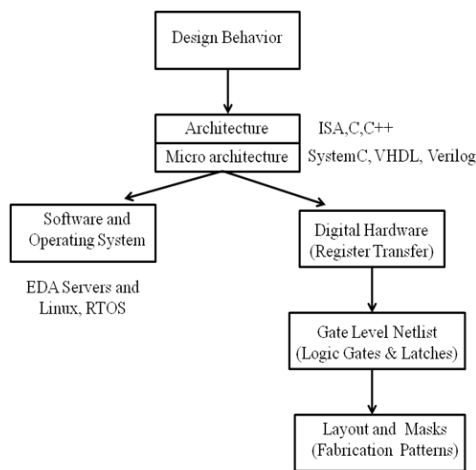

Figure 3 Design representation levels and formats associated

A. Structured Design Techniques
B. Programmable Logic Design
C. Gate Array and Sea of Gates Design
D. Cell Based Design
E. Full Custom and Semi custom Design
F. Platform based Design and SOC

IV. Adder Designs using various Technologies

There are numerous topologies and designs exist in literature. Few of them are as follows
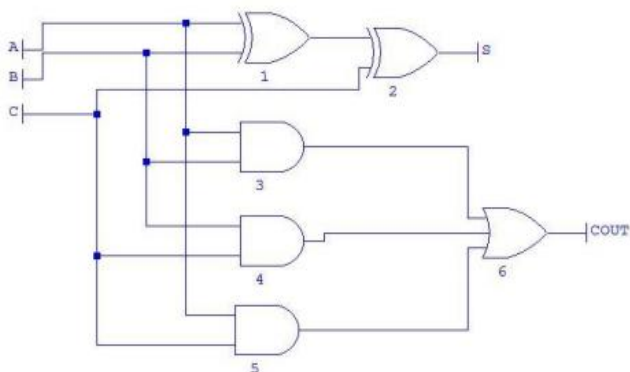

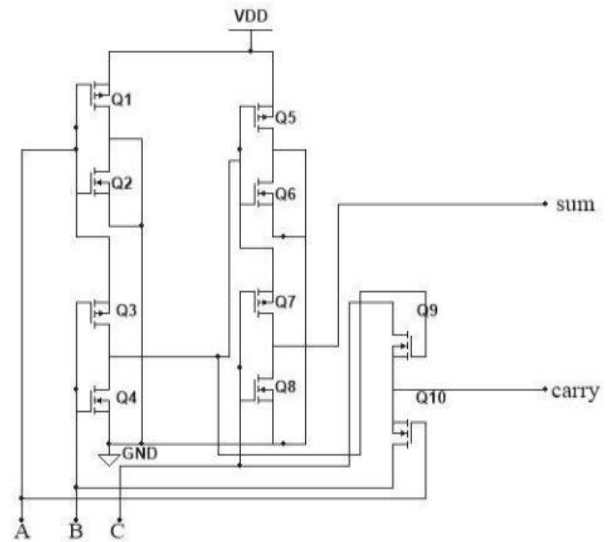Figure 4 Gated design for Adder Circuits
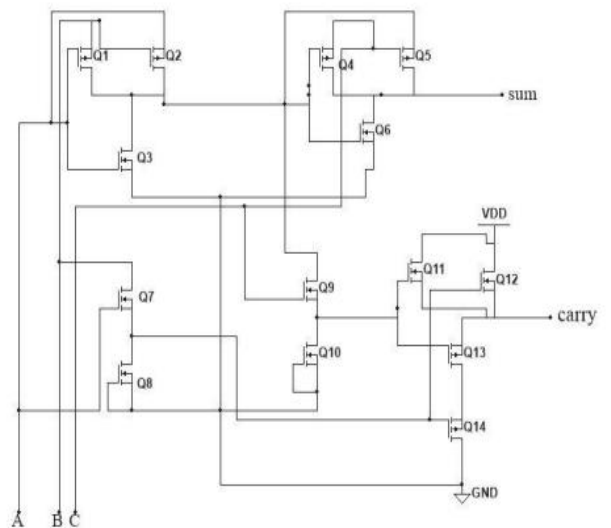

Figure 5 Schematic for SERF Adder
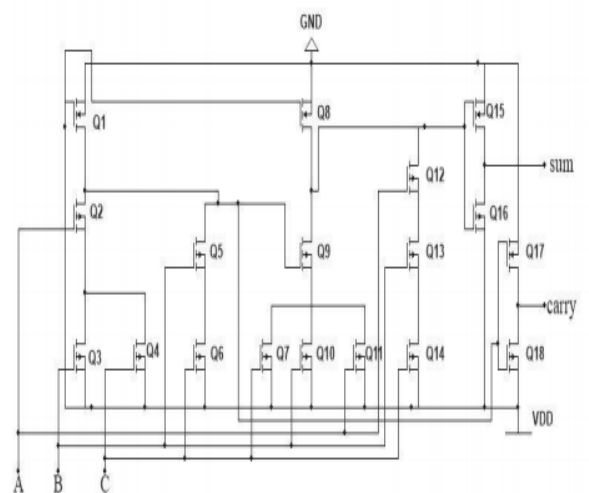

Figure 6 14T transistor Adder circuit

Figure 7 Pseudo nMOS Adder Circuit
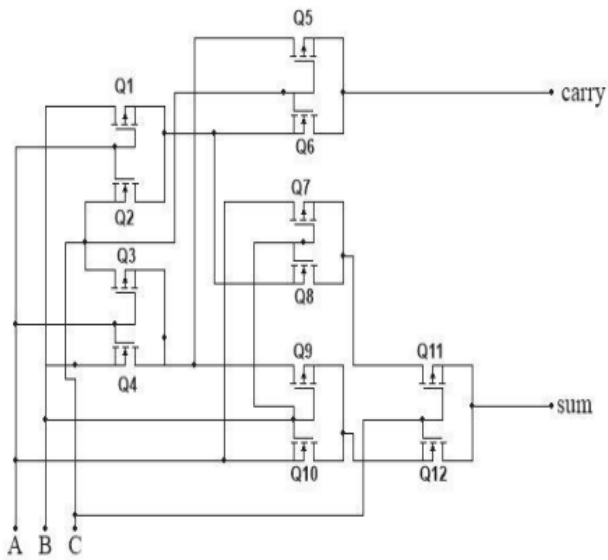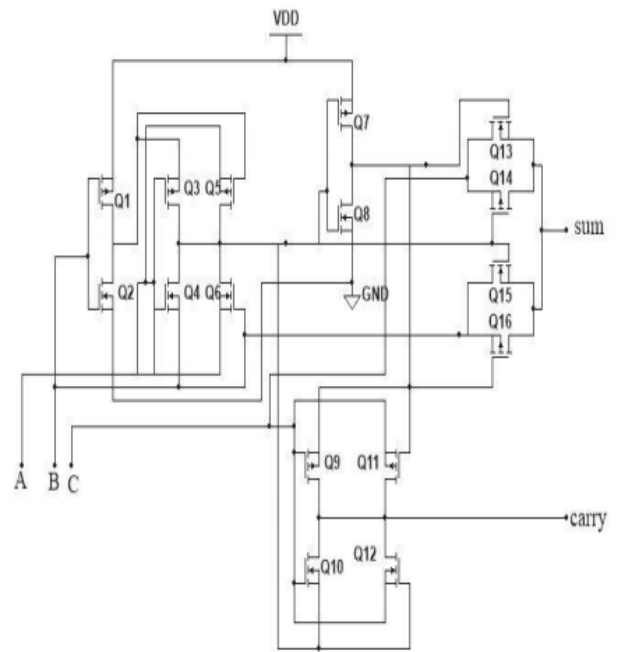
Figure 8 Multiplexer based Adder circuit design

Figure 9 8T Adder circuit design
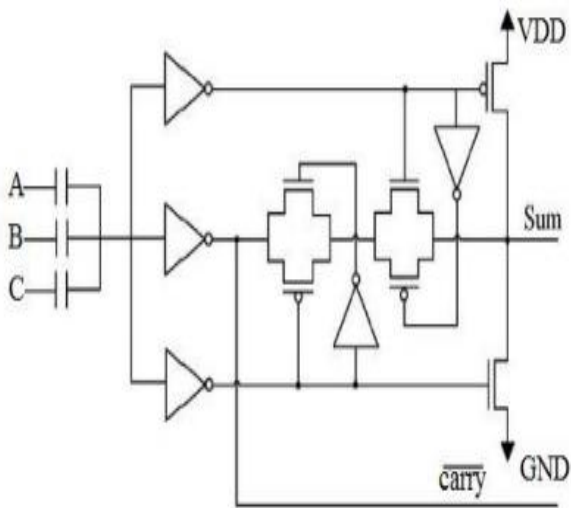
Figure 10 Inverter and Transmission Gate based adder design

Figure 11 Hybrid Adder circuit design

V. Comparison of various adders based on their delay analysis and associated process technologies

The performance analysis of several full adders drawn in table- 1 shows different adders with different parametervalues and different technology, no single adder have lessdelay,. thus, there exist tradeoffbetween these parameters. the results are helpful in selectionof an adder according to desired result and application.

Table 1
Comparison Table of Various adder circuits on the basic of delays and associated process technologies

Design Name	Process Technology	Delay (in ns)
6 Transistor	350 nm	0.133 ns
8 Transistor	150 nm	0.010 ns
9 Transistor	120 nm	0.295 ns
10 Transistor	180 nm	1.057 ns
12 Transistor	350 nm	0.217 ns
14 Transistor	180 nm	0.338 ns
20 Transistor	180 nm	0.250 ns
Pseudo NMOS	180 nm	0.182 ns
CMOS	180 nm	0.127 ns

A kind of activity which uses a computer to assist on the creation, modification and analysis of design. CAD tools generally consist of the following components, input handler (input from mouse or keyboard), data structure and algorithms (in memory), output handler (output to display). CAD environment generally consists of a simulator, design space exploration and design sign off.

The front end tools are used for design entry editors, simulation synthesis and timing analysis and test generation tools. The back end tools include floor planning place and route, extraction etc. Editors ,simulators, analyzers and synthesizers together contributes in computer oriented design.

VI. VLSI CAD Tools Vs Methodology for Adder Design

As we make progress in design technology, there is a ongoing debate within the design technology community about the importance of new algorithms and tools or new methodologies and associated tool flows.The simple fact is that history of design for microelectronic systems includes the going of both of them hand in hand to get the maximum benefit and in act these two aspects of the design technology are tightly coupled and correlated in terms of their impact.
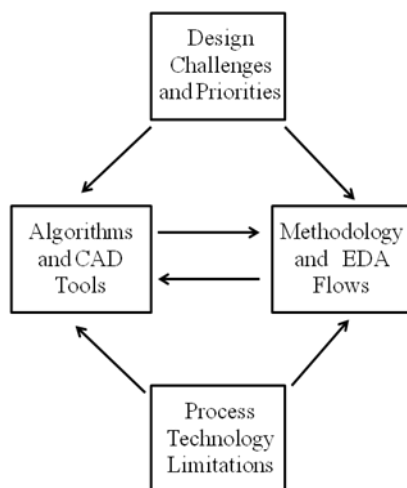

Fig.8.VLSI CAD/EDA vs CMOS Design Methodologies [1]

VLSI Design incorporates both the design methodologies and associated CAD tools because both forms the integral parts and should go hand in hand as they evolve based on the designer's needs.

VII. CONCLUSION

With design technology, it would be possible to implement, verify and test the complex integrated circuits like adders which is the basic unit of all arithmetic circuits. It is through design technology that the ideas and objectives of design, circuit and fabrication engineers are transformed into reality and the quality of the design tools and associated methodologies determine the design time, performance, cost and the correctness of the final product chip. The development in the design tools, collaborative design methods, the role of human factors and integration factors in the design technology marks the outline of various design methodologies. This paper explains design quality metrics from a CAD tool perspective and basic comparison of various adder topologies.Various shortcomings of the current designs and methodologies to tackle the VLSI design challenges were discussed and several promising remedies and their implications on design and methodologies are explored.

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