A Novel 21-level Inverter with Arithmetic Progression based Asymmetric Source Configuration

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Abstract **Multilevel inverters (MLI's) are attracting tremendous attention for high power DC-AC conversion. Efforts are also being done to employ MLI's for low power applications. However, for increased number of levels, component count remains an impending challenge. In this paper a new hybrid inverter is presented which utilizes lesser active switches along with asymmetric source configuration to synthesize 21-level waveform. Working of the proposed inverter is explained and concepts are validated with simulation results.**

Keywords **Multilevel inverters, hybrid topologies, asymmetric source configuration**

1. Introduction

In last some decades, multilevel voltage source inverters are being considered as cost-effective and efficient solution for high power DC to AC conversion [1]. A multilevel inverter (MLI) uses multiple input DC levels and power semiconductor devices to synthesize a staircase waveform. The voltage stresses handled by the power switches are lower as compared to the overall operating voltage level [2]. In addition, the output waveform has better harmonic profile as compared to the two level waveform obtained from the conventional inverters. Other advantages of MLI's are higher efficiency, reduced d*v*/d*t* tresses on the load and possibility of fault tolerant operations [3]. Attempts are also being made to employ MLI's for low power applications [4-6]. Harmonic profile of the multilevel waveform improves as number of levels increases, but it leads to necessity of a large number of power semiconductor devices and accompanying gate driver circuits. Hence, the overall system is rendered complex and expensive. Therefore, practical implementation requires reduction in number of switches and gate driver circuits [7].

So far, the topologies which are commercially available are: neutral point clamped (NPC) converters, cascaded H-bridge (CHB) converters and flying capacitors (FC) converters. Amongst these, the CHB topology offers higher reliability due to its modularity [7]. The CHB structure con series consists of several single-phase full bridge inverters also called 'cells'. However, for increased number of output levels, number of power switches number of switches conducting simultaneously and overall cost of the system increase significantly. Many modifications are being sought in the classical topologies to overcome these challenges. One of the simplest ways to increase number of levels using the same topology is to implement asymmetrical sources (i.e. two or more input DC sources are unequal) [7]. Decrease in component count, however, comes in this case at the cost of increased voltage rating of power switches.

In this paper, study of a newly proposed multilevel structure [8] is extended for asymmetric source configuration. The aforesaid topology is specifically proposed for reducing the count of power switches for a large number of levels in the output. Rest of the paper is organized as follows. In section 2, the topology in question is introduced. In section 3, popular asymmetric source configurations are briefly described and it is shown that these configurations are not applicable for the topology discussed in this paper. In section 4, a source configuration is proposed for the topology with four sources.

2. Introduction to the Topology

Gupta and Jain [8] have proposed a new topology with floating sources connected in cross fashion as shown in Fig.1. The topology utilizes only bidirectional-conducting-unidirectional-blocking power switches and electrically isolated input DC sources.

For n number of input DC sources, the topology would require '2n+2' number of power switches whereas a classical cascaded H-bridge topology would require '4n' number of power switches.

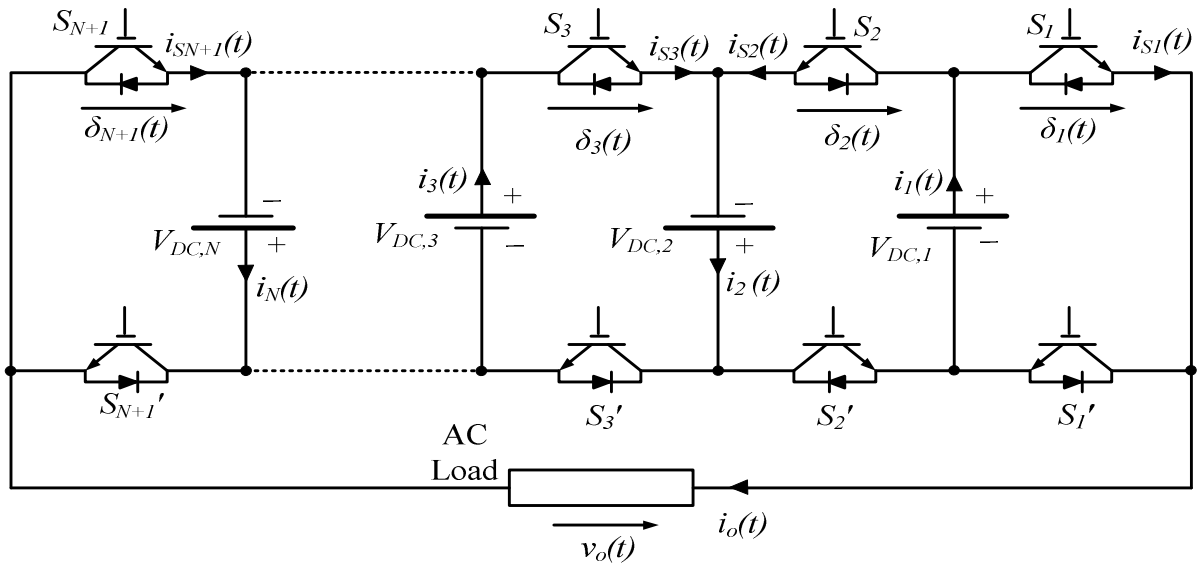

Fig.1. General structure of topology proposed by Gupta and Jain [8]

3. Conventional Asymmetric Source Configurations

Input DC sources in a multilevel structure can be configured in symmetric and asymmetric fashions. Considering four input sources viz. V_1, V_2, V_3 and V_4, the source configuration is designated as 'symmetric' when:

$$V_1 = V_2 = V_3 = V_4 = V_{DC} \quad (1)$$

When the values of input DC sources are different, the configuration is known as an 'asymmetric' source configuration. Two conventional asymmetric source configurations are :

(1) Binary Configuration :

Binary configuration is based on geometric progression (GP), i.e. the succeeding source has value equal to twice the preceding source. This means:

$$V_1 = V_{DC}, V_2 = 2V_{DC}, V_3 = 3V_{DC} \text{ and } V_4 = 4V_{DC} \quad (2)$$

(2) Trinary Configuration :

Trinary configuration is also based on geometric progression (GP), i.e. the succeeding source has value equal to thrice the preceding source. This means:

$$V_1 = V_{DC}, V_2 = 3V_{DC}, V_3 = 9V_{DC} \text{ and } V_4 = 27V_{DC} \quad (3)$$

These source configuration lead to a significant decrease in number of power switches in the cascaded H-bridge topology. For example, a CHB structure with two binary sources can synthesize seven levels with eight switches while a classical CHB would require twelve switches to synthesize seven levels. Similarly, a CHB structure with trinary configuration would synthesize twenty seven levels with eight switches whereas a classical CHB would require fifty power switches for the same.

Thus, by employing asymmetric source configuration, number of power switches can be further reduced for the topology shown in Fig.1. But while a CHB structure can synthesize all possibilities of additive and subtractive combinations of the input levels, the topology shown in fig.1 cannot do the same because of the limitations posed by the structure itself. For example, if a trinary source configuration is employed with V_1= 100V and V_2= 300V, a seven level waveform is synthesized with the level '200V' missing in the waveform, as shown in fig.2.

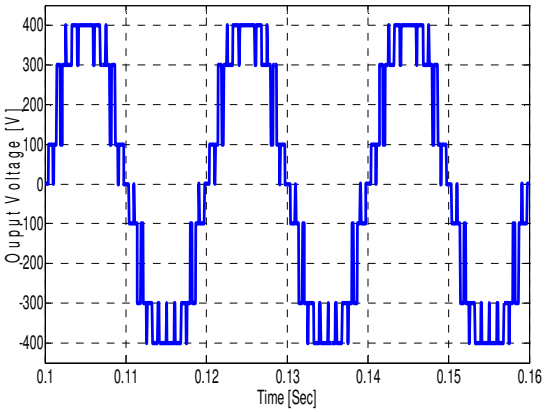

Fig.2. Output waveform for the topology with trinary sources

4. Proposed Asymmetric Source Configuration

Because of the configurational limitations posed by the topology, GP based asymmetric source configurations cannot be employed in the topology. In this paper, an arithmetic progression (AP) based asymmetric source configuration is proposed. That is to say, for four input sources, the source values are V_{DC} , $2V_{DC}$, $3V_{DC}$ and $4V_{DC}$. Still, the sources with these values cannot be placed in the natural sequence as appears in the topology. These sources

need to be strategically placed so that the output waveform has equal sized steps. For achieving this, the algorithm should be:

$$V_1 = V_{DC}$$
$$V_2 = 3V_{DC}$$
$$V_3 = 4V_{DC}$$
$$V_4 = 2V_{DC}$$

The aforesaid configuration can synthesize 21 levels in the output waveform, from $-10V_{DC}$ to $+10V_{DC}$ in steps of V_{DC}. Thus the waveform will have a peak value of $10V_{DC}$. The structure with four input DC sources with V_{DC} 100 V is shown in fig.3.

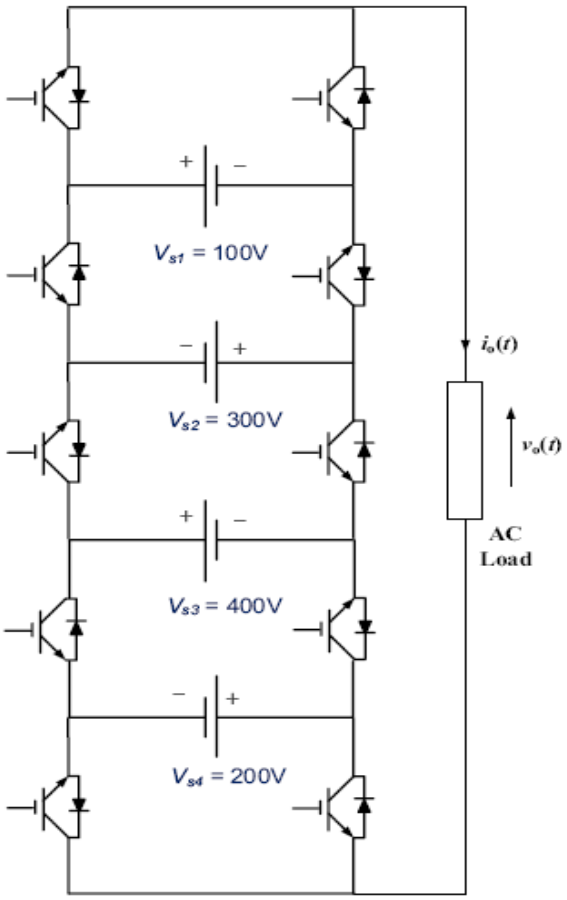

Fig.3. Cross connected sources based topology with asymmetric source configuration

The proposed source configuration leads to further decrease in number of power switches. For example, the topology with symmetric source configuration would require 22 switches while it would require only 10 switches with the proposed source configuration. Moreover, a classical CHB structure would need 40 switches for the same.

5. Simulation Results

In order to verify the proposed source configuration in the topology, MATLAB/Simulink based modelling is used to obtain simulated results.

A power circuit based on fig.3 is utilized and sine-triangle based PWM technique is implemented. A sinusoidal waveform with 50 Hz frequency is used as the reference and twenty phase opposition-disposed triangular waveforms with frequency 100 Hz are used as carrier signals. The model is shown in fig.4 while the reference and carrier waveforms are shown in fig.5.

Output voltage waveform is shown in fig.6. It is seen that the waveform has twenty one numbers of equal-sized levels and it shows a THD of 4.94% which is shown in fig.8. In addition, for an RL load with R = 10 and L = 25mH, the load current is shown in fig.7. Both the voltage and current waveforms have frequency of 50Hz.

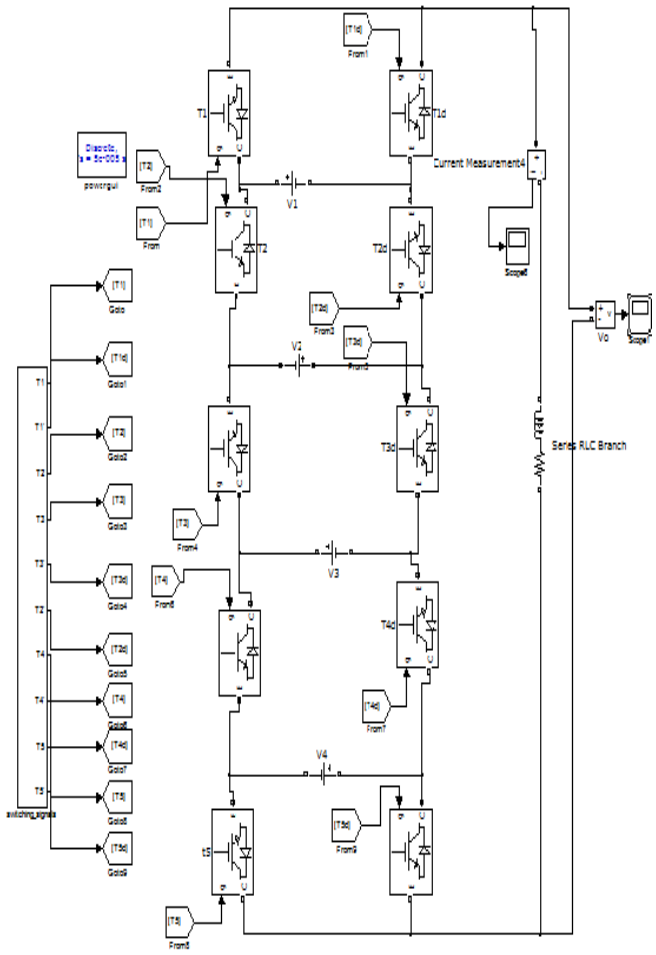

Fig.4.Simulation model of a 21-level inverter

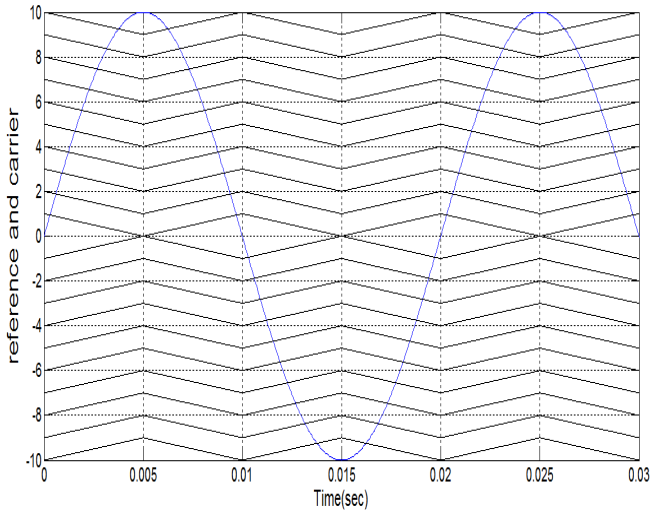

Fig.5. Reference and Carrier Waveform of a 21-level inverter

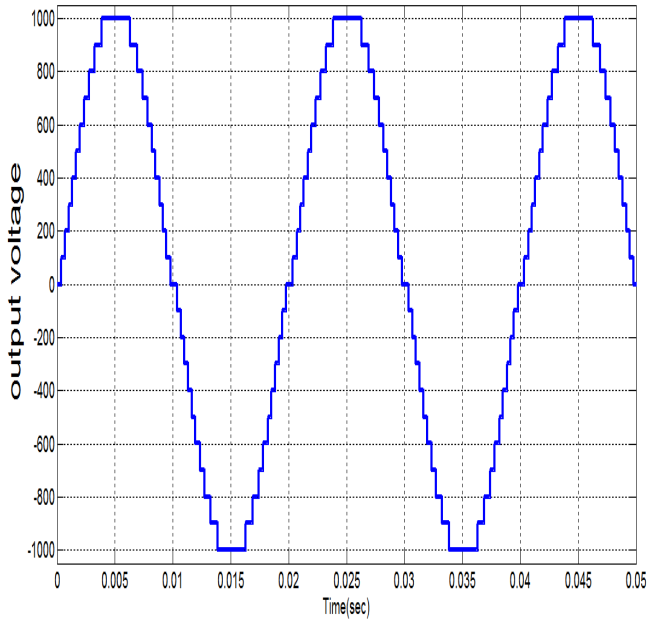

Fig.6. Output voltage of a 21-level inverter

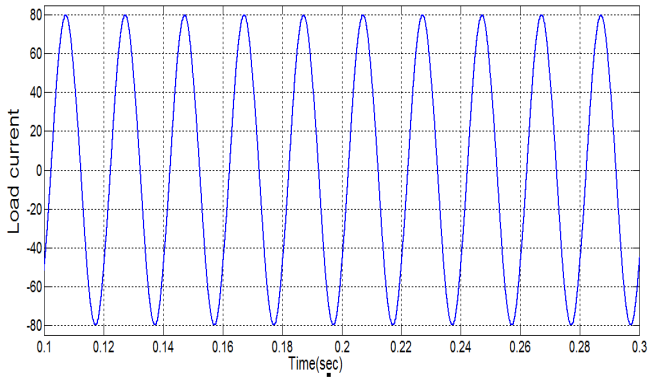

Fig.7. Line current of a 21-level inverter

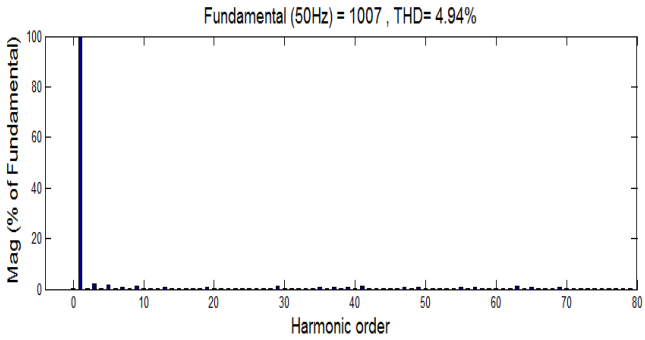

Fig.8. Harmonic spectrum of a 21-level voltage waveform

6. Conclusion

Asymmetric source configurations are known to reduce power switch count in multilevel inverter structures. Popular asymmetric source configurations are binary and trinary which are basically geometric progressions based schemes. In this paper, a newly proposed multilevel inverter is investigated for asymmetric source configuration. It is shown that the topology cannot be implemented with binary and trinary configurations because it has limitations in terms of combinations of input voltages that it can synthesize. Thus, to obtain an equal-sized waveform, geometric progression based asymmetric scheme cannot be implemented. Hence an arithmetic progression based methodology is proposed in this paper to obtain an equal-sized steps based waveform. Simulation results are used to verify the proposed algorithm.

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