Design of Capacitive DAC for a 14-bit Differential Successive Approximation Register ADC

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Abstract: - In this paper, Verilog-A based models of the comparator, SAR logic, switches, etc. of SAR ADC have been developed as ideal blocks to simulate in Cadence® Virtuoso® Analog Design Environment. Subsequently, 14-bit differential SAR ADC has been designed considering both conventional CDAC and optimally designed split CDAC integrating the Verilog-AMS based ideal blocks. Furthermore, a Verilog-AMS based testing module of INL (Integral non-linearity) and DNL (Differential non-linearity) for 14-bit differential SAR ADC using code is developed. Finally, INL and DNL have been calculated with developed code for a different resolution, and spectrum analysis of output signal has also been done.

Keywords: - SAR, ADC, DAC, Verilog

I. INTRODUCTION

The fundamental concept discussed in the previous chapter served as a guideline throughout the 14-bit differential SAR ADC design process. However, before implementing the circuit with the provided PDK, a high-level model was created. The high-level model consists of ideal sub-block models that are either described in Verilog-A code or implemented using ideal components from the analogLib library in the Cadence design environment. Although the sub-blocks do not take all non-idealities into account, limiting the accuracy of simulations, the overall functionality can be analyzed with great benefit using these models. One advantage of using a high-level model instead of directly going for a fully implemented design is that the simulation time can be reduced by using simplified models during the early stages of development [1, 2].

The efficiency in terms of accuracy, power consumption, and on-chip area of Successive Approximation Register (SAR) Analog to Digital Converter (ADC) depend on the charge redistribution Digital to Analog Converter (DAC) as mentioned in the previous chapter. Thus, the optimal design of SAR ADC demands accurate design and analysis of the DAC unit [3]. In this paper, a charge-redistribution DAC based on Binary Weighted with attenuation capacitor array has been presented for the design of a 14-bit differential SAR ADC and comparative study between presented work and conventional Binary Weighted DAC. Moreover, for calculation of INL (integral non-linearity) and DNL (differential non-linearity) through Verilog-A code are discussed for 14-bit differential SAR ADC. [4, 5]

The circuit was simulated using the test bench shown in figure 5.15, where ideal voltage sources generated input signal, reference voltage, a clock signal, and common-mode voltage all. The measurements were made with a sine wave as input signal and the ADC operating at a conversion speed of 10 KSps, as stated in the specification. In order to analyze the digital ADC output, an ideal DAC was put in series converting it to an analog signal [6, 7]. The fast Fourier transform (FFT) of this analog version of the output generates a spectrum in the frequency domain. From this spectrum, metrics such as SNDR and spurious-free dynamic range (SFDR), which is the ratio between the signal and the largest tone in the FFT, could be extracted by using the built-in spectrum-analysis tools in the Cadence environment. To provide an integer number of signal periods (coherent sampling) for the 32768-point FFT, a signal frequency of $33132768 * 10\text{KSps} = 101.0131836$ Hz was used.

II. SUCCESSIVE APPROXIMATION REGISTER (SAR) CONTROL LOGIC

The algorithm is sequentially executed in (n+1) states, one state for each of the n bits, and an additional state dedicated for sampling. Each state describes the events at a particular clock cycle in the conversion. In contrast to the comparator, the register triggers on rising clock edges. And the flow chart of SAR logic described below in figure 1, which shows the MSB (most significant bit) initially is set to '1' and remaining all bit at '0', according to the Binary search algorithm. Then depending upon the comparator value, SAR logic will decide the digital values. When the comparator gives the output '1', that means the MSB retained at '1' and set next MSB to '1', and this output of SAR logic will be feed into the positive CDAC. Consider the previous designed for 14-bit SAR logic, then the required number of D-F/F is more so the delay incorporated by its flip-flops is more. Thus avoiding this delay and some other non-idealities factor, we have using this SAR logic as an ideal sub-block, and it is designed by a Verilog-A code, which is shown in figure 2.

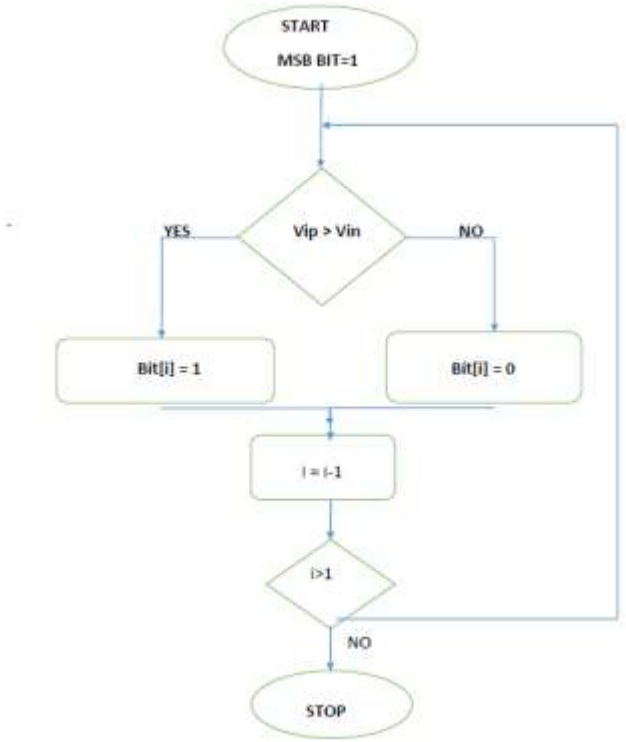

Figure 1: Flow chart of SAR logic

The SAR control logic makes its decision based on the output of the Comparator. So, in the Verilog-A model of SAR logic designed by using the below algorithm. For a 14-bit differential SAR logic, the digital outputs controlling the positive CDAC is d13 to d0, and controlling the negative CDAC is d13_b to d0_b, as shown in figure 2.

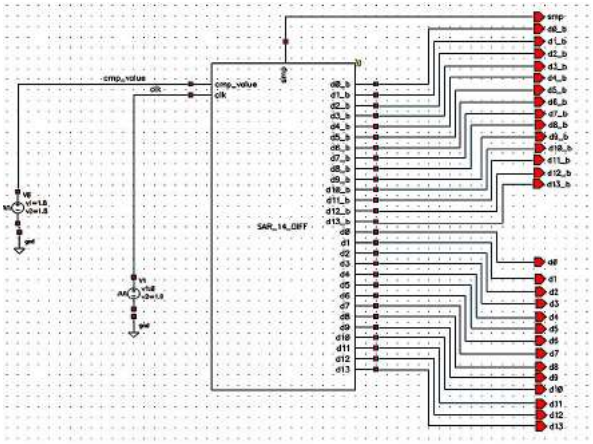

Figure 2: Verilog-A based model of SAR logic

III. IMPLEMENTATION OF 14-BIT DIFFERENTIAL SAR ADC

A differential 14-bit SAR ADC with a split capacitive DAC was implemented using ideal capacitors and switches. This high-level model was used for the evaluation of general functionality, measure non-linearity, and to verify the matching requirements of unit capacitors. Spectrum analysis for FFT calculation has been done using this testbench of input signal frequency fin = 101.0131836 Hz. Furthermore, a corresponding model for the conventional CDAC switching method was also created for comparison [8, 9].

Figure 3 shows the test bench of 14-bit differential SAR ADC considering split CDAC. In this design, we have taken designed switches, Comparator, and SAR control logic through the Verilog-A model from previously described and check the weather the output SAR ADC follows the input SAR ADC or not. In the test bench, we have applied the sinusoidal input for positive CDAC and the 180 phase shift of the original signal applied with negative CDAC. Where the sampling frequency is 10 KSPS, and the input signal having frequency is 100 Hz, and amplitude 900 mv and common-mode voltage is half of the reference voltage [10].

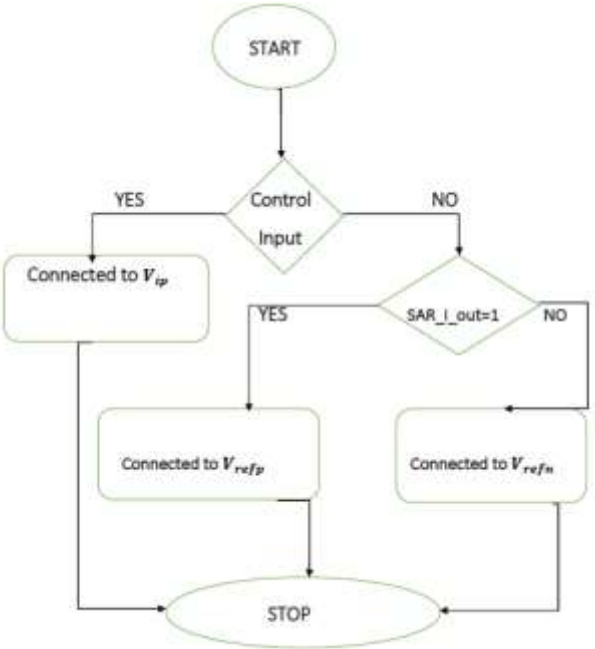

Figure 3: Flow chart of switch

Figure 4 (a) and (b) show that the differential output of split CDAC and the analog output from the ideal DAC sub-block, respectively. Both the waveform describing for the positive input voltage is 1.4 v, and the negative input voltage is 400 mV of 14-bit differential SAR ADC.

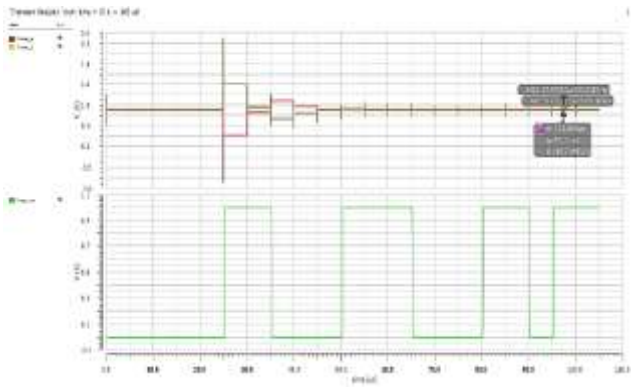

Figure 4: (a) differential outputs of split CDAC and analog Comparator's output for dc input 1.4 v.

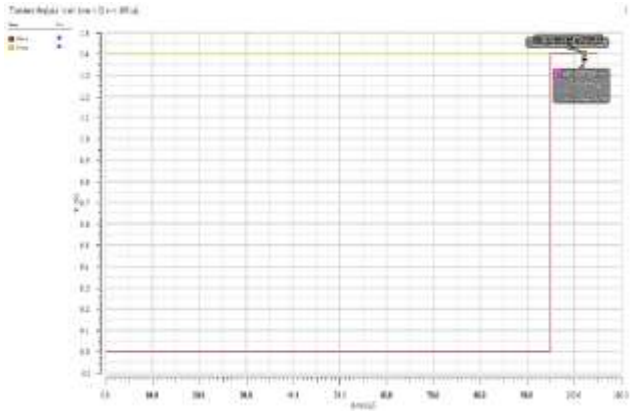

Figure 4 (b): Analog output of SAR ADC for dc input 1.4 v.

There are three phases of operation to perform the conversion:

(1) Sampled the input value: As mentioned in this thesis for five clock cycles, the sampling should have happened. In this sampling time

$$\boldsymbol{Ts = 5*5\mu = 25\mu\ seconds}$$

Which means for sampling frequency 10 KS/s, required 25μ sec for sampled the input signal

(2) For 5u sec, connecting MSB bit positive CDAC with a positive reference voltage and for negative CDAC with negative reference voltage according to Binary Search Algorithm.

(3) For conversion phase: for 14-bit SAR ADC required 14 comparison state

$$\boldsymbol{Tconv = 14*5\mu = 70\mu\ seconds}$$

Hence, the total time required to complete one complete conversion for a code is 100u sec.

For linear ramp total number of codes is 16384, so total transient time to simulate that is $\boldsymbol{Tsim}$ for the below testbench, which will take 3 to 4 hours to complete.

$$\boldsymbol{Tsim = 16384*100\mu = 1.6384\ seconds}$$

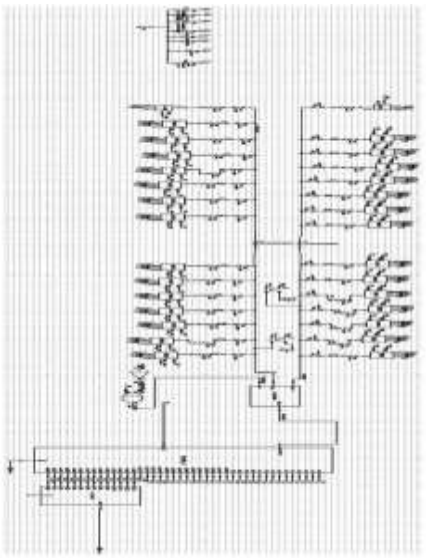

Figure 5: Schematic of differential 14-bit SAR ADC followed by split CDAC

Similarly, the 14-bit SAR ADC designed by 14-bit differential split CDAC, and its output waveform is shown in figure 5, which for sinusoidal input whose input frequency 100 Hz. The advantage over conventional CDAC is reducing the equivalent capacitance of split CDAC. In this design, we have used the unit capacitor values is 50fF.

Whereas in figure 6 shows the outputs waveform of negative and positive 14-bit differential split CDAC. The conversion period of 14-bit SAR ADC is 14 clock cycles, and for sample the signal, the sampling time is for six clock cycles.

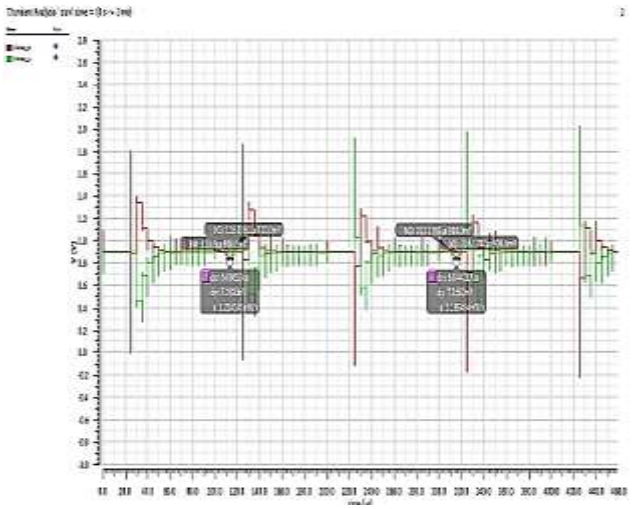

Figure 6: Differential CDAC outputs for input sinusoidal of 100 Hz.

Now the above test bench is verified by the giving dc input of 1.4 v. It is giving the correct results, which have been discussed above. Furthermore, for the sinusoidal input signal, which has input signal frequency is about 100 Hz and 900mv its amplitude. Figure 7 (a) and (b) show the output and input waveform of 14-bit differential SAR ADC for conventional and split CDAC, respectively.

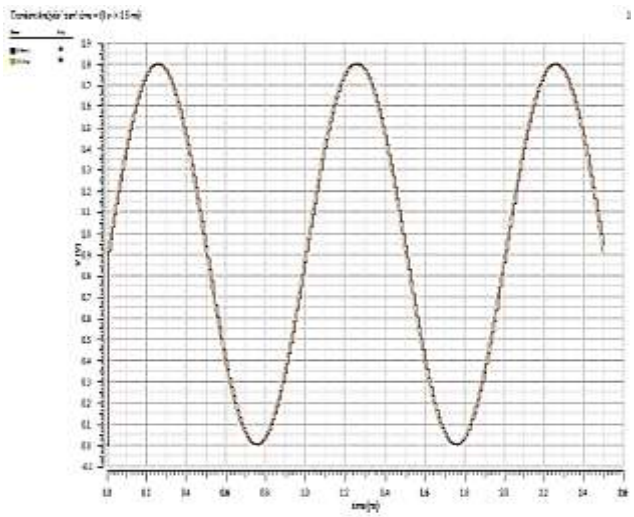

Figure 7 (a): The output waveform of 14-bit SAR ADC for conventional CDAC

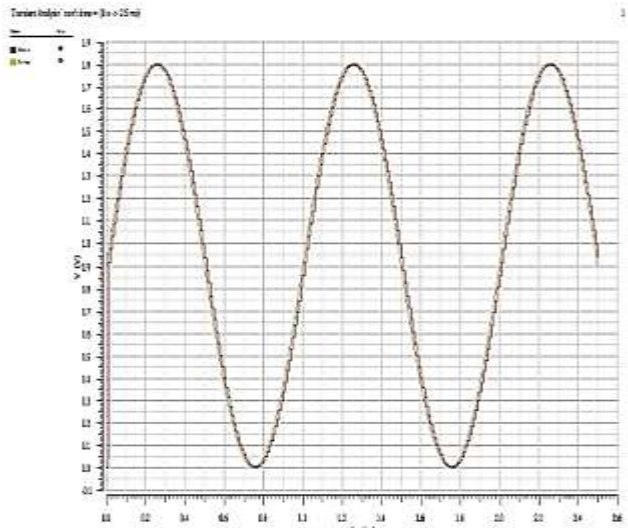

Figure 7 (b): The output waveform of 14-bit SAR ADC for split CDAC

IV. CONCLUSION

This paper presents the implementation of a 14-bit differential SAR ADC operating at sampling frequency 10KS/s and a supply voltage of 1.8V in 180 nm CMOS technology. This work has been demonstrated using a Verilog-A based ideal model of SAR control logic, Comparator, and switches, which has been reduced the simulation time in order.

In brief, the work primarily focused on the designing of an ideal model of 14-bit differential SAR ADC followed by split capacitive DAC. A Verilog-A model of SAR control logic developed to reduce the error and propagation delay, and it will give the required outputs. This output is the feedback of positive and negative CDAC. And also Comparator and switches are developed using the Verilog-A code to work as ideally.

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