

# VLSI Architecture for 4-bit & 8-bit Universal Shift Register using Reversible D-FF

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**Abstract-** Shift registers are the basic components in Very Large Scale Integration (VLSI) circuit design, which are used in various applications like communication transceivers, digital filters, cryptography circuits and network security devices. The expansion of word length in shift registers makes it appropriate for processing large scale data, since the data generated from various devices are of high quality one. Flip Flops (FFs) are the primary gadgets to integrate the shift register, where the numeral devices are interconnected with one other in series with respect to the register length. The performance of the shift register is prejudiced by key drivers such as area occupancy and energy consumption of the internal functional units. The target device used for implementation of linear feedback shift register is Xilinx software with Spartan-3 device family. The output waveforms and timing report are also discussed.

**Keywords**—Serial in Serial Output (SISO), Serial in parallel out (SIPO), Parallel in Serial out (PISO), Parallel in Parallel out (PIPO), Maximum Frequency

## I. INTRODUCTION

A digital circuit plays a vital role in the present communication era, use transistors to produce logic gates in order to realize various arithmetic and logical expressions. The benefits of digital circuits are better noise margin and quality than analog circuits. The error detection and correction is also easier with digital signals. One of the basic components in the digital circuit is a shift register [1]. In many applications such as digital filters, processor in personal computers, communication receivers and image processing Integrated Circuits (IC) is a generally used instance. In recent days the requirement of the shift register is increased in terms of word length, to handle the large size and high quality images in the image processing ICs. A 4K-bit and a 2K-bit shift registers are utilized in the image extraction as well as vector generation in VLSI chips and 10-bit 208-chain Liquid Crystal Display (LCD) column driver IC respectively [2].

It is fairly simple to design a shift register by connecting the required number Flip-flops in series based on its length up to N-bits. There is no circuit between the Flip-flops in the shift register; Flip-flops have superior speed than area and power consumption. The smallest Flip-flop is ideal to reduce area and power consumption by using the shift register. In many applications, pulsed latches

have recently replaced Flip-flops, as a pulsed latch is much smaller than a flip-flop. However, due to the existence of timing problem, the pulsed latches cannot be used in a shift register [3, 4].

For memory designs, shift registers are commonly used component in VLSI design. The shift registers are designed with Flip-flops and its count is depends on the register word length. The Flip-flops have a general structure with master-slave latches, that triggered either in the falling or rising edge and all the Flip-flops in the N-bit register are coordinated by means of clock- signal. The internal structure of the shift register consists of N number of series D Flip-flops that are interconnected with each other. The latches are designed using transmission gates [5]. Therefore there are no interlinked circuits between the Flip-flops and hence the speed of operation is not the principal constraint in the design of shift register while comparing with silicon area occupation and power utilization. The occurrence of timing problems between the latches in the design of the shift registers has been arrested by the non-overlapped pulse which is often considered to be the suitable choice for design of shift registers. This reduces the number of transistors in the design, reducing the area and energy consumption as well [6].

## II. SHIFT REGISTER

Shift registers are the synchronized sequential circuit, which have the capability to transmit the data from input to output. They are constructed using Flip-flops connected collectively in series and the number of bits stored (length) by the shift register are basically relative to the amount of Flip-flops. Each Flip-flop stores one bit at a time and in a shift register they are attached in such a way that the output of each Flip-flop is given as the input of another. Among the variety of Flip-flops, the DFF is preferred to construct the shift registers desirable. On every occasion, there is a modification in the clock signal of a DFF at either rise or fall edge, the input data (1 or 0) are transferred to the output of the Flip-flop and remains same until the arrival of the next clock pulse. The data at the output are always the same as the one at the input shown in Figure 1. Shift registers are primarily categorized by serial or parallel data transfer process. Serial In Serial Out shift register (SISO), Serial In Parallel Out (SIPO), Parallel In Parallel Out (PIPO) and Parallel In Serial Out (PISO) are the four common types of shift registers. Figure 1 displays the block diagram of the SISO shift register.

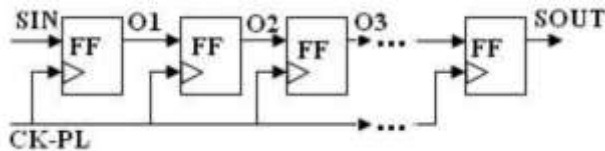


Figure 1: Block Diagram of SISO Shift register

The key limitation in low power design is power dissipation and therefore the overall power usage of the system has to be controlled. The overall energy usage of such equipment is important because it is desirable to use the run time with increased battery life, reduced battery weight and size requirements. So, low power architecture is the decisive factor in the design of System On Chip (SOC) in portable devices. Mobile users normally require additional features and extended battery life at a lower cost. Nearly, 70% of consumers look for the key feature for mobile devices like longer talking time and standby time. Power consumption is one of the most significant criteria, where the customers are always searching for mobile devices that are lighter, smaller and elegant. High levels of silicon integration in modern procedures are sufficient, but inherently high power indulgence is required in sophisticated processes. The architecture is very relevant in low power consumption applications [7].

**III. PROPOSED METHODOLOGY**

This sequential device loads the data present on its inputs and then moves or “shifts” it to its output once every clock cycle, hence the name Shift Register. A shift register basically consists of several single bit “D-Type Data Latches”, one for each data bit, either a logic “0” or a “1”, connected together in a serial type daisy-chain arrangement so that the output from one data latch becomes the input of the next latch and so on. Data bits may be fed in or out of a shift register serially, that is one after the other from either the left or the right direction, or all together at the same time in a parallel configuration. The number of individual data latches required to make up a single Shift Register device is usually determined by the number of bits to be stored with the most common being 8-bits (one byte) wide constructed from eight individual data latches. Shift Registers are used for data storage or for the movement of data and are therefore commonly used inside calculators or computers to store data such as two binary numbers before they are added together, or to convert the data from either a serial to parallel or parallel to serial format. The individual data latches that make up a single shift register are all driven by a common clock (Clk) signal making them synchronous devices. Shift register IC’s are generally provided with a clear or reset connection so that they can be “SET” or “RESET” as required. Generally, shift registers operate in one of four different modes with the basic movement of data through a shift register being:

- Serial-in to Serial-out (SISO) - the data is shifted serially “IN” and “OUT” of the register, one bit

at a time in either a left or right direction under clock control.

- Serial-in to Parallel-out (SIPO) - the register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form.
- Parallel-in to Serial-out (PISO) - the parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.
- Parallel-in to parallel-out (PIPO) - the parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.

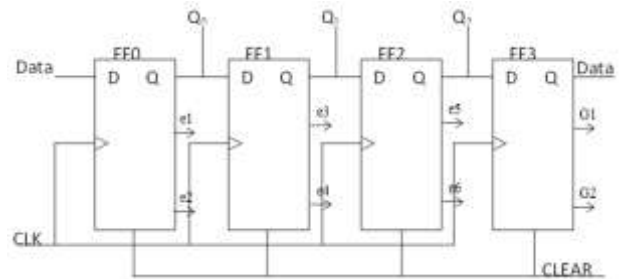


Figure 2: Flow Diagram of Serial in Parallel Output Shift Register

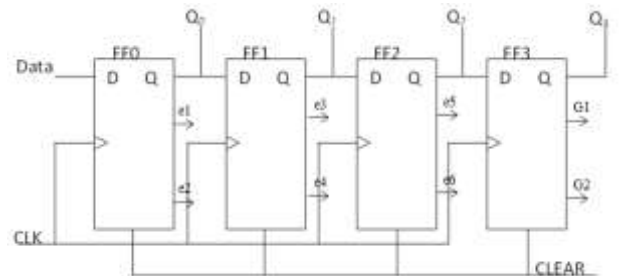


Figure 3: Flow Diagram of Parallel in Serial Output Shift Register

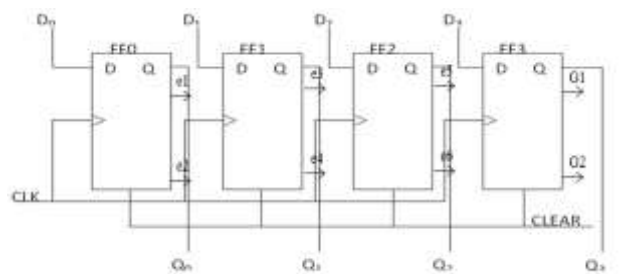


Figure 4: Flow Diagram of Parallel in Parallel Output Shift Register

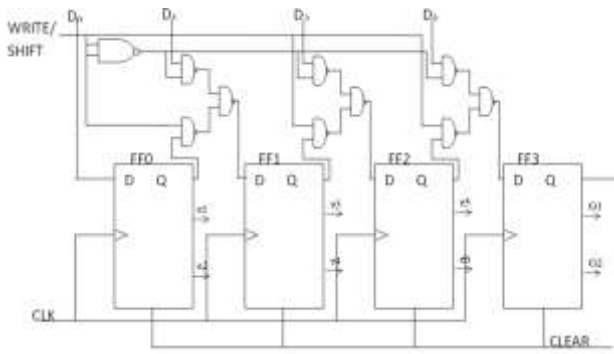


Figure 5: Block Diagram of Reversible Parallel in Serial out Shift Register

**Universal Shift Register**

The basic block diagram of universal shift resistor is shown in figure 6. This can be design using four 4x1 multiplexer and four D-flip-flops. The four multiplexers are M0, M1, M2 and M3. The D-flip-flops are DFF0, DFF1, DFF2 and DFF3, where the terminals D0, D1, D2 and D3 are parallel inputs and the terminals Q0, Q1, Q2 and Q3 are parallel output terminals. S0 and S1 terminals are the selection line for different mode of operations.

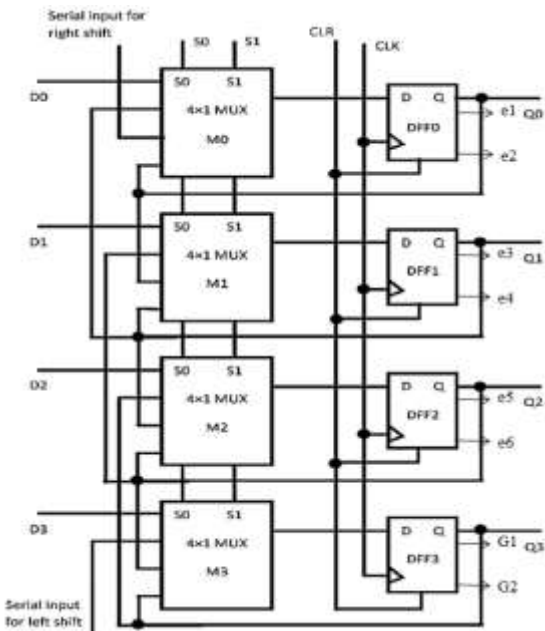


Figure 6: The 4 bits basic universal shift register

Figure 6 shows the proposed RUSR, where each multiplexer M0, M1, M2 and M3 are design by using three reversible MF Gates. Each of the D-flip-flops viz. DFF0, DFF1, DFF2 and DFF3 are designed using one SAM Gate and one Feynman Gate. The parallel inputs terminal, parallel outputs terminal and selection lines are same as figure shown in figure 6. Table 1 shows the functional characteristic of proposed shift register.

Table 1: Functional table of proposed 4-bits RUSR

S0	S1	Function
0	0	Parallel Load
0	1	Left Shift
1	0	Right Shift
1	1	No Change

**Reversible D\_FF**

Block diagram of reversible D\_FF is present by figure 7. There are three inputs and three outputs represent by reversible delay flip flop.

If (Rst = 0) then

P = 0

Q = 1 = G1 (Garbage Output)

R = Din = G2 (Garbage Output)

Else

P = Din

Q = not (Din)

R = Din XOR (Rst and Clk)

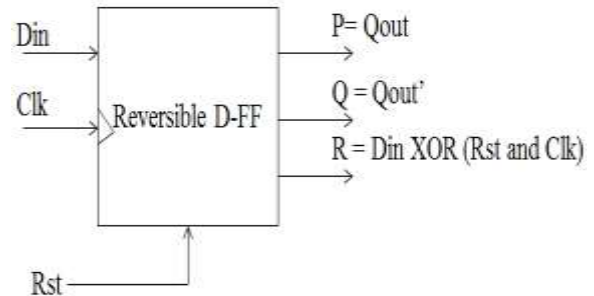


Figure 7: Block Diagram of Reversible D\_FF

**IV. SIMULATION RESULT**

All the designing and experiment regarding algorithm that we have mentioned in this paper is being developed on Xilinx 14.1i updated version. Xilinx 9.2i has couple of the striking features such as low memory requirement, fast debugging, and low cost. The latest release of ISE™ (Integrated Software Environment) design tool provides the low memory requirement approximate 27 percentage low. ISE 14.1i that provides advanced tools like smart compile technology with better usage of their computing hardware provides faster timing closure and higher quality of results for a better time to designing solution. ISE 14.1i Xilinx tools permits greater flexibility for designs which leverage embedded processors. The ISE 14.1i Design suite is accompanied by the release of chip scope Pro™ 14.1i debug and verification software. By the aid of that software we debug the program easily. Also included is the newest release of the chip scope Pro Serial IO Tool kit, providing simplified debugging of high-speed serial IO designs for Virtex-4 FX and Virtex-5 LXT and SXT FPGAs. With the help of this tool we can develop in the area of communication as well as in the area of signal processing and VLSI low power designing. To simplify multi rate DSP and DHT designs with a large number of clocks typically found in wireless and video applications, ISE 14.1i software features breakthrough advancements in place and route and clock algorithm offering up to a 15 percent performance advantage. Xilinx 14.1i Provides the low memory requirement while providing expanded support for Microsoft windows Vista, Microsoft Windows XP x64, and Red Hat Enterprise WS 5.0 32-bit operating systems.

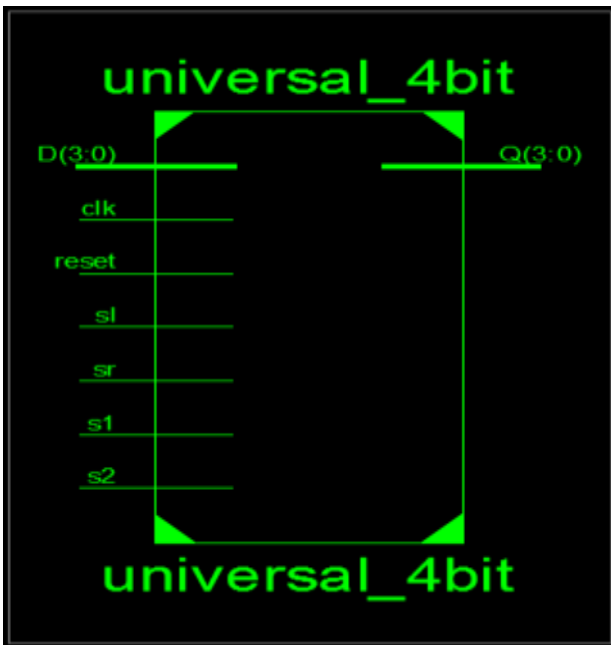


Figure 8: VTS of 4-bit Universal Shift Register

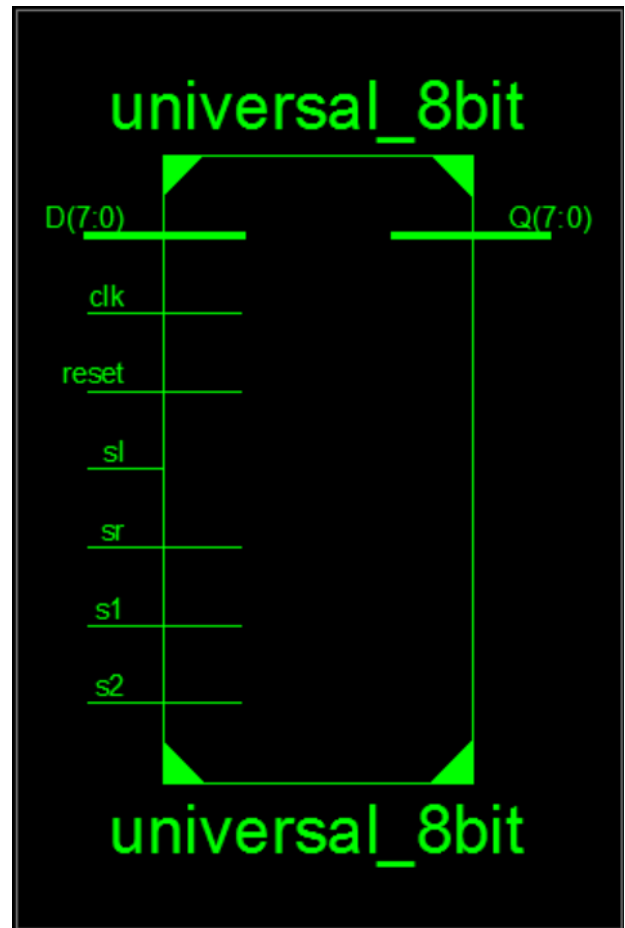


Figure 11: VTS of 8-bit Universal Shift Register

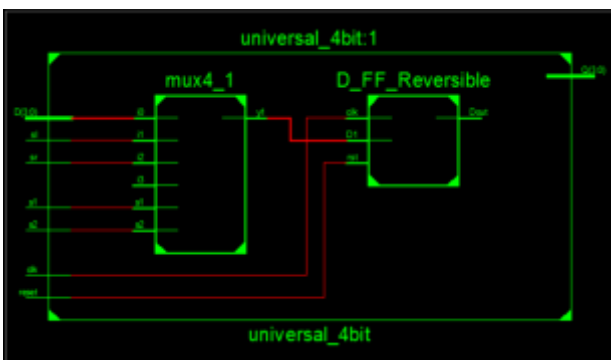


Figure 9: RTL of 4-bit Universal Shift Register

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Device utilization summary:
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Selected Device : 3s50pq208-4

Number of Slices:          11 out of   768   1%
Number of Slice Flip Flops:  4 out of  1536   0%
Number of 4 input LUTs:    25 out of  1536  1%
Number of IOs:             14
Number of bonded IOBs:     13 out of  124  10%
Number of GCLKs:           1 out of    8  12%

Timing Summary:
-----
Speed Grade: -4

Minimum period: 4.555ns (Maximum Frequency: 219.539MHz)
Minimum input arrival time before clock: 5.077ns
Maximum output required time after clock: 10.242ns
Maximum combinational path delay: 10.690ns
    
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Figure 10: Device Utilization of 4-bit Universal Shift Register

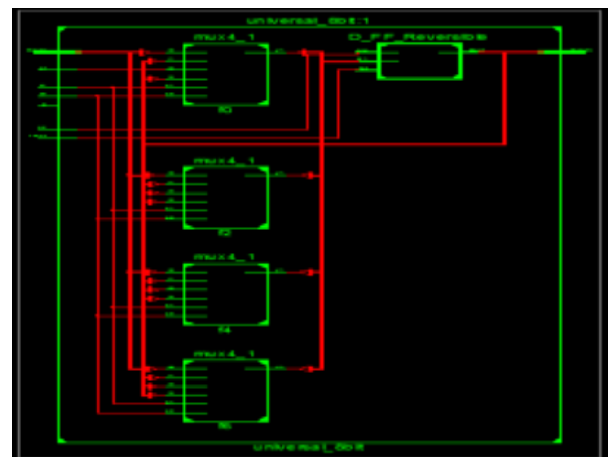


Figure 12: RTL of 4-bit Universal Shift Register

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Device utilization summary:
-----
Selected Device : 3s50pq208-4

Number of Slices:          10 out of   768   1%
Number of Slice Flip Flops:  4 out of  1536   0%
Number of 4 input LUTs:    23 out of  1536   1%
Number of IOs:             22
Number of bonded IOBs:     16 out of  124  12%
Number of GCLKs:           1 out of    8  12%

Timing Summary:
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Speed Grade: -4

Minimum period: 4.628ns (Maximum Frequency: 216.076MHz)
Minimum input arrival time before clock: 5.076ns
Maximum output required time after clock: 10.379ns
Maximum combinational path delay: 10.627ns
    
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Figure 13: Device Utilization of 8-bit Universal Shift Register

## V. CONCLUSION

In this paper, we have discussed the VHDL implementation of configurable linear feedback shift register by number of slice, number of flip flop, input output bounded, minimum period, arrival time before max input clock, arrival time after max input clock and maximum frequency. Similarly, another primary component which decides the action of the shift registers is the clock distribution circuit. The arrival of a clock signal to different Flip-flops from the clock generation unit, transistor transition and device count in the clock pulse generator are the important concerns in the design of clock pulse generator. In recent years, the need for shift length is increased dramatically in image processing ASICs to deal with outsized image data and in data communication transceiver circuits

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