Switched Capacitor based Multilevel Inverter with Reduced Device Counts for Electric Vehicles

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Abstract— MLIs have a significant advantage over two-level inverters, including lower *dv/dt*, less electromagnetic interference, improved harmonic performance and reduced output filter size. NPC inverter, FC inverter and CHB inverters are three of the earliest well-established inverter topologies that have been around for a long time. These conventional topologies each have their own set of advantages and disadvantages. In the case of NPC and FC suffer the capacitor voltage balancing issues and require a complex control strategy to balance the capacitor voltage. Six unidirectional switches, one diode, and one capacitor with a PV source are used. In this topology, a leg of the switched capacitor is cascaded with the H-bridge structure. The capacitor (C) is charged to the DC input voltage of V_{DC}. The proposed inverter generates different output levels of 0, $\pm V_{DC}$, and $\pm 2V_{DC}$. It archive five-voltage level at the output terminal and generates boost output voltage with levels of +200V, +100V, 0, -100V and -200V.

Keywords— Multi-level Inverter, 5-level, Boost Factor, Switched Capacitor

I. INTRODUCTION

In modern technology, power electronics and processor plays a vital role in the field of motor control, light control, heat control, power supplies, vehicle system, HVDC, FACTS and renewable applications. The philosophy focuses on preserving the energy and meeting the power demand accurately and the power modulator pertaining to inverter / converter technology fulfills the requirements and this attracts the researchers to explore in the inverter field. The above-mentioned applications work in the range of medium power, high power at a higher voltage. With the help of semiconductor device technology, power converters are to be designed with higher operating voltage. As a single device fails to support such high voltages, a number of devices need to connect in series to meet the voltage rating. Another challenge in the industrial sector is the requirement and maintenance of the sinusoidal power supply with variable voltage and frequency. The above demerits are overcome by the introduction of Inverters. The series connected switches in the inverters and through control mechanism, the voltage stress with respect to high voltage rating is shared among the series switches and also the losses are minimized. Due to advantage of minimum losses, inverters is also used for medium voltage applications. The classical square wave inverter operating at higher voltage introduces the dominant harmonics, thereby the performance on the load side and on the front end of the inverter has a large impact and the performance is affected. Though the solution is sought through the passive filters, the loss are increased and occupies more space. The alternative path is provided by Multilevel Inverters (MLI) [1, 2]. MLI generates sinusoidal voltage waveform in the form voltage steps through switching sequence. The other advantages of MLI are reduced electromagnetic interference, reduced current distortion, good quality voltage waveform, good current waveform. The basic types of MLI are neutral point clamped MLI, flying capacitor MLI and cascaded H-bridge MLI. To synthesize nearly sinusoidal voltage, higher number of levels needs to be generated with the help of more number of switches, more number of sources and more number of gate drivers [3, 4]. Due to this, the efficiency decreases as more number of switches are utilized in the conduction path.

II. PROPOSED METHODOLOGY

An exhaustive assessment of the literature is presented with the goal of decreasing the number of devices required to support an increased number of output levels. In this section, the thesis objectives and structure are discussed in detail. Nowadays, investments in new renewable and sustainable energy sectors are being rapidly carried out to reduce CO2 emissions and address global warming caused by the use of fossil fuels.

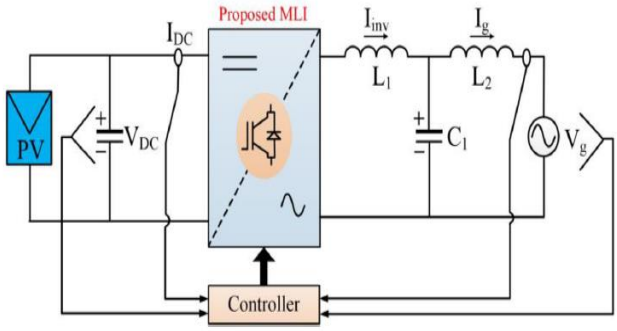

Fig. 1: Proposed Methodology

Advances in power electronics have contributed greatly to the advent of solar photovoltaic and wind energy-based power generation systems. In order to connect is these sources to the distribution grid and/or local loads. Basic application of proposed work is shown in figure 1.

MLIs have a significant advantage over two-level inverters, including lower *dv/dt*, less electromagnetic interference, improved harmonic performance and reduced output filter size. NPC inverter, FC inverter and CHB inverters are three of the earliest well-established inverter topologies that have been around for a long time. These conventional topologies each have their own set of advantages and disadvantages. In the case of NPC and FC suffer the capacitor voltage balancing issues and require a complex control strategy to balance the capacitor voltage. The number of clamping diodes and capacitors required increases as the voltage levels increase. To synthesize a multistep voltage waveform, Separate dc sources are required for the CHB inverter and consequently, the voltage gain in all the classical topologies is limited to one. To address these difficulties, the concept of switched DC source and reduced device count to maximize the voltage level have been investigated, as they provide a compact architecture that reduces the systems cost and control complexity. Existing topologies have the problem of voltage boosting capabilities. Novel topologies based on a Switched Capacitor (SC) are being researched to improve boosting ability and significantly reduce the number of devices further. Figure 2 shows the proposed five-level boosting inverter topology.

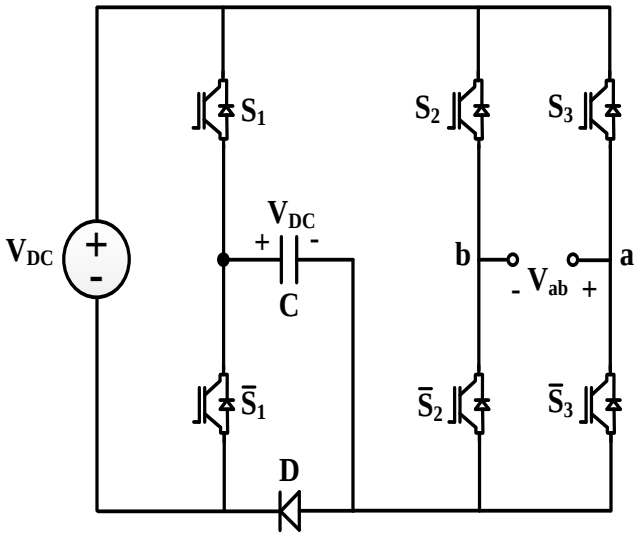

Fig. 2: 5-level Inverter

Boost Inverter

The operational states and capacitor parallel and series path (i.e., charging and discharging) for the proposed 5-Level inverter for a grid-connected PV power generation are shown in Table 4.1. It's worth noting that 1 and 0 represent the ON and OFF states of the power switches. "Δ" and "∇" indicate the charging and discharging modes of the capacitor 'C'. The path through which capacitors are charged is shown in green, and the resistive load and inductive load current path are shown in blue and red.

Table 1: Switching table of proposed boost inverter

Switching State	V_{ab}	Power Switches						Capacitors (C)
		S_1	$\bar{S}_1$	S_2	$\bar{S}_2$	S_3	$\bar{S}_3$	
μ_1	0	1	0	1	0	1	0	Δ
μ_2	$+V_{DC}$	1	0	0	1	1	0	Δ
μ_3	$+2V_{DC}$	0	1	0	1	1	0	∇
μ_4	0	1	0	0	1	0	1	Δ
μ_5	$-V_{DC}$	1	0	1	0	0	1	Δ
μ_6	$-2V_{DC}$	0	1	1	0	0	1	∇

Vab=0: It defines states μ1 and μ4. As shown in Figure 3 and Figure 4.4 zero-voltage state across the load in which switches S1, S2 and S3 or S1, $\overline{S2}$ and $\overline{S3}$ are ON, while turning OFF $\overline{S1}$, $\overline{S2}$ and $\overline{S3}$ or $\overline{S1}$,S2 and S3. As a result of being in parallel with the DC supply, the capacitor C gets charged to voltage V_{DC} through the switch S1.

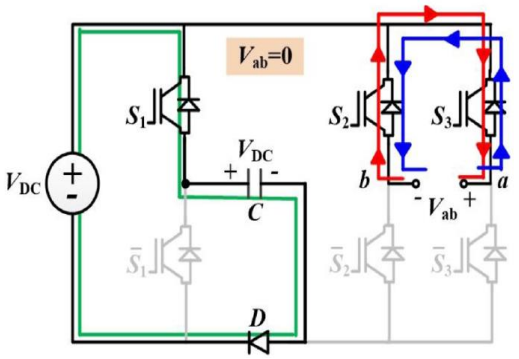

Figure 3: Vab=0

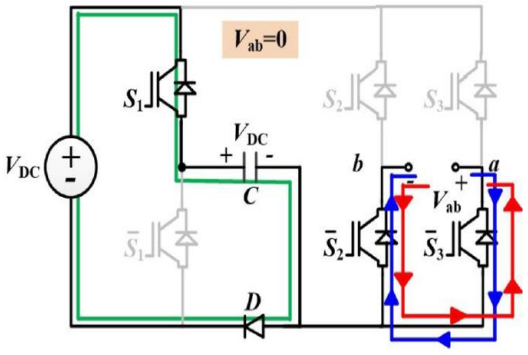

Figure 4: Vab=0

Vab=+VDC: As depicted in figure 4, power devices S1, $\overline{S2}$ and S3 are conducting while $\overline{S1}$, S2 and $\overline{S3}$ are OFF. The capacitor C is charged to the VDC by parallel connection with the source. This operation defines the state μ2.

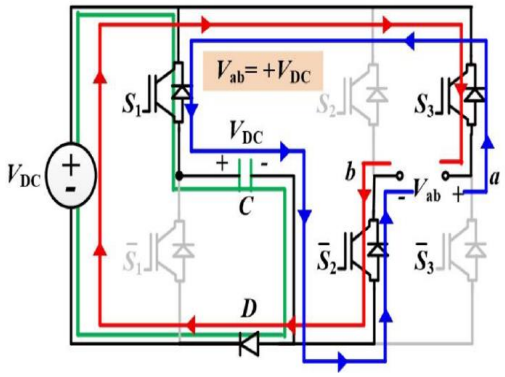

Figure 5: Vab=+V_{DC}

Vab= +2VDC: It defines state µ3. In this state, shown in figure 5, power devices $\overline{S1}$, $\overline{S2}$ and S3 are conducting while S1, S2 and $\overline{S3}$ are OFF. In this state, by turning ON the switch $\overline{S1}$ capacitor C appears in series with the DC source and gets discharged.

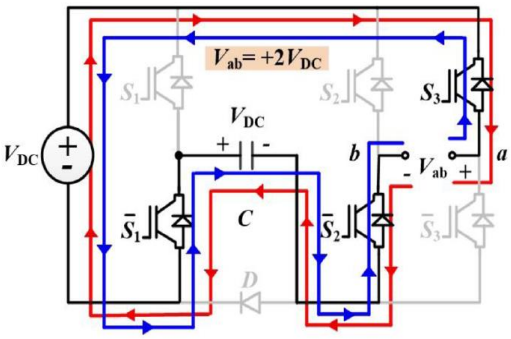

Figure 6: Vab=+2V_{DC}

Vab= -VDC: It defines state µ5. By turning ON S1 Capacitor C appeared across the DC source and got charged to voltage VDC. The level -VDC is achieved when power switches S1, S2 and $\overline{S3}$ conduct while turning OFF $\overline{S1}$, $\overline{S2}$ and S3. This state is shown in figure 7.

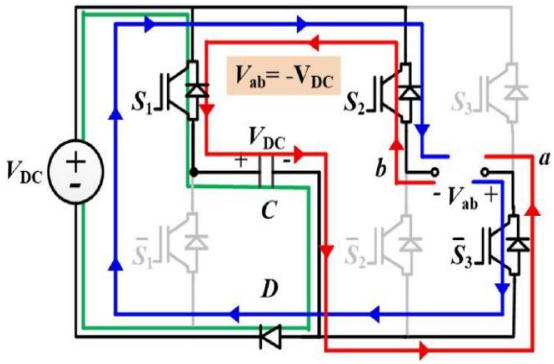

Figure 7: Vab=-V_{DC}

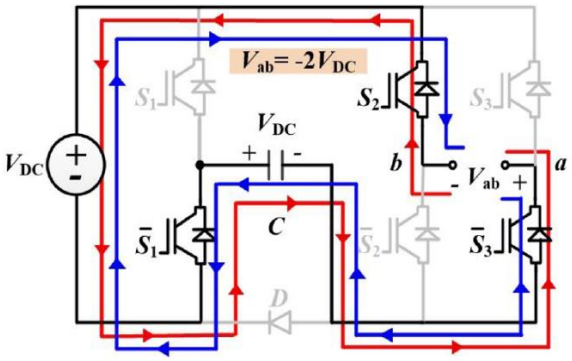

Figure 8: Vab=-2V_{DC}

Vab= -2VDC: In this state, as shown in figure 8, by turning ON the switch $\overline{S1}$ capacitor C appears in series with the source and gets discharged. The -2VDC level is achieved by conducting power switches $\overline{S1}$, S2 and $\overline{S3}$ while turning OFF S1, $\overline{S2}$ and S3. This operation defines the state µ6.

III. SIMULATION RESULT

Figure 9 shows the load voltage and load current with resistive load of 50 Ohm. It archive five-voltage level at the output terminal and generates boost output voltage with levels of +200V, +100V, 0, -100V and -200V.

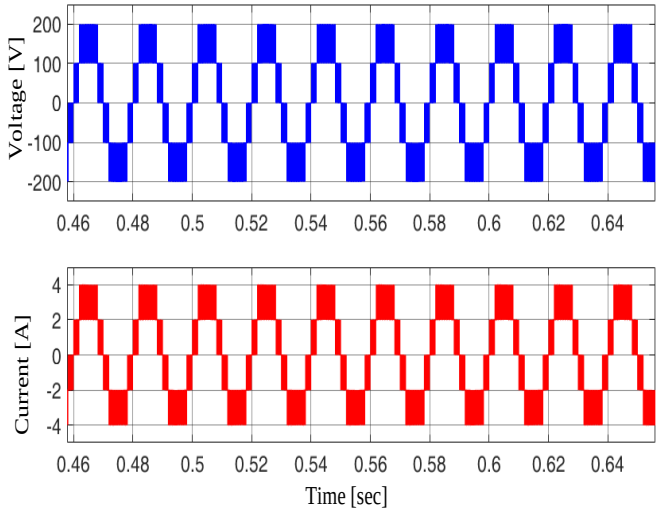

Figure 9: Output voltage and current with resistive load

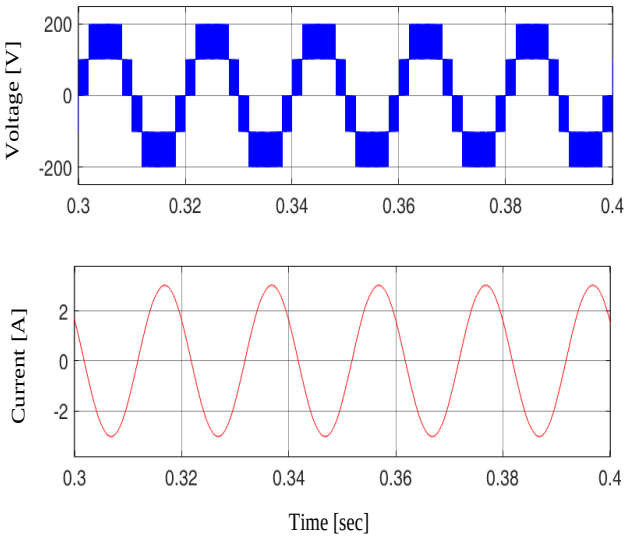

Figure 10: Output voltage and current with inductive load

Figure 10 shows the load voltage and load current with inductive load of 50 Ohm and 100mH. It archives five-voltage level at the output terminal and generates boost output voltage with levels of +200V, +100V, 0, -100V and -200V. Also, generates pure sinusoidal current at the output load terminal.
Figure 11 shows the dynamic response of the proposed multilevel inverter. In this intense the inductive load change from 100Ohm 100mH to pure resistive load 50Ohm at the time of 0.5sec. It can be clearly seen that the output voltage has not change at this time but output current has been doubled at this point. Its changes from 1.8A inductive current to the 4A resistive current after doing change the load.
Figure 12 shows the Total harmonic profile (THD) of the output current. Its achieves a minimum value of the THD i.e., 0.46% that is good enough to use for the grid and also can be used for the different load applications.

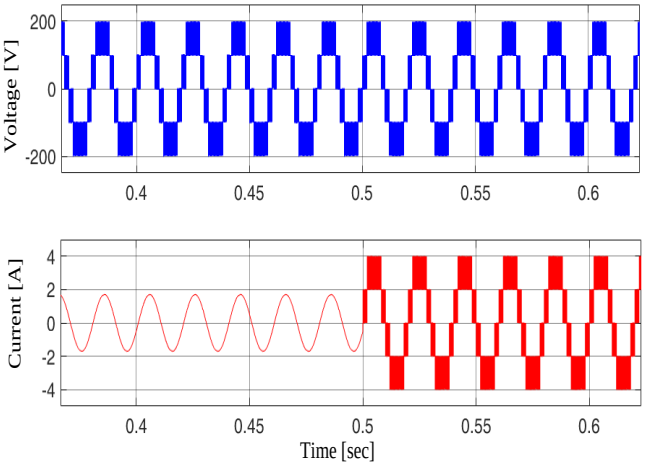

Figure 11: Output voltage and current with inductive load change to resistive load

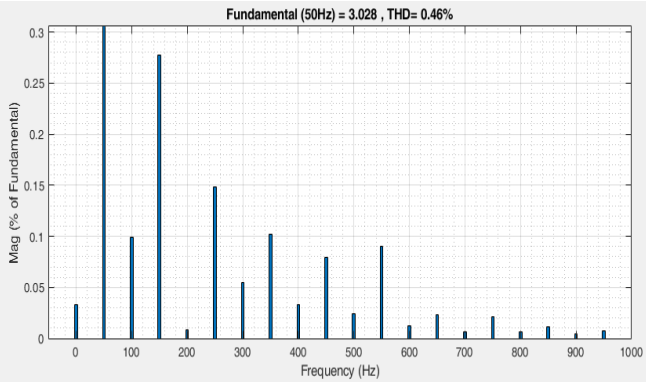

Figure 12: Total harmonic distortion (THD) profile of output current

IV. CONCLUSION

To generate a PWM signal, high-frequency triangular signals are compared with the sinusoidal reference. The resulting pulses are used to switch devices corresponding to various voltage levels. As depicted in figure 4.8, waveforms Vcrα{α = 1 to 2} of the similar frequency (fcr), phase angle, and maximum peak value (Acr) are utilized for carriers. The voltage controller generates a reference signal (Vref) with amplitude (Aref) and frequency (fref). The absolute value |Vref| is compared to the high-frequency triangle signal Vcr1 to Vcr2 with a similar frequency and phase angle.
When it is connected in series with the load, it releases its stored energy. Several charging durations of the capacitor occur during one cycle of the output voltage and capacitor voltages can dynamically maintain the source voltage, with some voltage ripples. This feature enables automatic balancing of the capacitor voltage. Capacitance discharge values are dependent on the load, the longest discharge time and the load power factor.

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