VLSI Architecture for 1-D and 2-D DWT using Canonic Signed Digit Technique

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Abstract— Several architectures have been suggested for efficient VLSI implementation of 2-D DWT for real-time applications. It is found that multipliers consume more chip area and increases complexity of the DWT architecture. Multiplier-less hardware implementation approach provides a solution to reduce chip area, lower hardware-complexity and higher throughput of computation of the DWT architecture. Based on the proposed 1-D & 2-D DWT using canonic signed digit (CSD) are presented in this paper for area-delay efficient realization of multilevel 2-D DWT. We demonstrate that CSD is a very efficient architecture with adders as the main component and free of ROM, multiplication, and subtraction. The simulation was performed using XILINX 14.5i and calculate simulated parameter i.e. number of slice, look up table and delay.

Keywords: - 1-D DWT, 2-D DWT, CSD, Xilinx Software

I. INTRODUCTION

The DWT is computationally intensive and most of its application demand real-time processing. One way of achieving high speed performance is to use fast computational algorithm in a general purpose computers. Another way is to exploit the parallelism inherent in the computation for concurrent processing by a set of parallel processor. But, it is not cost effective to use a general purpose computer for a specific application. Also, general purpose computer used for their implementation required more space, large power and more computation time. With the development of very large scale integration (VLSI) technology it facilitates to digital signal processing (DSP) system designer to design a high performance, low cost and low power system in a single chip. The characteristic of VLSI system are that they offer greater potential for large amount of concurrency and offer an enormous amount of computing power within a small area [1, 2]. The computation is very cheap as the hardware is not an obstacle for VLSI system. But, the non-localized global communication is not only expensive but demands high power dissipation. Thus, a high degree of parallelism and a nearest neighbor communication are crucial for realization of high performance VLSI system [3]. Keeping this in view, high performance application specific VLSI systems are rapidly evolving in recent years. The special purpose VLSI systems maximize processing concurrency by parallel / pipeline processing and provides cost effective alternative for real- time application. Therefore, 2-D DWT is currently implemented in a VLSI system to meet the temporal requirement of real-time application. Keeping this fact in view, several design schemes have been suggested in the last two decades for efficient implementation of 2-D DWT in a VLSI system. Researchers have adopted different algorithm formulation, mapping scheme, and architectural design methods to reduce the computational time, arithmetic complexity or memory complexity of 2-D DWT structures.
However, the area-delay performance of the existing structures changes marginally. This is mainly due to the memory complexity, which forms a major hardware component of folded 2-D DWT structure [4].
Now a day, most of the information in Computer processing is handled online. This online information is either graphical or pictorial in nature, and the storage and communication requirements are immense [5]. Hence method of compressing the data prior to storage and transmission are of significant practical and commercial interest. Image compression means reducing the redundant amount of data required to represent a digital image. The Digital image compression in mathematical form can be defined as transformation of a 2-D pixel array by image, into a statistically uncorrelated data set. The transformation is applied on image prior to storage and transmission of Digital Image Data. The compressed image is reconstructed into original image by the process of Decompression [6]. Decompressed image can be an original image or approximation of it. Image compression is the technology for handling the increased spatial resolutions of today's imaging sensors and evolving broadcast television standards. Image compression plays an important role in many important and diverse applications including tele video conferencing, remote sensing, document and medical imaging, facsimile transmission and the control of remotely piloted vehicles in military, space, and hazardous waste management applications [7]. The application list is ever expanding on the efficient manipulation storage and transmission of different types of digital image such as binary images, gray-scale images, and color images etc.

II. DISCRETE WAVELET TRANSFORM

The resolution analysis limit and time-gradation district properties of the DWT has set up it as stunning resource for different applications, for instance, signal examination, picture pressure and numerical assessment, as communicated by Mallat. It is driven different exploration social occasions to make counts and gear models to execute the DWT.

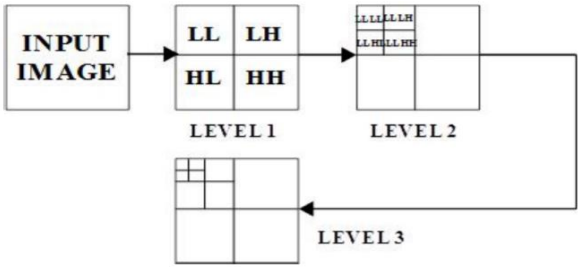

Figure 1: 3-level DWT of an image

In the standard convolution method for DWT, several Finite Impulse Response (FIR) aqueducts are applied in equal, to decide high_pass and low_pass aqueduct coefficients. Mallat's monolith estimation can be recycled to addresses the wavelet coefficients of an illustration in a couple of spatial headings.

The plans are by and large crumbled, and can be completely requested into consecutive and equal structures as discussed [7]. The designing discussed executes aqueduct bank structure capably, using digit consecutive pipelining. This building structures the explanation behind the gear execution of sub band rot, using the conversational DWT for JPEG 2000. An accustomed plan in whichever DWT break down the information picture is showed up underneath in Fig. 1.

Each crumbling level showed up in Fig. 2 incorporates two stages arrange performs level isolating, and stage 2 operate vertical permeate. In the primary level rot, the breadths of the data picture are N by N size and dissociate four standby federate L_L, H_H, L_H and H_L. L is imitate by Low and H is imitate by high frequency. Four standby federate are N/2 by N/2 size. L_L standby federate more dossier compared to other standby federate by virtue of L standby federate is boilerplate value of pixel and H standby federate is difference value of pixel. H_H standby federate is fewer dossiers. Derived the all standby federate is below:

$$x_{LL}^{J}(n_1,n_2)=\sum_{i_1=0}^{K-1}\sum_{i_2=0}^{K-1}h(i_1)h(i_2)x_{LL}^{J-1}(2n_1-i_1)(2n_2-i_2)$$

$$x_{LH}^{J}(n_1,n_2)=\sum_{i_1=0}^{K-1}\sum_{i_2=0}^{K-1}h(i_1)g(i_2)x_{LL}^{J-1}(2n_1-i_1)(2n_2-i_2)$$

$$x_{HL}^{J}(n_1,n_2)=\sum_{i_1=0}^{K-1}\sum_{i_2=0}^{K-1}g(i_1)h(i_2)x_{LL}^{J-1}(2n_1-i_1)(2n_2-i_2)$$

$$x_{HH}^{J}(n_1,n_2)=\sum_{i_1=0}^{K-1}\sum_{i_2=0}^{K-1}g(i_1)g(i_2)x_{LL}^{J-1}(2n_1-i_1)(2n_2-i_2)$$

Position of X_{LL} is 2-D data picture, J is boilerplate by decompose, h & g is boilerplate by low and high pass distill coefficient.

Explanatory and iterative reproduction calculations are the two philosophies in PC tomography for the examination of picture quality. Explanatory model is one in which it endeavors to locate the immediate answer for the picture remaking from the obscure projections. Investigative calculation is constrained to fragmented projections and scanty in see. In iterative reproduction, Image gauge is dynamically refreshed towards an improved arrangement. To help the iterative picture reproduction calculation, numerous methodologies have been introduced in writing. Among these techniques, the projection based strategy is an proficient and a twisting less method.

III. PROPOSED METHODOLOGY

In the DWT, the bi-balanced wavelets are realized by using the lifting strategy. The spatial territory and lifting system is used to create the lifting strategy. In the lifting plan, three guideline steps are generally played out that are, split, anticipate and update. The information picture tests x(n) are apportioned concerning the odd and even models in the split square. The channel is required for the odd and even guides to keep from the bothersome hailing. Lifting plan is performed by based kind of the channel.

Scaling step is used to find the low pass sub-gatherings of the odd and even tests. Channel utilization is changed into the growth cross sections in the lifting plan.

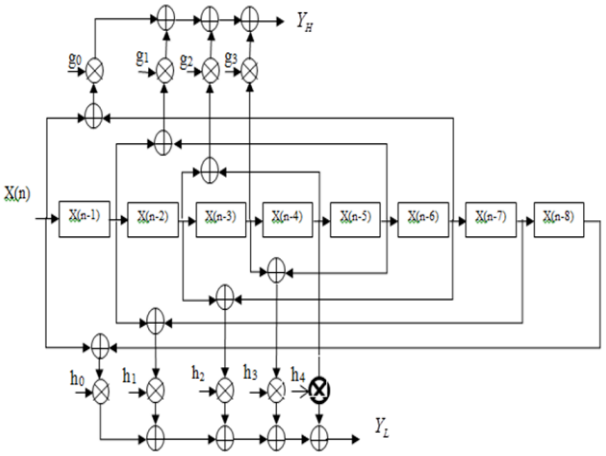

Figure 2: Multiplier Based 9/7 Coefficient based 1-D DWT

The image pressure is performed successfully by using the lifting plan, and the gear uses are significantly diminished by using the channels.

Inner product computation can be expressed by CSD. The DWT formulation using convolution scheme given in can be expressed by inner product, where the 1-D DWT formulation given in (1) – (2) cannot be expressed by inner product. Although, convolution DWT demands more arithmetic resources than DWT, convolution DWT is considered to take the advantages of CSD-based design. CSD formulation of convolution-based DWT using 5/3 biorthogonal filter is presented here.

According to (1) and (2), the 5/3 wavelet filter computation in convolution form is expressed as

$$Y_L=\sum_{i=0}^{4}h(i)X_n(i)$$

$$Y_H = \sum_{i=0}^{2} g(i) X_n(i)$$

The low-pass filter coefficients {h(i)} and high-pass filter coefficients {g(i)} of the 5/3 wavelet filter coefficient. Y_H is the high pass filter output and Y_L is the low pass filter output.

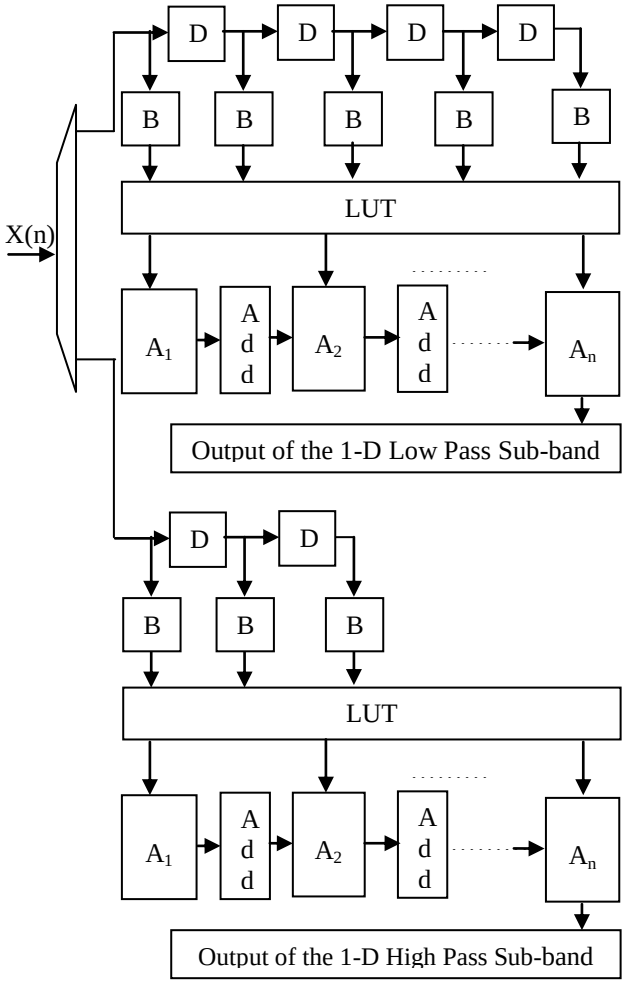

Figure 3: Block Diagram of 5/3 1-D DWT using CSD Technique

Where
B: Buffer
D: Delay flip flop
A_1: First output of the LUT
A_2: Second output of the LUT and add '0'
A_n: N output of the LUT and add (N-1) zero bit

IV. SIMULATION RESULT

The simulation was performed using XILINX 14.5i and ModelSim simulator. VHDL Descriptions consist of primary design units and secondary design units. The primary design units are the Entity and the Package. The secondary design units are the Architecture and the Package Body. Secondary design units are always related to a primary design unit. Libraries are collections of primary and secondary design units.

9/7 1-D DWT are represents primary and secondary design in fig. 4 & fig. 5.

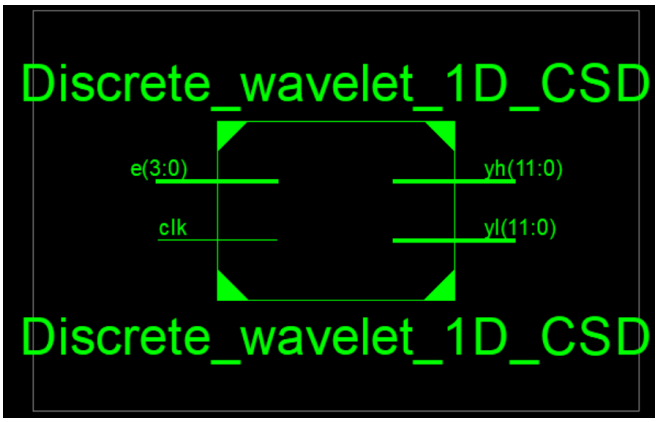

Figure 4: Primary Design of 1_D DWT including 9/7 coefficient

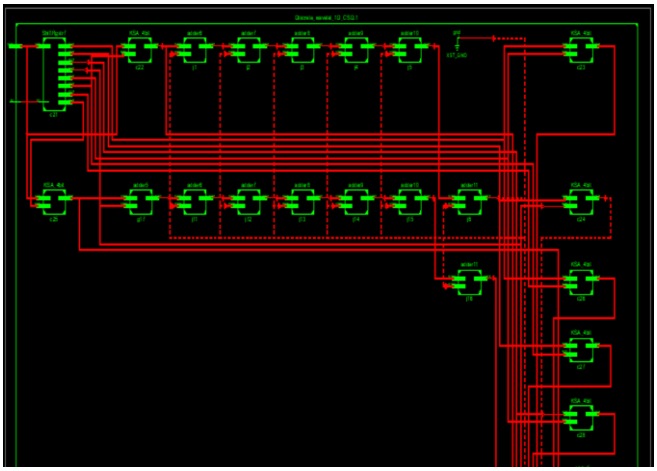

Figure 5: Secondary design of 1_D DWT including 9/7 coefficient

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Device utilization summary:
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Selected Device : 6vcx75tff484-2


Slice Logic Utilization:
 Number of Slice Registers:              35  out of  93120     0%
 Number of Slice LUTs:                  212  out of  46560     0%
    Number used as Logic:               210  out of  46560     0%
    Number used as Memory:                2  out of  16720     0%
       Number used as SRL:                2

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    231
   Number with an unused Flip Flop:     196  out of    231    84%
   Number with an unused LUT:            19  out of    231     8%
   Number of fully used LUT-FF pairs:    16  out of    231     6%
   Number of unique control sets:         2

IO Utilization:
 Number of IOs:                         29
 Number of bonded IOBs:                 29  out of    240    12%
Timing Summary:
---------------
Speed Grade: -2

   Minimum period: 1.380ns (Maximum Frequency: 724.638MHz)
   Minimum input arrival time before clock: 0.471ns
   Maximum output required time after clock: 11.439ns
   Maximum combinational path delay: 11.127ns
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Figure 6: Summary of 1_D DWT including 9/7 coefficient

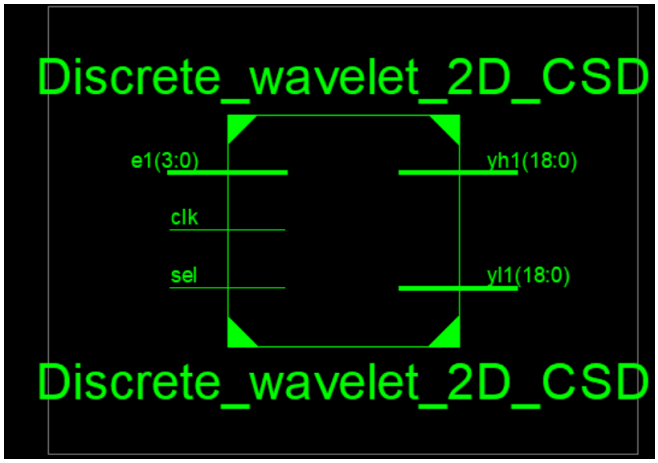

Figure 7: Primary Design of 2_D DWT including 9/7 coefficient

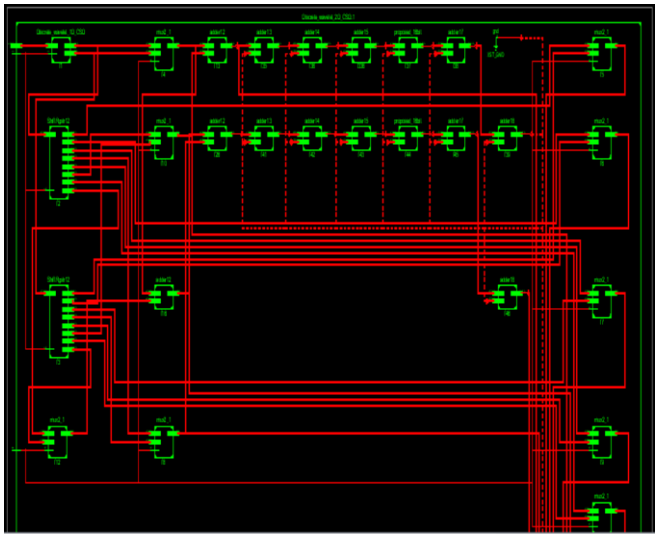

Figure 8: Secondary design of 2_D DWT including 9/7 coefficient

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Device utilization summary:
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Selected Device : 6vcx75tff484-2


Slice Logic Utilization:
 Number of Slice Registers:             227  out of  93120     0%
 Number of Slice LUTs:                  740  out of  46560     1%
    Number used as Logic:               740  out of  46560     1%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    834
   Number with an unused Flip Flop:     607  out of    834    72%
   Number with an unused LUT:            94  out of    834    11%
   Number of fully used LUT-FF pairs:   133  out of    834    15%
   Number of unique control sets:         1

IO Utilization:
 Number of IOs:                          44
 Number of bonded IOBs:                  44  out of    240    18%

Timing Summary:
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Speed Grade: -2

   Minimum period: 6.916ns (Maximum Frequency: 144.596MHz)
   Minimum input arrival time before clock: 6.847ns
   Maximum output required time after clock: 13.177ns
   Maximum combinational path delay: 13.108ns
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Figure 9: Summary of 1_D DWT including 9/7 coefficient

V. CONCLUSION

In this paper, CSD-based architecture for computation of 1-D and 2-D DWT is presented. The proposed CSD-based 1-D DWT structure involves significantly less logic resources than the similar existing multiplier-less designs and, it has less bit-cycle period than others. It is concluded that the CSD based 2_D DWT provide best result compared to previous design.

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