Study of 1-D and 2-D Discrete Wavelet Transform for Image Compression Application

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Abstract— Discrete wavelet transform (DWT) provides an efficient computing method for sparse representation of wide class of signals. The DWT only analyzes the lower frequency subbands, implicitly ignoring any information embedded in the higher frequency sub-bands. There are few applications where signal information equally distributed in entire signal spectrum such as ultrasound images, ECG and EEG images. The DWT is expressed in a generalized form know as discrete wavelet packet transform (DWPT) which analyzes both the low and high sub-bands with equal priority at every decomposition level. The DWT is currently implemented in very large scale integration (VLSI) system to meet the space-time requirement of various real-time applications. Several design schemes have been suggested for efficient implementation of 2-D DWT in a VLSI system. In this paper is study of DWT and analysis of best technique for design 2-D DWT.

Keywords: - *1*-D Discrete Wavelet Transform (DWT), Low Pass Filter, High Pass Filter, Xilinx Simulation

I. INTRODUCTION

The wavelet transform (WT) produces a time-frequency representation of the signal. It was developed to overcome the limitation of the short time Fourier transform (STFT), which can also be used to analyze non-stationary signals. While STFT gives a constant resolution at all frequencies, the WT uses multi-resolution technique by which different frequencies are analyzed with different resolutions. The wavelet analysis is similar to the STFT analysis. The signal to be analyzed is multiplied with a wavelet function similar to the multiplication of the window function in STFT, and then the transform of each segment is computed. A wavelet is a short oscillating function which contains both analysis function and the window function. In WT, time information is obtained by shifting the wavelet over the signal, while the frequencies are changed by contraction and dilatation of the wavelet function. The continuous wavelet transform (CWT) retrieves the time-frequency content information with an improved resolution compared to the STFT [1]. Discrete wavelet transform (DWT) is a mathematical tool that provides a new method for signal processing and decomposes a discrete signal in the time domain by using dilated / contracted and translated versions of a single basis function, named as prototype wavelet [2, 3].

DWT offers wide variety of useful features over other unitary transforms like discrete Fourier transforms (DFT), discrete cosine transform (DCT) and discrete sine transform (DST). Some of these features are; adaptive time-frequency windows, lower aliasing distortion for signal processing applications, efficient computational complexity and inherent scalability. Due to these features one dimensional (1-D) DWT and two dimensional (2-D) DWT are applied in various application such as numerical analysis, signal analysis and image coding.

DWT provides an efficient computing method for sparse representation of wide class of signals. The DWT only analyzes the lower frequency sub-bands, implicitly ignoring any information embedded in the higher frequency components [4]. In other word, DWT puts more emphasis on the low frequencies by continuously decomposing the signal in the low-frequency band. There are few applications where signal information equally distributed the entire signal spectrum such as ultrasound images, ECG and EEG images etc. In such cases, DWT is not able to analyze the signal to capture the required frequency component of interest. The DWT is expressed in a generalized form know as discrete wavelet packet transform (DWPT) which uses a generalized tree structure instead of a dyadic tree structure of DWT. The DWPT give equal priority to all signal components and analyzes both the low-pass and high-pass sub-bands at every decomposition level. As a result, DWPT provides a better signal analysis enabling it to achieve higher compression ratio and better scaling effects within an analysis framework compared to DWT. DWPT is used in wide range of bio-medical applications, medical imaging, healthcare applications [5, 6]. Few algorithms and computation schemes have been suggested during last three decades for efficient hardware implementation of DWT and DWPT.

II. LITERATURE REVIEW

Yuan-Ho Chen et al. [1], a brand-new QRS complex detection algorithm based on the discrete wavelet transform (DWT) is presented in this paper on a very large-scale integration chip. The first step in many aspects of electrocardiogram (ECG) analysis is to detect the QRS complex. Since the RR interval is used to evaluate heart rate variability (HRV), for instance, an effective QRS detection algorithm would have a significant impact on the subsequent HRV analysis steps. On the other hand, this study proposes a simple, dependable, low-power, and cost-effective QRS detection method and its VLSI implementation because wireless monitoring is still prohibitively expensive and reducing its cost and power consumption requires reducing the complexity of the algorithm. The quadratic

spline wavelet transform based wavelet packet decomposition is utilized in this instance to carry out the task of QRS complex detection. A novel noise level detection is carried out following a four-level DWT decomposition in order to improve the QRS complex. The proposed noise level detector would first determine the product of two of the four wavelet coefficients. Consequently, the processing stage also includes the execution of decision rules, the adaptive thresholding scheme, and the product of the two chosen wavelet coefficients. Manufactured on a 0.18-µm integral metal oxide semiconductor, the 1-KHz processor draws just 4.2 µW of force, and the chip region is just 0.83 mm2 . Additionally, 48 recordings from the MIT-BIH arrhythmia database are used to confirm the proposed method's detection accuracy (Se = 99.57%, +P=99.59%), indicating that the proposed QRS detector may be able to detect QRS complexes with high accuracy and low cost.

Jhilam Jana et al. [2], for the one-dimensional (1-D) and two-dimensional (2-D) discrete wavelet transform (DWT), a comprehensive analysis of VLSI architectures is presented in this paper. Additionally, three related architectures are proposed. There are three types of 1-D DWT and inverse DWT (IDWT) architectures: B-spline, lifting, and convolutional models. They are talked about with regards to equipment intricacy, basic way, and registers. Concerning the 2-D DWT, the most pressing issues are the substantial amount of frame memory access and die area occupied by the embedded internal buffer. Different external memory scan techniques are used to classify and examine the two-dimensional DWT architectures. The internal buffer's implementation issues are also discussed, and some real-world experiments demonstrate that the internal buffer's area and power are highly correlated with memory technology and working frequency rather than just the required memory size. The overlapped stripe-based scan method and the B-spline-based IDWT architecture are also suggested in addition to the analysis. Last but not least, we suggest a one-level 2-D DWT architecture that takes full advantage of the analysis's many advantages and is both adaptable and effective.

W. Yan et al. [3], a more accurate and resource-efficient "QRS" detector is what we propose in this paper. We used a pipeline-scheduled, reconfigurable time-sharing computation unit inspired by the folded architecture's approach. We developed the position calibration unit (PCU) on the basis of the data compression method in order to more precisely locate the position of the "R" peak and to reduce the need for additional hardware. Using the Verilog programming language, the proposed architecture was implemented on the Xilinx Zynq-7000. On the MIT-BIH database, the proposed architecture has the best performance when compared to current designs, with a sensitivity of 99.76 percent, a precision of 99.85 percent, and a detection error rate of 0.40 percent. Additionally, the proposed architecture reduces power consumption, storage memory, and computing resources by 13.35 percent, 1.28 percent, and 4.35 percent, respectively.

Z. Zhang et al. [4], a real-time QRS-detection algorithm and a dynamic tracking-based 12-bit successive approximation register (SAR) ADC are proposed. There are two tracking windows in the dynamic tracking algorithm that are right next to the prediction interval. The prediction code is updated and the subrange interval is automatically adjusted by this algorithm, which is able to locate the variation range of the input signal. Real-time QRS-detector and synchronous time sequential ADC are incorporated into the QRS-complex detection algorithm. The chip is made using a 0.6 V supply and the standard 0.13 m CMOS process. At 10k Hz sample rate and 41.5 Hz sinusoid input, measurements reveal that the proposed ADC has an effective number of bits (ENOB) of 10.72 and a spur-free dynamic range (SFDR) of 79.63 dB. The limits of the DNL and INL are -0.67/1.43 LSB and -0.62/0.62. In the ideal scenario, the ADC achieves a FoM of 48 fJ/conversion step. Additionally, the prototype successfully extracts the heartbeat signal when subjected to ECG signal input.

J. Li et al. [5], this paper introduces power reduction strategies and considerations at the system level of design, where we have the greatest potential to influence power, with the goal of lowering the power consumption of wearable healthcare devices based on electrocardiography. It focuses on algorithm design and implementation, data acquisition, and transmission with limited resources in particular. On the basis of metrics like sensitivity, positive predictivity, power consumption, parameter selection, and time delay, nine existing algorithms are thoroughly examined for their suitability for on-sensor QRS feature detection. A direct memory access (DMA) list approach and low-level register manipulations for task delegation are used to optimize data acquisition on CPU-based IoT systems and reduce current consumption by a factor of three. Additionally, the batch size, buffer size, sampling rate, and acquisition data rate are all optimized. The impact of on-sensor versus off-sensor processing is investigated in order to cut down on the amount of power required for data transmission. While the experiments in this work were carried out on a generic low-power wearable platform and focused on CPU-based systems, the design optimization and considerations suggested in this work could be extended to custom designs, which would make it possible to conduct additional research into optimizing the QRS detection algorithm for wearable devices.

B. Mishra et al. [6], the vital data contained in an electrocardiogram (ECG) signal can be used to identify a variety of arrhythmia conditions. In this work, we have fostered a calculation to identify the R pinnacles of the ECG signal in light of the Skillet Tompkins Calculation. The work has also been improved to a first-level approximation for the purpose of identifying various arrhythmia conditions. The Q and S points that are based

on the R-peaks are also found in order to compute the QRS complex. The MIT/BIH arrhythmia database is used as a reference for R peak annotations and as a source for ECG signals in order to verify that the proposed algorithm works. The metric of False Detection Rate (FDR) of 1.289%, Sensitivity of 99.492%, and Positive Predictivity of 99.293% is provided by the algorithm. In order to extract the P and T waves from the signal, the entire QRS complex is reset to zero after it has been detected. As a result, this work offers a unique strategy for real-time P, Q, R, S, and T wave detection of an ECG signal. To demonstrate the approach's efficacy, the algorithm is further ported to a low-cost ECG monitoring patch.

G. Da Poian et al. [7], have wireless body sensor networks, compressive sensing (CS) has recently been used as a low-complexity compression framework for long-term electrocardiogram (ECG) signal monitoring. ECG signals can be recorded over a long period of time for diagnostic purposes and to track the progression of a number of common diseases. By calculating the distance between QRS complexes (R-peaks) in the ECG signal, beat-to-beat intervals, in particular, can be derived from the signal and provide important clinical information. For uncompressed ECG, a variety of R-peak detection techniques are available. However, with relatively complex optimization algorithms and possibly a significant amount of energy consumption, signal reconstruction can be carried out with compressed sensed data. Without reconstructing the entire signal, this paper addresses the issue of estimating heart rate from CS ECG recordings. Methods: We consider a framework in which CS linear measurements are used to represent the ECG signals. The correlation between the compressed ECG and a known QRS template is used to estimate the QRS locations in the compressed domain. The proposed method proves to be very convenient for low-power real-time applications because it does not require reconstruction.

T. Tekeste et al. [8], Internet of Things (IoT) medical wearable devices require an ultra-low power electrocardiogram (ECG) processing architecture that is accurate enough. An innovative real-time QRS detector and an ECG compression architecture for IoT healthcare devices are presented in this paper. An A-CLT, or absolute-value curve length transform, is proposed to effectively improve QRS complex detection while using as few hardware resources as possible. Only adders, shifters, and comparators are required in the proposed architecture, which eliminates multipliers altogether. QRS recognition was achieved by involving versatile limits in the A-CLT changed ECG signal, and accomplished a responsiveness of 99.37% and the predictivity of 99.38% while approved utilizing Physionet ECG data set. The proposed architecture also includes a lossless compression method that makes use of entropy encoding and the ECG signal's first derivative. Utilizing the MIT-BIH database, the evaluation produced an average compression ratio of 2.05. With minimal hardware resources, the proposed QRS detection architecture addresses nearly all ECG signal artifacts, including baseline drift, low-frequency noise, and high-frequency interference.

III. COMPUTATION SCHEME OF DWT

DWT decomposes input signal spectrum into two sub-bands. These two sub-bands are known as low-pass sub-band and high-pass sub-band. The input signal is filtered by a lowpass filter to obtain the low-pass sub-band where the same input signal is filtered by the highpass filter to obtain the high-pass sub-band. The pair of low-pass and high-pass filters form a quadrature mirror filter (QMF) for perfect signal reconstruction. The low-pass and high-pass filters are realized using short length finite impulse response (FIR) filter. As shown in Figure 1, the low-pass filter and high-pass filter forms a two-channel filter bank and performs down-sampled filter computation on the input signal to obtained the low-pass subband output (ul(n)) and high-pass sub-band output (uh(n)). The 1-D DWT computing unit is represented by a two-channel filtering unit comprised of a low-pass filter (LPF), one high-pass filter (HPF)), and a pair of down samplers. The low-pass and high-pass filter computation of DWT are performed using (i) convolution scheme and (ii) lifting scheme.

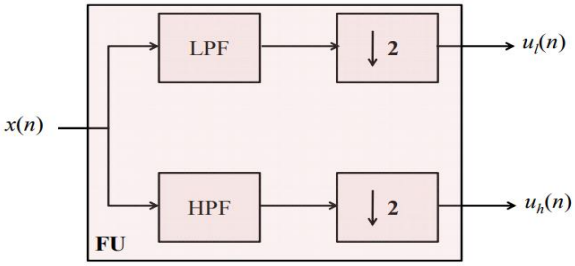

Figure 1: Block diagram of filtering unit (FU) of 1-D DWT

DWT computation using convolution scheme:- In convolution scheme, the low-pass and high-pass filter output of an filtering unit (FU) are calculated using the expressions

$$u_l(n) = \sum_{i=0}^{k_1-1} h(i)x(2n-i)$$

$$u_h(n) = \sum_{i=0}^{k_2-1} g(i)x(2n-i)$$

Where, k1 is the length of low-pass filter, k2 is the length of high-pass filter, x(n) is the input signal. ul(n) and uh(n) are the low-pass and high-pass subband components, respectively. h(n) and g(n) are, respectively, low-pass and high-pass filter coefficients of wavelet filter. Wavelet filters are classified as, orthogonal and bi-orthogonal wavelets. The wavelet filter coefficients satisfy the orthogonal property is known as orthogonal

wavelet, where the biorthogonal wavelet filter coefficients satisfy the orthonormal property in addition to orthogonal property. The orthogonal low-pass and high-pass filters are, asymmetric and have same lengths, where the low-pass and the high-pass filters of bi-orthogonal wavelet are symmetric and different in length.
DWT computation using lifting scheme:- The lifting scheme was proposed by Sweldens (1996). According to lifting scheme, the low-pass and high-pass filter computation of 1-D DWT are decomposed into lifting steps. The basic principle of lifting scheme is to factorize the polyphase matrix (P(z)) of the wavelet filters comprising of low-pass and high-pass bi-orthogonal filter into a sequence of alternating upper and lower triangular matrices and a constant diagonal matrix. This leads to wavelet computation by means of banded-matrix multiplications [8, 9]. The lifting based DWT has many useful properties such as symmetric forward and inverse transform, in-place computation, integer-to-integer transform and requires less computation than convolution based DWT [10]. Let H(z) and G(z) are the system function of low-pass and high-pass bi-orthogonal wavelet filters. H(z) can be decomposed into He(z) and Ho(z), where He(z) and Ho(z) represents the system function of even and odd part of the impulse response h(n) of low-pass wavelet filter. Similarly, Ge(z) and Go(z) represents the system function of even and odd part of the impulse response g(n) of high-pass wavelet filter. The system function (P(z)) of FU can be expressed as

$$\mathbf{P}(z) = \begin{bmatrix} H_e(z) & G_e(z) \\ H_o(z) & G_o(z) \end{bmatrix}$$

IV. VLSI SYSTEM

DWT algorithms can be implemented in a programmable system such as general purpose computer or digital signal processor. These programmable systems use a fixed computing architecture and perform arithmetic operations sequentially and they offer limited throughput for computationally intensive algorithms such as DWT. However, DWT algorithms can be implemented general purpose programmable systems for high-throughput applications employing parallel processing. Engaging general purpose programmable system to perform a specific task is not cost-effective. Besides, general purpose computing systems occupy substantial amount of space and consumes power which makes the deployment of signal processing system difficult in a resource constrained and hostile environment. In recent years, there is tremendous growth of portable and wireless devices in various applications. Portable and wireless devices are resource and power constrained, and uses complex signal processing algorithms including DWT. Besides, high-throughput rate, low-area and low-power are considered the key requirements of systems implementing digital signal processing algorithms especially for portable and wireless devices which are battery operated. Therefore, realization of DWT in resource and power constrained environment and delivering real-time performance is a challenging task for portable and wireless devices.
With the advancement of VLSI technology, high density and low-cost memory chips are rapidly evolving in recent years. Field programmable gate array (FPGA) is a programmable logic device. FPGA offers high capacity programmable devices for realization of complex DSP algorithms. FPGA uses a fixed architecture and offers specific types of memory and logic resources for realization of digital systems. On the other hand, modern synthesis tools offer a wide range of logic and memory components for realization of application specific integrated circuit (ASIC) systems. Therefore, ASIC based dedicated system offers higher-performance and consumes less-power compared to FPGA based dedicated systems. However, ASIC system does not allow reusing its resources through programming unlike the FPGA. Therefore, FPGA offers rapid prototyping the DSP algorithm with lesser performance than the ASIC. In general ASIC implementation is preferred for computation intensive algorithms and high volume applications.

V. IMAGE COMPRESSION UISNG DWT

In the course of past few years, the wavelet transform has gained massive amounts of popularity in the research area and commercial industries, because of their powerful image compression techniques. Numerous wavelets based compression techniques, also known as sub-band coding, are more powerful and popular than DCT algorithms. As the image is not required to be divided in to blocks, the wavelet theory has advantage over signal distortion, due to variable length of wavelet coding schemes. Wavelet-based coding offers sequential image transmission. They are more resilient to decoding errors and transmission errors. The wavelets are highly suitable for application which requires good flexibility of scaling and reasonable amount of distortion. This is because of the characteristic multi resolution nature of wavelets.

(a) (b)

Figure 2: (a) Original Image, and (b) Reconstructed Image with only DC components

VI. CONCLUSION

DWT provides an efficient computing method for sparse representation of wide class of signals. The DWT only analyzes the lower frequency sub-bands, implicitly ignoring any information embedded in the higher frequency components. There are few applications where signal information equally distributed the entire signal spectrum such as ultrasound images, ECG and EEG images etc. The DWT is expressed in a generalized form know as discrete wavelet packet transform (DWPT) which analyzes both the low-pass and high-pass subbands in equal priority at every decomposition level. As a result, DWPT provides a better signal analysis enabling it to achieve higher compression ratio and better scaling effects within an analysis framework compared to DWT. The DWT is widely used in various signal and image processing applications such as image coding, image compression and speech coding etc. DWPT is used in wide range of bio-medical applications, medical imaging, and healthcare applications. Efficient realization of DWT/DWPT in dedicated VLSI system has great practical interest for low-power and resource constrained applications. Several computation schemes and architectural designs have been suggested during last three decades for efficient hardware implementation of DWT and DPWT.

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