Survey of Arithmetic and Logical Unit based on Reversible Logic Gate Structure

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Abstract- Power crisis is a vital problem in today's world. In recent years, the growing market of electronic systems suffers from power dissipation and delay removal problem. Bennett et al. proved that the one-to-one mapping between the inputs and outputs of reversible circuit drastically reduces the power consumption and delay consumed of a circuit. There are four major design parameters of reversible circuits. First is the gate count which is the number of gate are used in the circuit. Second is the quantum delay. Third is the number of ancilla inputs which are constant inputs which are used to maintain the reversibility of the device. Fourth is the number of garbage outputs i.e. output signals which are not used as inputs to other gates and are only there to maintain reversibility. We study of arithmetic and logical unit based on reversible gate and parameter in this paper.

Keywords—Reversible Gates, Logical Unit, Garbage Output, Quantum Cost

I. INTRODUCTION

Reversible logic could also help to potentially recover and retain a fraction of the signal energy that can be reused for subsequent operations by doing the computation using the forward path and then undoing the computation using the backward path. These concepts have been implemented in CMOS to save significant amount of energy dissipation even close to 90% using the concepts such as reversible energy recovery logic (RERL) etc. [1, 2]. Reversible logic has also promising applications in online and offline testing of faults. For example, it has been proved by researchers that for reversible logic circuits, the test set that detects all single stuck-at faults can also detect multiple stuck-at faults [3]. Further, such a logical structure must possess the same number of inputs and outputs and a one-to-one mapping between the input and output states. Any device designed to these constraints is known as a reversible logic device.

A few critical measurements should be considered in the outline of reversible circuits the significance of which should be talked about. The steady contribution to the reversible quantum circuit is called the ancilla info qubit (ancilla information bit), while the trash yield alludes to the yield which exists in the circuit just to keep up coordinated mapping however is not an essential or a helpful yield. Quantum PCs of numerous qubits are to a great degree hard to acknowledge in this manner the quantity of qubits in the quantum circuits should be minimized.

The importance of minimizing the garbage and ancilla bits could be best illustrated with an example. Suppose there is a need to realize 6 inputs and 4 outputs function in a quantum computer and the design requires 6 additional garbage outputs (that is have the 4 constant inputs). This will result in a reversible function having 10-inputs and 10 outputs. Suppose the best realizable quantum computer due to technology limitations had only 7 qubits, thus we will not able implement the required design. This sets the major objective of optimizing the number of ancilla input qubits and the number of the garbage outputs in the reversible logic based quantum circuits. Additionally, there are number of implementation platforms that are being explored for physical implementations for qubits and quantum gates [4].

Some of these implementation platforms are trapped ions, spintronics, superconducting circuits, linear optics/ photonics, quantum dots, etc. [5]. There is no clear winner and it is not sure which implementation technology will be the future of the quantum computers. Thus there is a need of technology independent design and synthesis of reversible logic circuits that are applicable to quantum computing. The reversible circuit has other important parameters of quantum cost and delay which need to be optimized. The quantum cost of a design is the number of 1x1 and 2x2 reversible gates used in its design thus can be considered equivalent to number of transistors needed in a conventional CMOS design.

II. LITERATURE SURVEY

S.Vijayashaarathi et al. [1], the advanced world, computerized gadgets frameworks are reduced and quicker. However, the serious issue of these frameworks are power scattering. The Power scattering have various variations like a static power, dynamic power, short out and spillage current dissemination. In VLSI Plan, the power utilization assumes a significant part. To limit the power dispersal there are various low power strategies are utilized, for example, a multi-Vth technique, clock gating and reversible rationale entryway strategy. The significant benefits of a circuit planning utilizing a reversible rationale doors will be viable with a possible assets and the reversible Entryways have a zero intensity dispersal. The Number juggling and Coherent Unit is crucial piece of figuring frameworks. This paper, presents a Plan of low trash Reversible Math and legitimate unit plan for registering framework and the plan incorporates Viper, subtractor and Multiplier blocks. The usefulness of a plan execution, waste results, Quantum cost are examined. The proposed plan has a 11 junk yields and 57 quantum costs. The plan is coded on Verilog HDL and combined, recreated by a Xilinx programming.

Safaiezadeh et al. [2], quantum speck cell automata (QCA) innovation is viewed as one of the most appropriate substitutions to decrease the CMOS-based

advanced circuit plan issues at the nanoscale because of its little size, quick, inertness and exceptionally low power utilization. One of the fundamental parts of microchips is the math rationale unit (ALU) and at the end of the day, it goes about as the core of chip. This paper presents a QCA innovation based reversible ALU unit utilizing fundamental reversible blocks and an original reversible block to be specific BS1 Block. The proposed block performs rationale and number juggling activities in the proposed plot. The reproductions of the proposed plan are done by QCA Fashioner. As per the recreated results, the proposed structure has a 35%, 27% and 30% improvement in quantum cost, the quantity of cells and the involved region in contrast with the past led explores, separately.

Swathi et al. [3], quantum is an arising innovation in ongoing PCs. Reversibility is the fundamental benefit of quantum PCs. In traditional PCs, the calculation is irreversible for example the information pieces are lost once the rationale block creates the result and info bits can't be reestablished yet it very well may be finished in reversible calculation in light of the fact that in reversible calculation the data sources and results have a coordinated correspondence. Hence, a reversible door information really might not set in stone from their result which prompts less power utilization. Subsequently the intricacy of the computerized circuits can be decreased by utilizing reversible registering. In quantum PC to perform reversible activities, we really want to execute the reversible doors utilizing quantum entryways. In this paper, we examined different reversible rationale entryways like Feynman, Toffoli, R, Peres and TR doors utilizing essential quantum doors like CNOT, Pauli, Trade entryways and their execution utilizing IBM quantum experience.

Bhattacharya et al. [4], in this period of nanometer semiconductor hubs, the semiconductor scaling and voltage scaling are no longer in accordance with one another, prompting the disappointment of the Dennard scaling. Subsequently, it represents an extreme plan challenge. Reversible registering assumes an imperative part in applications like low power CMOS, nanotechnology, quantum figuring, optical processing, advanced signal handling, cryptography, PC illustrations and some more. The essential purposes behind planning reversible rationale are lessening the quantum cost, significance of the circuits and the trash yields. It is difficult to decide the quantum processing without executing the reversible calculation. This paper will address the writing study in light of a few papers on combinational circuits utilizing reversible registering and furthermore the future degree is to be examined.

Jeevitha K et al. [5], in this short, a low-intricacy and novel strategy is proposed to proficiently carry out the location age hardware of the 2-D deinterleaver utilized in the WiMAX transreceiver utilizing the Xilinx field-programmable entryway exhibit (FPGA). The floor capability related with the execution of the means, expected for the stage of the approaching piece stream in channel interleaver/deinterleaver for IEEE 802.16e standard is extremely challenging to carry out in FPGA. A straightforward calculation alongside its numerical foundation created in this brief, wipes out the necessity of floor capability and consequently permits low-intricacy FPGA execution. The utilization of an inside multiplier of FPGA and the sharing of assets for quadrature stage shift keying, 16-quadrature-plentifulness regulation (QAM), and 64-QAM adjustments alongside all conceivable code rates makes our way to deal with be novel and profoundly effective when contrasted and customary look-into table-based approach. The proposed approach shows huge improvement in the utilization of FPGA assets. Comprehensive reenactment has been completed to guarantee matchless quality of our proposed work.

Radha et al. [6], presently a-days, reversible rationale is getting gigantic interest among the IC fashioner in light of the fact that it consumes less power. Reversible rationale has been found in applications like Advanced signal handling, DNA and quantum processing and rapid VLSI plan. The execution of reversible rationale contains number of reversible rationale doors. In this work, a multiplier is planned utilizing HNG entryway. A productive rapid multiplier has been proposed utilizing verilog coding and Rhythm 180 nm innovation is utilized for its execution. Contrasted with the current multiplier, the proposed multiplier consumes less power and similarly less quantum cost. Thus, the proposed multiplier brings about less power utilization without forfeiting the speed.

Swamynathan et al. [7], a Number juggling rationale Unit (ALU) is utilized in math, coherent capability in all processor. It is likewise a significant subsystem in advanced framework plan. Math Rationale Unit (ALU) is one of the main parts of any framework and is utilized in numerous apparatuses like number crunchers, cells, and PCs. A 32-cycle ALU was planned utilizing Verilog HDL with the consistent doors, for example, AND or potentially for every the slightest bit ALU circuit. The plan was executed in Xilinx. It can work quick than the ALU processor utilizing less power. The plan of an ALU and a Reserve memory for use in a superior execution processor was inspected. Reversible rationale fundamental as of late on the grounds that it has capacity to diminish the power dissemination which is principal necessity in low power plan. ALU which are planned utilizing non reversible rationale doors consume more power. So there is a requirement for lesser power utilization and the reversible rationale has been assuming crucial part during ongoing years for low power VLSI Plan strategies. This method assists in decreasing with controlling utilization and power dissemination. This paper presents an execution of ALU in view of reversible rationale while contrasting it with an ALU design with the typical rationale entryways. Every one of the modules are recreated in modelsim SE 6.4c and blended utilizing Xilinx ISE 14.5. ALU which is planned utilizing non reversible rationale doors consume more force of around 0.312 mw and the execution of ALU in view of reversible rationale lessens the power utilization during tasks to around 5.1 rates.

Shukla et al. [8], computerized circuits have been fundamentally applied to each field of life. Low power effective frameworks are the need of this period. Reversible rationale approach is the fundamental result of this need. Reversible innovation is broadly material in the area of nanotechnology, low power CMOS plan, optical figuring and so on. Reversible methodology fundamentally means to upgrade any advanced circuit with reversible plan units. Here, we propose an effective way to deal with plan N-digit Viper/subtractor utilizing reversible methodology. In light of proposed N-bit Snake/Subtractor plan we have additionally thought about 4-bit, 8-digit and 16-cycle circuits with the current plans. Proposed plans are reenacted and combined with Xilinx Austere 3E for Gadget XC3S500E at 200 MHz recurrence.

Shukla et al. [9], computerized circuits have been essentially applied to each field of life. Low power effective frameworks are the need of this period. Reversible rationale approach is the fundamental result of this need. Reversible innovation is broadly material in the area of nanotechnology, low power CMOS plan, optical figuring and so on. Reversible methodology fundamentally means to upgrade any advanced circuit with reversible plan units. Here, we propose an effective way to deal with plan N-digit Viper/subtractor utilizing reversible methodology. In light of proposed N-bit Snake/Subtractor plan we have additionally thought about 4-bit, 8-digit and 16-cycle circuits with the current plans. Proposed plans are reenacted and combined with Xilinx Austere 3E for Gadget XC3S500E at 200 MHz recurrence.

Silviyasara et al. [10], to work on the presentation of opposite converter, the buildup numeral framework is proposed utilizing Han-Carlson structure with abundance one unit. They produce and proliferate signals are sent to the radix tree and the information structure is utilized to store the strings that permits quick gaze upward. Han-Carlson decreases the intricacy and it upholds the immense number of adders with elite execution activity. This strategy utilizes less number of computerized administrators by changing the quantity of stages. It proficiently decreases the deferral and it expands the timing, speed and power utilization. Han-Carlson structure is extremely helpful for applications like cryptography, the number juggling process, security purposes, worldwide extraordinary identifiers, PC programming.

III. REVERSIBLE GATES

Reversible rationale is picking up significance in regions of CMOS configuration in light of its low power dissemination. The conventional entryways like AND, OR, XOR are all irreversible doors. Consider the instance of conventional AND entryway. It comprises of two inputs and one yield. Subsequently, one piece is lost every time a calculation is completed. As indicated by reality table appeared in Fig.1, there are three inputs (1, 0), (0, 1) and (0, 0) that compares to a yield zero. Subsequently it is unrealistic to decide interesting information that brought about the yield zero. With a specific end goal to make an entryway reversible extra info and yield lines are added so that a balanced mapping exists between the information and yield. This keeps the loss of data that is fundamental driver of force scattering in irreversible circuits. The info that is added to an m x n capacity to make it reversible is known as steady information (CI). Every one of the yields of a reversible circuit need not be utilized as a part of the circuit [8]. Those yields that are not utilized as a part of the circuit is called as trash yield (GO). The number of garbage output for a particular reversible gate is not fixed. The two main constraints of reversible logic circuit is

- Fan out not allowed
- Feedbacks or loops not allowed.

○ BASIC REVERSIBLE GATES

Several reversible logic gates are used in previous design. In figure 1, show the block diagram of two input (A, B) and two output (P, Q) Feynman gate.

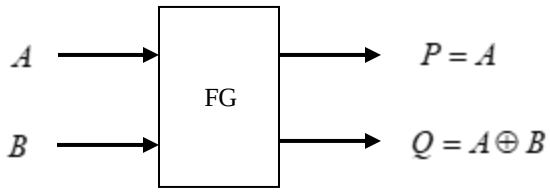

Figure 1: Feynman gate [1]

In figure 2, show the block diagram of the three inputs (A, B, C) and three output (P, Q, R) Fredkin gate.

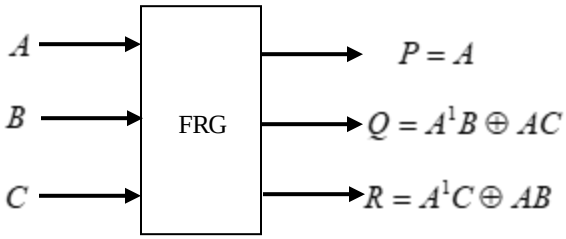

Figure 2: Fredkin gate

Figure 3 shows the Peres gate. A portion of the 4x4 doors are intended for executing some imperative combinational capacities notwithstanding the fundamental capacities. The vast majority of the aforementioned entryways can be utilized as a part of the outline of reversible adders.

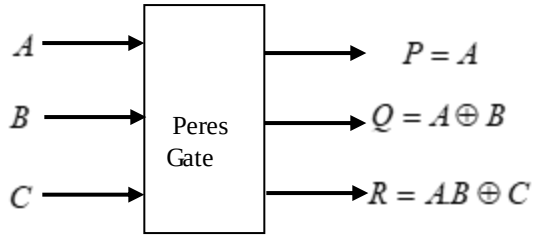

Figure 3: Peres gate

The HNG gate, presented in [10], produces the following logical output calculations:

$$P = A \quad (1)$$

$$Q = B \quad (2)$$

$$R = A \oplus B \oplus C \quad (3)$$

$$S = (A \oplus B).C \oplus (AB \oplus D) \quad (4)$$

The quantum cost and delay of the HNG is 6. At the point when D = 0, the consistent estimations created on the R and S yields are the required total and complete operations for a full snake. The quantum representation of the HNG is exhibited in Fig. 4.

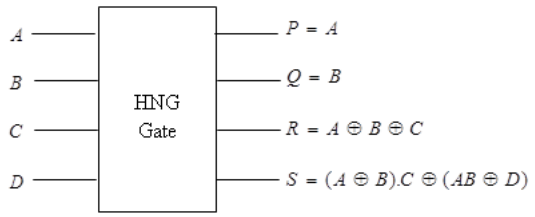

Figure 4: Block Diagram of the HNG Gate

A new programmable 4x4 reversible logic structure Peres And-OR (PAOG) gate is presented which produces outputs

$$P = A \quad (5)$$

$$Q = A \oplus B \quad (6)$$

$$R = AB \oplus C \quad (7)$$

$$S = (AB \oplus C).C \oplus ((A \oplus B) \oplus D) \quad (8)$$

Figure 5 shows the block diagram of the PAOG gate. This gate is an extension of the Peres gate for ALU realization.

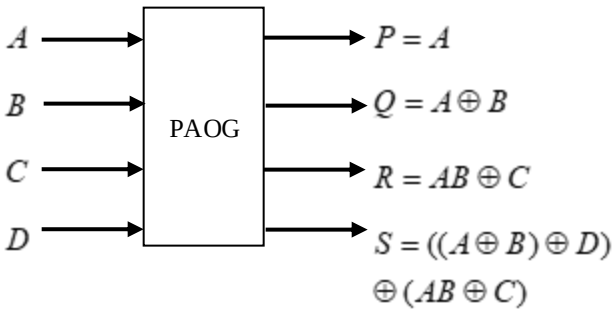

Figure 5: Block Diagram of the PAOG

IV. REVERSIBLE PARAMETER

Some of the reversible gate are NOT Gate, CNOT/ Feynman Gate, Toffoli Gate, Fredkin Gate and Peres Gate. Important parameters of any reversible circuit are as follows:

Gate Count (GC): The number of gates used to realize reversible circuit.

Garbage Outputs (GO): The number of unused outputs in a reversible logic. The inputs regenerated at the outputs are not garbage outputs.

Ancilla Inputs (AI): The number of input kept constant at either 0 or 1.

Quantum Cost (QC): The cost of the circuit in term of cost of a primitive gate.

Delay: It corresponds to number of primitive quantum gates in the critical path of the circuit.

V. PROPOSED METHODOLOGY

The architecture of the proposed reversible processor is shown in Figure 6. In this figure design the overall structure of the reversible ALU has been divided into small components.

- Layout the data bus to handle all of the operations of the reversible ALU.
- Design the reversible realizations of the multiplexer.
- Design the reversible memory circuits such as d_ff and comparator.
- Design the arithmetic circuits such as multiplier, adder and sub-tractor.

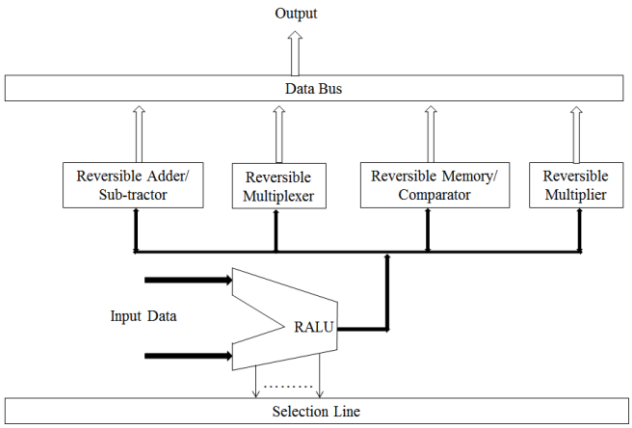

Figure 6: Flow Chart of Proposed Arithmetic Logic Unit

VI. CONCLUSION

We have tried the arithmetic logic unit is consist of adder, multiplier, memory element, sub-tractor and multiplexer in different reversible gate. The proposed reversible ALU design will have analyzed on Xilinx 14.1 Spartan-3 device family. The proposed design will have compared in terms of maximum combinational path delay (MCPD) and quantum cost with the existing reversible ALU. We can also design 4-bit to 8-bit reversible ALU.

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