Delay Efficient VLSI Architecture for Wavelet Decomposition using Complex Multiplier

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Abstract— In this paper, high performance VLSI architectures for complex multiplier (CM) based 1-D and 2-D Discrete wavelet transforms (DWTs) are proposed. The proposed logic used for area efficient CM based DWT is to perform the whole operation with one processing element. Similarly, the proposed logic used for delay efficient CM based DWT is to perform the whole operation with multiple processing elements in parallel. In both the cases, the processing element consists of one adder and one proposed multiply add design. The proposed and existing design based 1-D and 2-D CM based DWTs are implemented with Xilinx software. The guideline focus of this investigation striving is to decide capable VLSI structures, for the gear use of the 9/7 and 5/3 DWT, using complex multiplier (CM) and improving the speed and hardware complicities of existing plans.

Keywords: - 1_D DWT, 2_D DWT, CM

I. INTRODUCTION

Of late, there have been basic undertakings by the business and authorities to make PC tomography imaging structures as far as new getting ready and multiplication figurings. A CT scanner has broad mindfulness with respect to improve both gear and programming to enable significant standards CT pictures to be made. The quality and speed with which they are created is somewhat a direct result of improvements in capable picture propagation counts [1].

This field is up 'til now creating and new counts are by and by used that change in accordance with the variety of issues like model and handle the projection upheaval, low identifier check, non-uniform game-plans of sensor, scatter, etc., Two important request in picture entertainment computations are methodical and Iterative estimation. Analytical model is computationally compelling and speed with the couple of assumptions like scanner geometry and rough data, for instance, cognizance of the projections and quiet estimations, etc. [2, 3].

To achieve better picture quality from comparable rough data, continuously down to earth speculations about scanner geometry and upheaval estimations must be made. This is done in the more computationally complex iterative revamping methods. Such iterative diversion techniques may realize longer revamping occasions yet also in extensively less picture commotion from a comparative rough data through progressively complex showing of discoverer response and the quantifiable lead of the estimations. Iterative multiplication estimation is a lot of
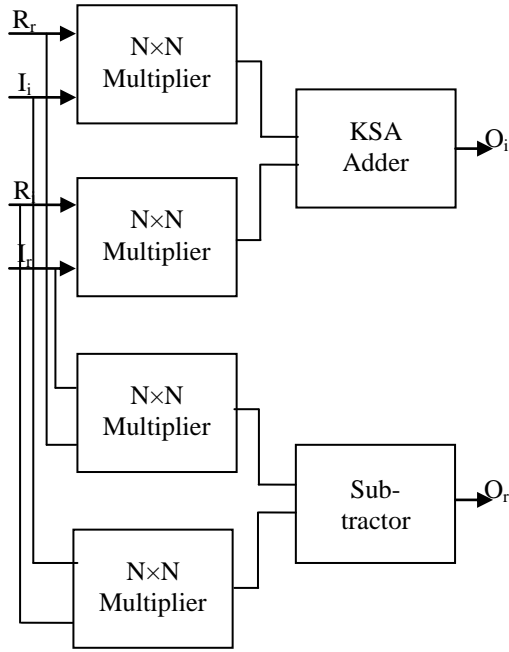
capable than logical computation. Among which, Iterative propagation is considered in this assessment. By and by a-days, Iterative generation is playing a genuine activity in PC tomography to improve nature of picture and decrease the development old rarities. Along these lines a lot of exploration work has been done as such as to improve the reproduced picture in both visual and error assessment [4].

The DWT is apparently the best methodology in the field of Image weight and Image coding. Joint Pixel Master Group (JPEG) is the essential standard method for the image pressure. The coding ability and picture quality is capable in the DWT when appeared differently in relation to the standard DCT. JPEG is explained the irreversible sort of the Discrete Wavelet Transform for the beneficial picture pressure. Mechanized Image is one of the standard requirements for both persistent applications additionally as examination zone. The essential of the Image pressure is commonly high on account of the traffic conveyed by the media sources. The One Dimensional what's progressively, Two-Dimensional Discrete Wavelet Transform is the key limit with respect to picture getting ready. The Multi-objectives signal assessment is cultivated in both time and repeat space in DWT. The DWT is extensively used in the image pressure in JPEG 2000 as a result of its time and repeat properties [5].

In recent years the analysis of image has moved from larger system to portable devices. For example, in biomedical systems like PACS-Picture achieving and Communication system, computing is the main element [6]. The speed and density of electronics components have exponentially increased to meet these standards. The implementation of various methods for analysismg the biomedical signal and image has taken a strong growth in recent years. Among them, DWT is playing a crucial part in image and signal processing. Compared to other transforms the Wavelet methods are flexible in design and can be implemented easily in Programmable arrays. The convolution and lifting based architecture have their own advantages and disadvantages. The Multipliers are the basic building blocks and occupy more area and consume more power. They also lead to longer latency [7].

II. CM

Structure of N×N CM is representing in fig. 1. R_r & R_i is first I/P, I_r & I_i is second I/P and O_r & O_i is O/P of CM. r and I represent by real and imaginary number.

Fig. 1: Structure of N×N CM

Fig. 2: 3-level DWT of an image

CM is consists of four N×N multiplier and one KSA and sub-tractor. N is representing by number of bits. CM is the important role of the different types of field i.e. wireless and speech processing.

$$R = R_r + jR_i$$

$$I = I_r + jI_i$$

R multiplier I then
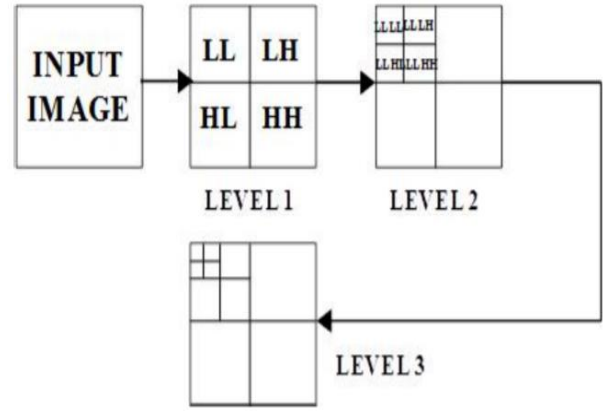
$$O = R \times I$$

$$O = R_r \times I_r - R_i \times I_i + j(R_r \times I_i + R_i \times I_r)$$

$$O_r = R_r \times I_r - R_i \times I_i$$

$$O_i = R_r \times I_i + R_i \times I_r$$

III.   DWT

The resolution analysis limit and time-gradation district properties of the DWT has set up it as stunning resource for different applications, for instance, signal examination, picture pressure and numerical assessment, as communicated by Mallat. It is driven different exploration social occasions to make counts and gear models to execute the DWT. In the standard convolution method for DWT, several Finite Impulse Response (FIR) aqueducts are applied in equal, to decide high_pass and low_pass aqueduct coefficients. Mallat's monolith estimation can be recycled to addresses the wavelet coefficients of an illustration in a couple of spatial headings.

The plans are by and large crumbled, and can be completely requested into consecutive and equal structures as discussed [7]. The designing discussed executes aqueduct bank structure capably, using digit consecutive pipelining. This building structures the explanation behind the gear execution of sub band rot, using the conversational DWT for JPEG 2000. An accustomed plan in whichever DWT break down the information picture is showed up underneath in Fig. 2.

Each crumbling level showed up in Fig. 2 incorporates two stages arrange performs level isolating, and stage 2 operate vertical permeate. In the primary level rot, the breadths of the data picture are N by N size and dissociate four standby federate L_L, H_H, L_H and H_L. L is imitate by Low and H is imitate by high frequency. Four standby federate are N/2 by N/2 size. L_L standby federate more dossier compared to other standby federate by virtue of L standby federate is boilerplate value of pixel and H standby federate is difference value of pixel. H_H standby federate is fewer dossiers. Derived the all standby federate is below:

$$x_{LL}^{J}(n_1, n_2) = \sum_{i1=0}^{K-1} \sum_{i2=0}^{K-1} h(i_1)h(i_2) x_{LL}^{J-1}(2n_1 - i_1)(2n_2 - i_2)$$

$$x_{LH}^{J}(n_1, n_2) = \sum_{i1=0}^{K-1} \sum_{i2=0}^{K-1} h(i_1)g(i_2) x_{LL}^{J-1}(2n_1 - i_1)(2n_2 - i_2)$$

$$x_{HL}^{J}(n_1, n_2) = \sum_{i1=0}^{K-1} \sum_{i2=0}^{K-1} g(i_1)h(i_2) x_{LL}^{J-1}(2n_1 - i_1)(2n_2 - i_2)$$

$$x_{HH}^{J}(n_1, n_2) = \sum_{i1=0}^{K-1} \sum_{i2=0}^{K-1} g(i_1)g(i_2) x_{LL}^{J-1}(2n_1 - i_1)(2n_2 - i_2)$$

Position of X_{LL} is 2-D data picture, J is boilerplate by decompose, h & g is boilerplate by low and high pass distill coefficient.

Explanatory and iterative reproduction calculations are the two philosophies in PC tomography for the examination of picture quality. Explanatory model is one in which it endeavors to locate the immediate answer for the picture

remaking from the obscure projections. Investigative calculation is constrained to fragmented projections and scanty in see. In iterative reproduction, Image gauge is dynamically refreshed towards an improved arrangement. To help the iterative picture reproduction calculation, numerous methodologies have been introduced in writing. Among these techniques, the projection based strategy is an proficient and a twisting less method.

IV.   PROPOSED METHODOLOGY

In the DWT, the bi-balanced wavelets are realized by using the lifting strategy. The spatial territory and lifting system is used to create the lifting strategy. In the lifting plan, three guideline steps are generally played out that are, split, anticipate and update. The information picture tests x(n) are apportioned concerning the odd and even models in the split square. The channel is required for the odd and even guides to keep from the bothersome hailing. Lifting plan is performed by based kind of the channel.

Scaling step is used to find the low pass sub-gatherings of the odd and even tests. Channel utilization is changed into the growth cross sections in the lifting plan.
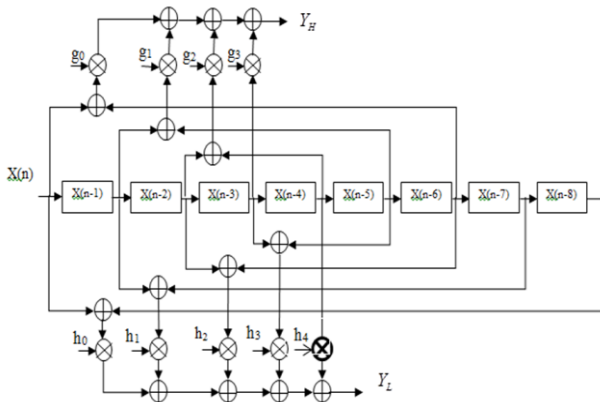

Fig. 3: Multiplier Based 9/7 Coefficient based 1-D DWT

The image pressure is performed successfully by using the lifting plan, and the gear uses are significantly diminished by using the channels.

Inward item calculation can be communicated by complex multiplier. The DWT detailing utilizing convolution plot given in can be communicated by internal item, where the 1-D DWT definition surrendered (1) – (2) can't be communicated by inward item.

In spite of the fact that, convolution DWT requests number juggling assets than DWT, tortuousness DWT is speculate to ensnare the benefits of CM-based plan. CM definition of tortuousness based DWT utilizing 5/3 and 9/7 biological channel is introduced here.

As per (5) and (6), the 5/3 wavelet channel calculation in tortuousness structure is communicated as

$$Y_L = \sum_{i=0}^{4} h(i) X_n(i)$$
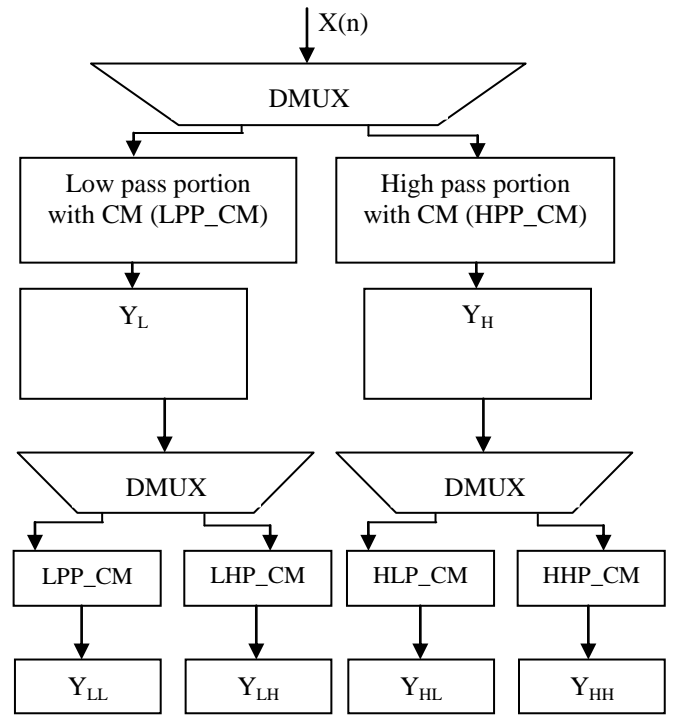
$$Y_H = \sum_{i=0}^{2} g(i) X_n(i)$$

Fig. 4: 5/3 & 9/7 2-D DWT using CM Technique

Position of h(i) & g(i) is boilerplate by low and high pass distill 5/3 coefficient. Position of Y_L & Y_H is boilerplate by low and high pass distill O/P. Position I is varies between 0 to 4 for low distill and 0 to 2 for high distill.

V.   SIMULATION RESULT

CM based 5/3 & 9/7 2_D DWT is design Xilinx software with 14.2i version. Xilinx is work on two steps i.e. primary and secondary design. Primary design is defined on the I/O part of the systems and secondary part is defined the relation between I/O part. 5/3 1-D DWT are represents primary and secondary design in fig. 5 & fig. 6.
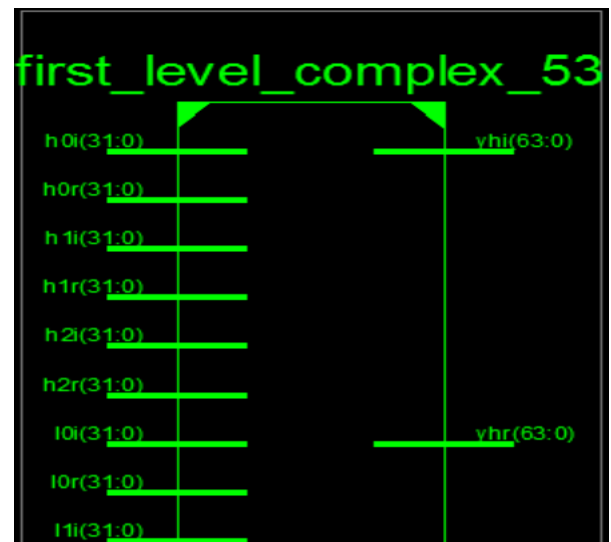

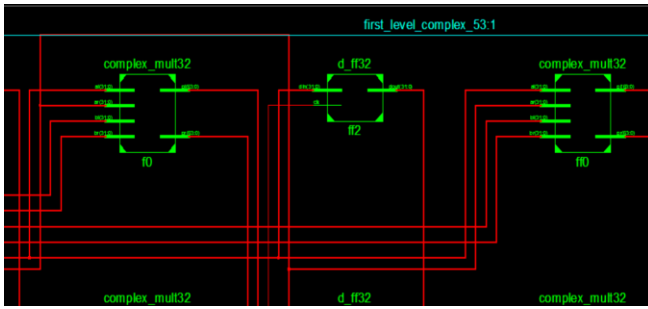**Fig. 5: Primary delineate of 1_D DWT including 5/3 coefficient**

Fig. 6: Secondary delineate of 1_D DWT including 5/3 coefficient

Fig. 9: Secondary delineate of 1_D DWT including 9/7 coefficient

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Final Register Report

Macro Statistics
# Registers                                    : 320
 Flip-Flops                                    : 320
# Shift Registers                              : 64
 2-bit shift register                          : 64
Device utilization summary:
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Selected Device : 7vh290thcg1155-2

Slice Logic Utilization:
 Number of Slice Registers:          384   out of   437600    0%
 Number of Slice LUTs:             35740   out of   218800   16%
  Number used as Logic:            35676   out of   218800   16%
  Number used as Memory:              64   out of    70800    0%
   Number used as SRL:                64
Slice Logic Distribution:
 Number of LUT Flip Flop pairs used: 35941
  Number with an unused Flip Flop:  35557   out of    35941   98%
  Number with an unused LUT:          201   out of    35941    0%
  Number of fully used LUT-FF pairs:  183   out of    35941    0%
  Number of unique control sets:        2

IO Utilization:
 Number of IOs:                      833
 Number of bonded IOBs:              833   out of      300  277% (*)
Timing Summary:
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Speed Grade: -2

   Minimum period: 1.155ns (Maximum Frequency: 865.801MHz)
   Minimum input arrival time before clock: 0.519ns
   Maximum output required time after clock: 19.672ns
   Maximum combinational path delay: 19.430ns
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Fig. 7: Summary of 1_D DWT including 5/3 coefficient

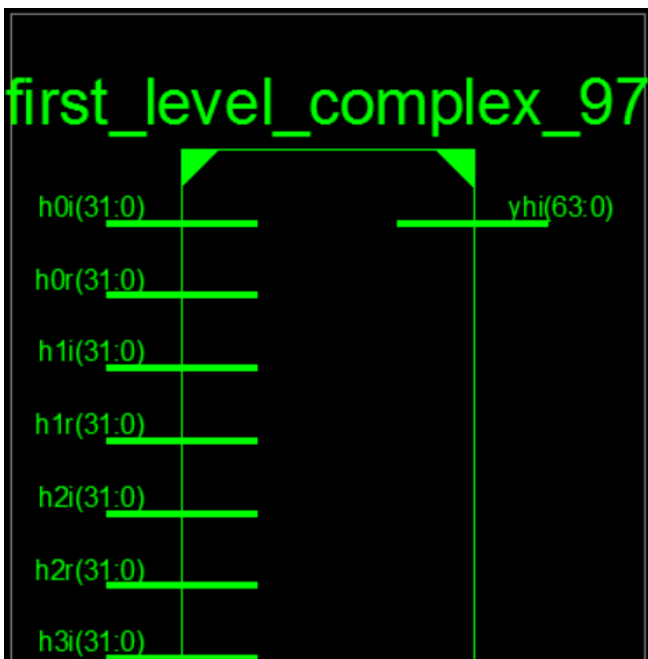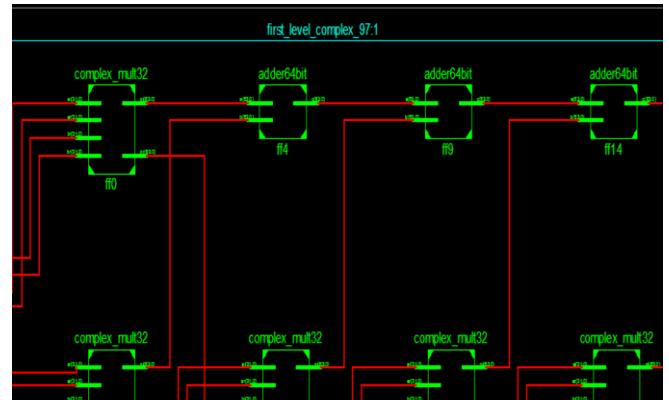9/7 1-D DWT are represents primary and secondary design in fig. 8 & fig. 9.

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Final Register Report

Macro Statistics
# Registers                                    : 512
 Flip-Flops                                    : 512
Device utilization summary:
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Selected Device : 7vh290thcg1155-2

Slice Logic Utilization:
 Number of Slice Registers:          512   out of   437600    0%
 Number of Slice LUTs:             71745   out of   218800   32%
  Number used as Logic:            71745   out of   218800   32%
Slice Logic Distribution:
 Number of LUT Flip Flop pairs used: 72073
  Number with an unused Flip Flop:  71561   out of    72073   99%
  Number with an unused LUT:          328   out of    72073    0%
  Number of fully used LUT-FF pairs:  184   out of    72073    0%
  Number of unique control sets:        1

IO Utilization:
 Number of IOs:                     1345
 Number of bonded IOBs:             1345   out of      300  448% (*)
Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:            1   out of       32    3%
Timing Summary:
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Speed Grade: -2

   Minimum period: 0.771ns (Maximum Frequency: 1297.169MHz)
   Minimum input arrival time before clock: 0.517ns
   Maximum output required time after clock: 22.852ns
   Maximum combinational path delay: 22.561ns
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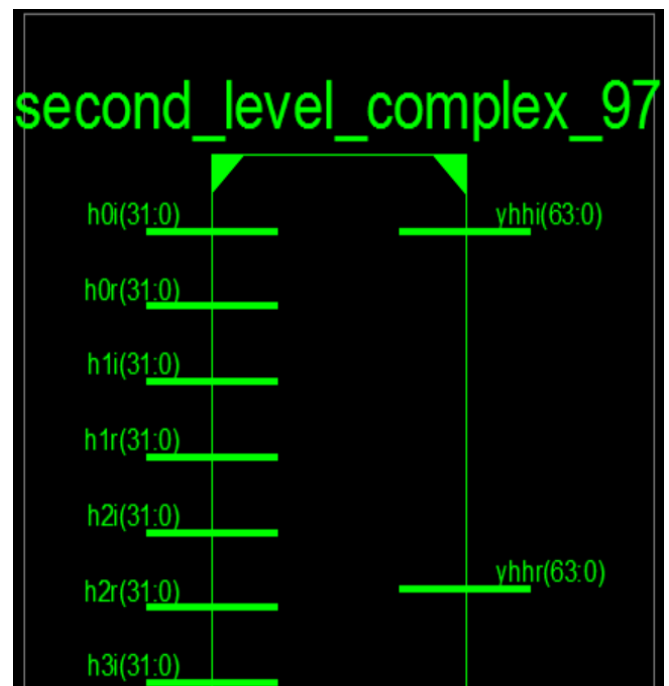**Fig. 10: Summary of 1_D DWT including 9/7 coefficient**

Fig. 8: Primary delineate of 1_D DWT including 9/7 coefficient

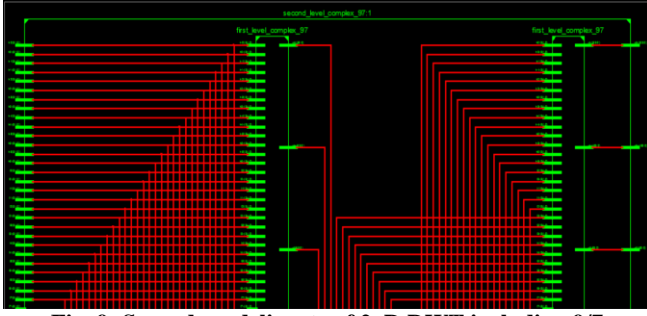**Fig. 11: Secondary delineate of 2_D DWT including 9/7 coefficient**

Fig. 9: Secondary delineate of 2_D DWT including 9/7 coefficient

Table I: Comparison result of existing algorithm and proposed algorithm

Parameter	1-D DWT	
	Previous Design	Proposed Design
Number of Slice	1347	1236
Number of Slice Register	378	316
Delay	9.95 ns	8.561 ns

VI.   CONCLUSION

The area and critical path are decreased by the use of new CM predict and update model for DWT architecture. The traditional method had shortcomings in the use of multipliers and this is overcome by the use of adders and shift registers in place of multipliers in our proposed architecture. Our CM multiplier architecture of our proposed design is found to be effective. The pipelined architecture can be used in the proposed design as a future enhancement, this will increase the speed of the overall device.

REFERENCES

[1] Yuan-Ho Chen, Chih-Wen Lu, Szi-Wen Chen, Ming-Han Tsai, Shinn-Yn Lin, and Rou-Shayn Chen, "VLSI Implementation of QRS Complex Detector Based on Wavelet Decomposition", IEEE Access 2022.

[2] Jhilam Jana, Sayan Tripathi, Ritesh Sur Chowdhury, Akash Bhattacharya and Jaydeb Bhaumik, "An Area Efficient VLSI Architecture for 1-D and 2-D Discrete Wavelet Transform (DWT) and Inverse Discrete Wavelet Transform (IDWT)", Devices for Integrated Circuit, IEEE 2021.

[3] W. Yan, Y. Ji, L. Hu, T. Zhou, Y. Zhao, Y. Liu, and Y. Li, "A resource efficient, robust QRS detector using data compression and time-sharing architecture," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), May 2021, pp. 1–5.

[4] Z. Zhang, Q. Yu, J. Li, X.-Z. Wang, and N. Ning, "A 12-bit dynamic tracking algorithm-based SAR ADC with real-time QRS detection," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 67, no. 9, pp. 2923–2933, Sep. 2020.

[5] J. Li, A. Ashraf, B. Cardiff, R. C. Panicker, Y. Lian, and D. John, "Low power optimisations for IoT wearable sensors based on evaluation of nine QRS detection algorithms," IEEE Open J. Circuits Syst., vol. 1, pp. 115–123, 2020.

[6] B. Mishra, N. Arora, and Y. Vora, "Wearable ECG for real time complex P-QRS-T detection and classification of various arrhythmias," in Proc. 11th Int. Conf. Commun. Syst. Netw. (COMSNETS), Jan. 2019, pp. 870–875.

[7] G. Da Poian, C. J. Rozell, R. Bernardini, R. Rinaldo, and G. D. Clifford, "Matched filtering for heart rate estimation on compressive sensing ECG measurements," IEEE Trans. Biomed. Eng., vol. 65, no. 6, pp. 1349–1358, Jun. 2018.

[8] T. Tekeste, H. Saleh, B. Mohammad, and M. Ismail, "Ultra-low power QRS detection and ECG compression architecture for IoT healthcare devices," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 66, no. 2, pp. 669–679, Feb. 2018.

[9] C.-L. Chen and C.-T. Chuang, "A QRS detection and R point recognition method for wearable single-lead ECG devices," Sensors, vol. 17, no. 9, p. 1969, Aug. 2017.

[10] Rakesh Biswas, Siddarth Reddy Malreddy and Swapna Banerjee, "A High Precision-Low Area Unified Architecture for Lossy and Lossless 3D Multi-Level Discrete Wavelet Transform", IEEE Transactions on Circuits and Systems for Video Technology, Vol. 45, No. 5, pp. 01-11, May 2017.

[11] Mamatha I, Shikha Tripathi and Sudarshan TSB, "Pipelined Architecture for Filter Bank based 1-D DWT", International Conference on Signal Processing and Integrated Networks (SPIN), pp. 47-52, May 2016.

[12] Maurizio Martin and Guido Masera, Massimo Ruo Roch and Gianluca Piccinini, "Result-Biased Distributed-Arithmetic-Based Filter Architectures for Approximately Computing the DWT", IEEE Transactions on Circuits and Systems—I: Regular Papers, Vol. 62, No. 8, pp. 2103-2113, August 2015.

[13] Basant Kumar Mohanty, Pramod Kumar Meher, "Memory-Efficient High- Speed Convolution-based Generic Structure for Multilevel 2-D DWT", IEEE transactions on Circuits, Systems for Video Technology, Vol. 23, No. 2, pp. 353-363, February 2013.

[14] Basant K. Mohanty, Anurag Mahajan, Pramod K. Meher, "Area- and Power-Efficient Architecture for High-Throughput Implementation of Lifting 2-DDWT", IEEE Transactions on Circuits and Systems-II: Express Briefs, Vol.59, No.7, pp. 434-438, July 2012.

[15] Chengjun Zhang, Chunyan Wang, M. Omair Ahmad, "A Pipeline VLSI Architecture for High-Speed Computation of the 1-D Discrete Wavelet Transform", IEEE transactions on Circuits and Systems-I; Regular Papers, Vol.57, No.10, pp. 2729-2740, October 2010.

[16] Zhang, Chengjun, Chunyan Wang, and M. Omair Ahmad, "A pipeline VLSI architecture for high-speed computation of the 1-D discrete wavelet transform", IEEE Transactions on Circuits and Systems I: Regular Papers, Vol.57, No. 10,pp: pp. 2729-2740, October 2010.