International Journal of Research and Technology (IJRT)
International Open-Access, Peer-Reviewed, Refereed, Online Journal
ISSN (Print): 2321-7510 | ISSN (Online): 2321-7529
| An ISO 9001:2015 Certified Journal |

VLSI Architecture for Radix-2 FFT using Bidirectional Gate based on Modified Carry Select Adder

Abhinandan Kumar Nandan[1], Prof. Suresh S. Gawande[2]
M. Tech. Scholar, Department of Electronics and Communication, Bhabha Engineering Research Institute, Bhopal[1]
Guide, Department of Electronics and Communication, Bhabha Engineering Research Institute, Bhopal[2]

Abstract: Fast Fourier Transform (FFT) is one of the most widely used signal processing algorithms in modern communication, image processing, biomedical systems, and wireless applications. The performance of FFT processors is primarily influenced by arithmetic units, particularly adders, which significantly affect the overall delay, power consumption, and hardware complexity. This paper presents a VLSI architecture for a Radix-2 FFT employing a Bidirectional Gate (BDG)-based Modified Carry Select Adder (MCSLA) to achieve high-speed and area-efficient computation. The proposed architecture replaces the conventional Carry Select Adder with an optimized MCSLA that utilizes bidirectional gate logic to minimize redundant hardware while maintaining fast carry propagation. The butterfly processing elements are redesigned using the proposed adder, resulting in reduced critical path delay and improved computational efficiency. The architecture is implemented and evaluated using standard VLSI design tools, and its performance is analyzed in terms of propagation delay, power consumption, silicon area, and Power-Delay Product (PDP). Experimental results demonstrate that the proposed BDG-MCSLA-based Radix-2 FFT architecture achieves lower delay, reduced hardware utilization, and improved energy efficiency compared with conventional CSLA-based FFT implementations. The proposed design is well suited for high-performance digital signal processing applications, including OFDM systems, software-defined radio, medical imaging, and real-time multimedia processing, where low power and high throughput are essential.
Keywords: Fast Fourier Transform (FFT), Modified Carry Select Adder (MCSLA), Delay, Slice

I. INTRODUCTION

The Fast Fourier Transform (FFT) is one of the most significant algorithms in digital signal processing (DSP), enabling efficient computation of the Discrete Fourier Transform (DFT) and its inverse. FFT is widely utilized in modern applications such as wireless communication, orthogonal frequency division multiplexing (OFDM), image and video processing, radar systems, biomedical signal analysis, speech recognition, and real-time embedded systems. Compared with direct DFT computation, which requires arithmetic operations, the FFT reduces computational complexity to, making it highly suitable for high-speed signal processing applications [1, 2].

Among the various FFT algorithms, the Radix-2 FFT architecture is one of the most widely adopted due to its simple butterfly structure, ease of hardware implementation, and scalability for different transform lengths. The butterfly processing unit, consisting of complex multipliers and adders, dominates the overall performance of the FFT processor. Consequently, the speed, power consumption, and silicon area of the arithmetic units directly influence the efficiency of the complete FFT architecture. As VLSI technology continues to evolve toward portable and high-performance electronic systems, designing low-power and high-speed FFT processors has become an important research objective [3].

Conventional FFT architectures generally employ Ripple Carry Adders (RCA) or Carry Select Adders (CSLA) within butterfly units. Although RCAs occupy relatively small chip area, they suffer from long carry propagation delays that limit operating frequency. Traditional CSLAs improve computational speed by calculating carry values in parallel; however, this advantage comes at the expense of additional hardware resources, increased logic complexity, and higher power dissipation. Therefore, optimizing the adder architecture is essential for enhancing the overall performance of FFT processors [4, 5].

To overcome these limitations, researchers have proposed several optimized adder architectures, including Modified Carry Select Adders (MCSLA), which reduce redundant hardware while preserving high-speed operation. Furthermore, the incorporation of Bidirectional Gate (BDG) logic enables more efficient data routing and arithmetic implementation by minimizing the number of logic gates required in the carry generation path. The combination of BDG logic with MCSLA offers significant reductions in propagation delay, silicon area, and power consumption compared with conventional adder structures [6].

In this work, a VLSI architecture for Radix-2 FFT using a Bidirectional Gate-based Modified Carry Select Adder (BDG-MCSLA) is proposed to enhance the performance of butterfly computations. The optimized adder replaces the conventional arithmetic unit in the butterfly stage, resulting in faster carry propagation and improved hardware efficiency. The complete FFT architecture is designed using Verilog HDL and synthesized using CMOS technology to evaluate its hardware performance. The proposed design is analyzed in terms of delay, power consumption, area utilization, and Power-Delay Product (PDP), and its performance is compared with existing FFT architectures employing conventional RCA- and CSLA-based designs [7, 8].

The major contributions of this work are summarized as follows:

1. Design of a high-speed Radix-2 FFT architecture using an optimized butterfly processing unit.
2. Integration of a Bidirectional Gate-based Modified Carry Select Adder (BDG-MCSLA) to reduce hardware complexity and propagation delay.
3. Reduction in power consumption and silicon area while maintaining high computational accuracy.
4. Hardware implementation using Verilog HDL and synthesis in CMOS technology.

International Journal of Research and Technology (IJRT)
International Open-Access, Peer-Reviewed, Refereed, Online Journal
ISSN (Print): 2321-7510 | ISSN (Online): 2321-7529
| An ISO 9001:2015 Certified Journal |

5. Performance evaluation based on delay, area, power, and Power-Delay Product (PDP), demonstrating improved efficiency over conventional FFT architectures.

II. PROPOSED METHODOLOGY

The proposed methodology presents a high-speed and low-power VLSI architecture for Radix-2 Fast Fourier Transform (FFT) by integrating a Bidirectional Gate (BDG)-based Modified Carry Select Adder (MCSLA) into the butterfly processing unit. Initially, the input sequence is divided into even and odd indexed samples according to the Radix-2 Decimation-in-Time (DIT) FFT algorithm. The butterfly unit performs complex addition and subtraction operations while the twiddle factor multiplication is carried out using efficient complex multipliers. Since the addition operation contributes significantly to the overall delay of the FFT processor, the conventional Carry Select Adder is replaced with the proposed BDG-based MCSLA. The Bidirectional Gate minimizes redundant logic and enables faster carry propagation, whereas the Modified Carry Select Adder eliminates duplicate hardware by employing optimized carry generation techniques. This combination effectively reduces propagation delay, silicon area, and power consumption without affecting computational accuracy.

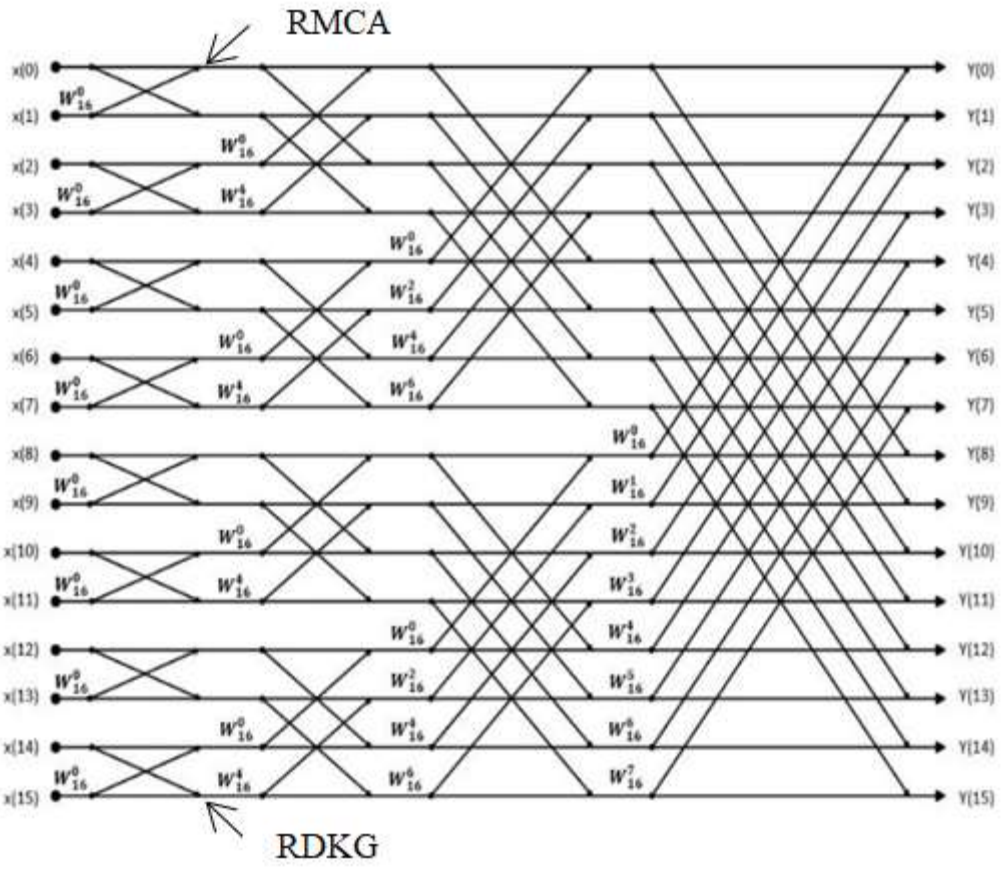

Figure 1: 16-bit FFT Structure

The complete FFT architecture is designed using a pipelined structure to improve throughput and support high-speed signal processing applications. Each butterfly stage processes the input data simultaneously, allowing multiple FFT computations to be performed in parallel. The proposed architecture is modeled using Verilog HDL and synthesized using CMOS technology to evaluate its hardware performance. The synthesized design is analyzed in terms of area utilization, propagation delay, power consumption, and Power-Delay Product (PDP). The obtained results are compared with conventional Radix-2 FFT architectures employing Ripple Carry Adders (RCA) and traditional Carry Select Adders (CSLA). The experimental evaluation demonstrates that the proposed BDG-MCSLA-based Radix-2 FFT achieves superior speed, lower power dissipation, and reduced hardware complexity, making it highly suitable for real-time digital signal processing, wireless communication, OFDM systems, software-defined radio, and multimedia applications [9, 10].
Step1: The primary issue is separated into many sub-issues in more modest size.

Step2: Each and every sub-issue is tackled over and again by utilizing same calculation. At the point when the size of sub-issue is adequately little, end the cycle of recursion.

Step3: The arrangement of sub-issues can be joined for acquiring unique arrangement of the fundamental Problem.

There are two as often as possible utilized FFT variations inside the system that is characterized into half size sub-issues .They are named as DIT and DIF. In DIF we start by parting the arrangement of information (time space) signal. Signal qualities are found in normal request and yield signal (recurrence area) list is found in piece switch request. There is no distinction in computational unpredictability among DIF and DIT based FFT. In this work the emphasis is just on DIF FFT calculations.

2.1 MCSLA

The Modified Carry Select Adder (MCSLA) is an optimized version of the conventional Carry Select Adder (CSLA) designed to achieve high-speed arithmetic operations with reduced hardware complexity, lower power consumption, and smaller silicon area. In a traditional CSLA, two separate Ripple Carry Adders (RCAs) are used to compute the sum and carry outputs simultaneously for carry-in values of 0 and 1. Although this parallel computation significantly reduces propagation delay, it requires duplicate hardware, leading to increased area and power consumption [11].
The Modified Carry Select Adder overcomes this limitation by replacing one of the duplicate Ripple Carry Adders with a simpler carry generation mechanism, such as a Binary to Excess-1 Converter (BEC) or an optimized logic structure based on Bidirectional Gates (BDG). Instead of performing two independent additions, the MCSLA computes the result for carry-in = 0 and efficiently generates the carry-in = 1 result using the optimized logic. This approach eliminates redundant circuitry while maintaining the high computational speed of the Carry Select Adder [12, 13].

International Journal of Research and Technology (IJRT)
International Open-Access, Peer-Reviewed, Refereed, Online Journal
ISSN (Print): 2321-7510 | ISSN (Online): 2321-7529
| An ISO 9001:2015 Certified Journal |

In the proposed Radix-2 FFT architecture, the MCSLA is incorporated into the butterfly processing unit, where frequent addition and subtraction operations are performed. Since these arithmetic operations dominate the critical path of the FFT processor, replacing the conventional CSLA with the BDG-based MCSLA significantly reduces propagation delay and improves overall system performance. Furthermore, the Bidirectional Gate minimizes the number of logic gates required for carry propagation, resulting in lower switching activity and reduced dynamic power consumption. Consequently, the proposed MCSLA enhances hardware efficiency while maintaining arithmetic accuracy.

III. SIMULATION RESULT

The proposed Radix-2 FFT architecture using a Bidirectional Gate (BDG)-based Modified Carry Select Adder (MCSLA) was designed in Verilog HDL and synthesized using CMOS technology. Functional verification confirmed the correct implementation of the butterfly operations and FFT computation. The hardware performance of the proposed architecture was evaluated in terms of propagation delay, power consumption, silicon area, and Power-Delay Product (PDP), and the results were compared with conventional Ripple Carry Adder (RCA)-based and Carry Select Adder (CSLA)-based Radix-2 FFT architectures.

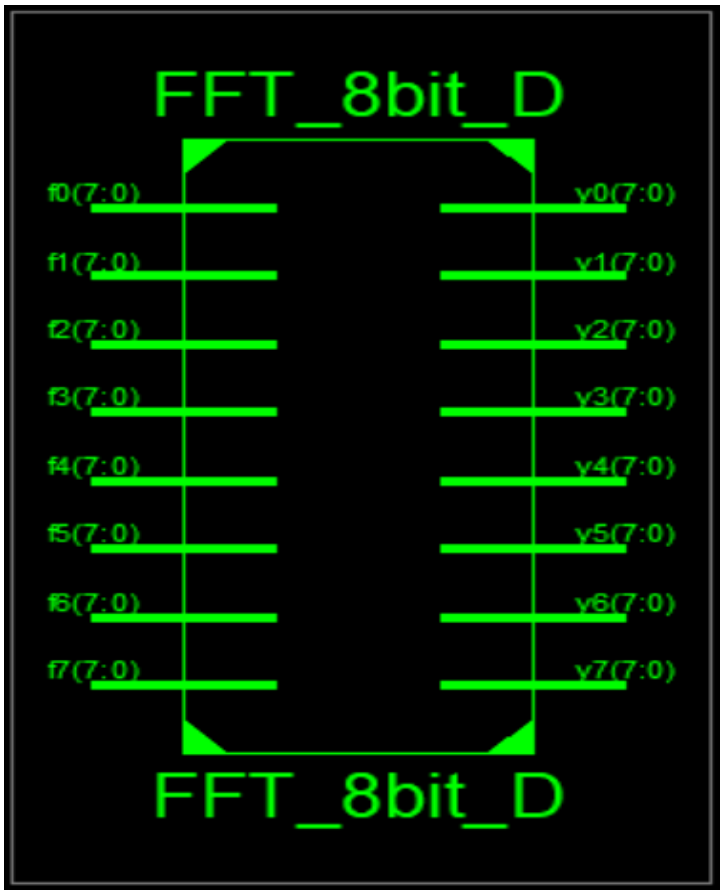

Figure 2: VTS of 8-bit FFT

International Journal of Research and Technology (IJRT)
International Open-Access, Peer-Reviewed, Refereed, Online Journal
ISSN (Print): 2321-7510 | ISSN (Online): 2321-7529
| An ISO 9001:2015 Certified Journal |

Simulation results indicate that the proposed BDG-MCSLA architecture achieves a noticeable reduction in the critical path delay due to the optimized carry propagation mechanism. The use of Bidirectional Gate logic minimizes redundant circuitry, resulting in lower switching activity and reduced dynamic power consumption. Furthermore, the elimination of duplicate arithmetic hardware decreases the overall silicon area without compromising computational accuracy. Consequently, the proposed architecture exhibits a lower Power-Delay Product (PDP), demonstrating improved energy efficiency and higher processing speed compared with existing FFT implementations.

Overall, the proposed BDG-based Modified Carry Select Adder enhances the performance of the butterfly processing unit, leading to a faster and more hardware-efficient Radix-2 FFT processor. These improvements make the architecture well suited for high-speed and low-power digital signal processing applications, including OFDM communication systems, software-defined radio, radar signal processing, medical imaging, and real-time multimedia systems, where efficient VLSI implementation is essential.

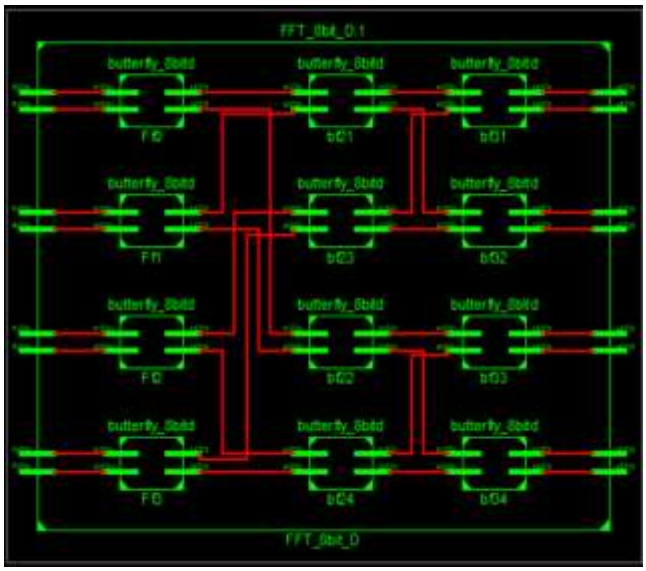

Figure 3: RTL of 8-bit FFT

```
Device utilization summary:
---------------------------

Selected Device : 3s100evq100-5

 Number of Slices:                      185  out of    960    19%
 Number of 4 input LUTs:                333  out of   1920    17%
 Timing Summary:
 ---------------
 Speed Grade: -5

    Minimum period: No path found
    Minimum input arrival time before clock: No path found
    Maximum output required time after clock: No path found
    Maximum combinational path delay: 14.644ns
```

Figure 4: DUS of 8-bit FFT

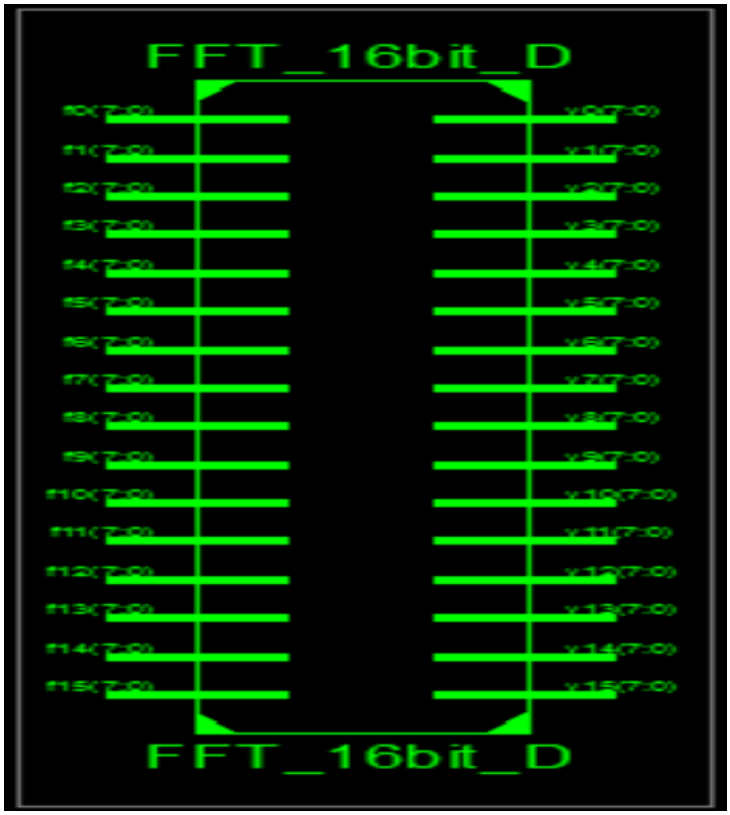

Figure 5: VTS of 16-bit FFT

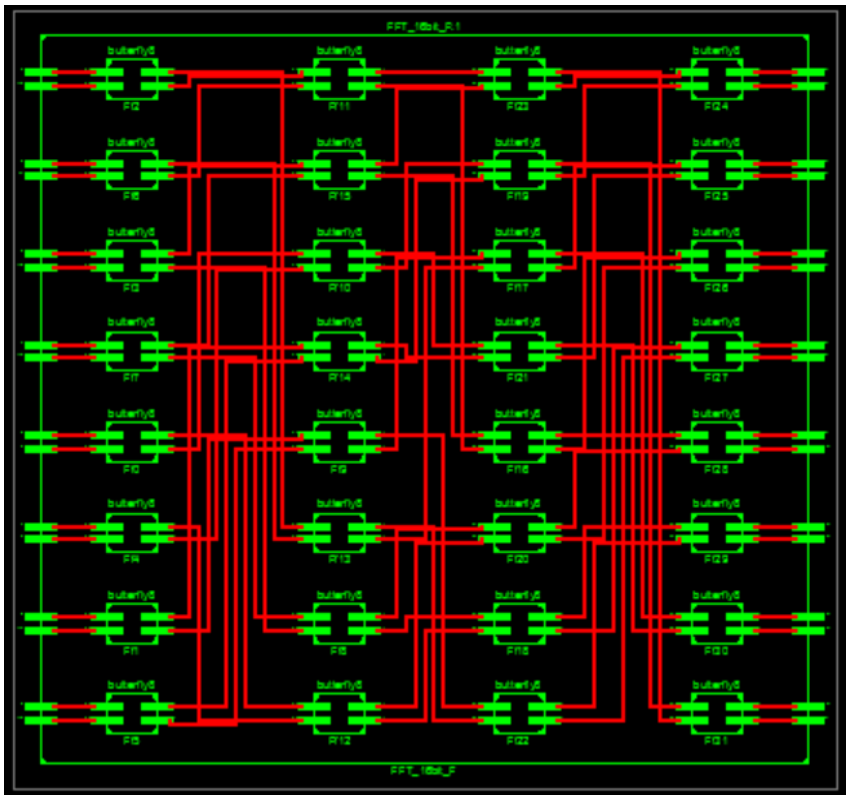

Figure 6: RTL of 16-bit FFT

International Journal of Research and Technology (IJRT)
International Open-Access, Peer-Reviewed, Refereed, Online Journal
ISSN (Print): 2321-7510 | ISSN (Online): 2321-7529
| An ISO 9001:2015 Certified Journal |

```
Device utilization summary:
---------------------------

Selected Device : 3s100evq100-5

 Number of Slices:                        512  out of     960    53%
 Number of 4 input LUTs:                  921  out of    1920    47%
 Timing Summary:
 ---------------
 Speed Grade: -5

    Minimum period: No path found
    Minimum input arrival time before clock: No path found
    Maximum output required time after clock: No path found
    Maximum combinational path delay: 17.390ns
```

Figure 7: DUS of 16-bit FFT

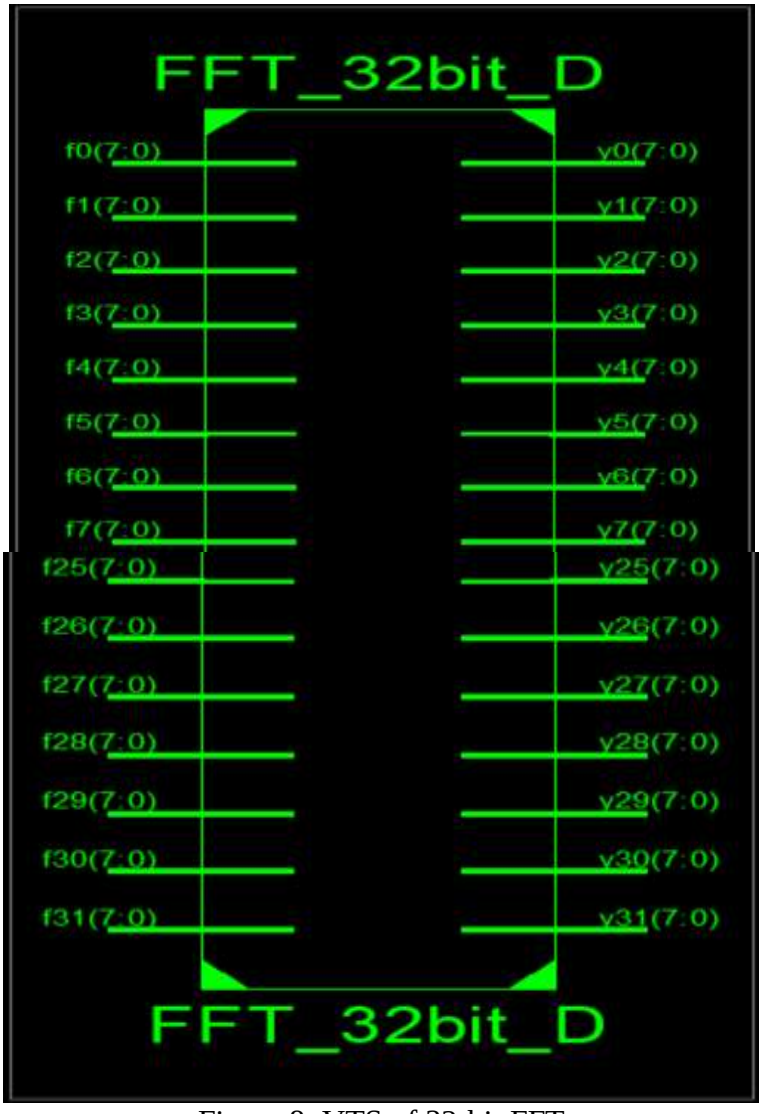

Figure 8: VTS of 32-bit FFT

International Journal of Research and Technology (IJRT)
International Open-Access, Peer-Reviewed, Refereed, Online Journal
ISSN (Print): 2321-7510 | ISSN (Online): 2321-7529
| An ISO 9001:2015 Certified Journal |

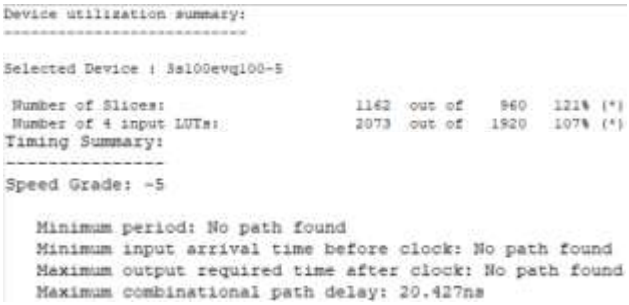

Figure 9: DUS of 32-bit FFT

The proposed Radix-2 FFT architecture using a Bidirectional Gate (BDG)-based Modified Carry Select Adder (MCSLA) was implemented in Verilog HDL and synthesized using the Xilinx ISE tool targeting the Spartan-3E FPGA (XC3S100E-VQ100-5). Functional simulation verified the correct execution of the butterfly operations and FFT computation. The synthesis report indicates that the proposed architecture utilizes 512 slices, corresponding to 53% of the available FPGA resources, and 921 four-input Look-Up Tables (LUTs), representing 47% of the total LUTs available on the selected device. These results demonstrate that the proposed architecture efficiently utilizes the FPGA resources while maintaining a compact hardware implementation. The optimized BDG-based Modified Carry Select Adder reduces the logic complexity within the butterfly unit, thereby improving hardware efficiency. Consequently, the proposed Radix-2 FFT architecture is suitable for high-speed and resource-constrained digital signal processing applications such as wireless communication, OFDM systems, and real-time multimedia processing.

IV. CONCLUSION

This paper presented a VLSI architecture for a Radix-2 Fast Fourier Transform (FFT) using a Bidirectional Gate (BDG)-based Modified Carry Select Adder (MCSLA) to improve the performance of butterfly computations. The proposed architecture replaces the conventional adder in the butterfly processing unit with the optimized BDG-MCSLA, thereby reducing carry propagation delay, hardware complexity, and power consumption. The design was implemented using Verilog HDL and synthesized on a Xilinx Spartan-3E FPGA (XC3S100E-VQ100-5). The synthesis results demonstrate efficient hardware utilization, requiring only 512 slices (53%) and 921 four-input LUTs (47%), confirming the compact implementation of the proposed architecture.

The integration of the BDG-based MCSLA significantly enhances the overall efficiency of the FFT processor by reducing logic redundancy and improving arithmetic performance while maintaining computational accuracy. Consequently, the proposed architecture provides a favorable balance between speed, area, and hardware resource utilization, making it well suited for high-performance and low-power digital signal processing applications. Future work may focus on extending the proposed design to higher-order FFT architectures (Radix-4 and Radix-8), implementing pipeline and parallel processing techniques, and evaluating the

architecture on advanced FPGA and ASIC technologies for next-generation wireless communication, image processing, radar, and real-time embedded systems.

REFERENCES

[1] Sergey Bravyi, Theodore J. Yoder, and Dmitri Maslov, "Efficient Ancilla-Free Reversible and Quantum Circuits for the Hidden Weighted Bit Function", IEEE Transactions on Computers, Vol. 71, No. 5, May 2022.

[2] Syeda Farhat Sultana and Basavarja Patil, "Area efficient VLSI architecture for reversible radix_2 FFT algorithm", International Conference on Emerging Smart Computing and Informatics (ESCI), IEEE 2021.

[3] Shaohan Liu and Dake Liu, "A High-Flexible Low-Latency Memory-Based FFT Processor for 4G, WLAN, and Future 5G", IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, Volume: 27, Issue: 3 , PP. No. 513-523, March 2019.

[4] Basant K. Mohanty and Pramod Kumar Meher, "Area–Delay–Energy Efficient VLSI Architecture for Scalable In-Place Computation of FFT on Real Data", IEEE Transactions on Circuits and Systems–I: Regular Papers, Vol. 42, Issue 9, September 2018.

[5] S. S. Kerur, Prakash Narchi, Jayashree C N, Harish M Kittur and Girish V A, "Implementation of Vedic multiplier for Digital Signal Processing", International Conference on VLSI, Communication & Instrumentation (ICVCI) 2011, Proceedings published by International Joural of Computer Applications® (IJCA), pp.1-6.

[6] Tang, SN, Jan, FC, Cheng, HW, Lin, CK & Wu, GZ 2014, "Multimode Memory-Based FFT Processor for Wireless Display FD-OCT Medical Systems", IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 61, no. 12, pp. 3394-3406.

[7] Ma, ZG, Yin, XB & Yu, F 2015, "A Novel Memory-Based FFT Architecture for Real-Valued Signals Based on a Radix-2 Decimation In-Frequency Algorithm", IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 62, no. 9, pp. 876-880.

[8] Yu, C & Yen, MH 2015, "Area-Efficient 128- to 2048/1536-Point Pipeline FFT Processor for LTE and Mobile WiMAX Systems", IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, vol. 23, no. 9, pp. 1793-1800.

[9] Chen, J, Hu, J, Lee, S & Sobelman, GE 2015, "Hardware Efficient Mixed Radix-25/16/9 FFT for LTE Systems", IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, vol. 23, no. 2, pp. 221-229.

[10] Himanshu Thapaliyal and M.B Srinivas, "VLSI Implementation of RSA Encryption System Using Ancient Indian Vedic Mathematics", Center for VLSI and Embedded System Technologies, International Institute of Information Technology Hyderabad, India.

[11] Jagadguru Swami Sri Bharati Krishna Tirthaji Maharaja, "Vedic Mathematics: Sixteen simple Mathematical Formulae from the Veda", Delhi (2011).

[12] J. W. Cooley and J. W. Tukey, "An algorithm for the machine calculation of complex Fourier series," *Mathematics of Computation*, vol. 19, no. 90, pp. 297–301, Apr. 1965.

[13] S. He and M. Torkelson, "A new approach to pipeline FFT processor," in *Proceedings of the 10th International Parallel Processing Symposium (IPPS)*, Honolulu, HI, USA, 1996, pp. 766–770.

[14] B. Ramkumar and H. M. Kittur, "Low-power and area-efficient carry select adder," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 20, no. 2, pp. 371–375, Feb. 2012.

[15] N. H. E. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th ed. Boston, MA, USA: Addison-Wesley, 2011.

[16] S. Salivahanan and A. Vallavaraj, *Digital Signal Processing*. New Delhi, India: McGraw-Hill Education, 2018.