Review on Development Process & characteristic analysis of SOI MOSFET devices

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Abstract— **As the device count in an IC is running into billions per chip, the issue of power dissipation in the chip is becoming too critical. Due to decreasing device dimension the performance of the bulk Si MOSFET is limited by its fundamental physical limits such as reduction in carrier mobility due to impurities, increasing gate tunnelling effect as the gate oxide thickness decreases and increasing p-n junction leakage current as the junction become more and more shallow. These requirements have led to development of alternating technology. SOI (silicon on insulator) technology is one such alternative which can offer the performance as may be expected from the next generation technology. SOI technology offers significant advantages in design, fabrication and performance for many semiconductor circuits such as excellent isolation, improved latch up free operation, radiation hardness, reduced short channel effects, improved switching speeds and reduced leakage current, due to reduction in the drain-body capacitance. The reduction in the parasitic capacitances leads to improved switching speed and superior performance.. This paper is focused on the brief of SOI MOSFET Technology, its characteristics, advantages and disadvantages of it.**

Keywords— ***SOI, MOSFET, CMOS, wafer, Silicon, Insulator***

I. INTRODUCTION

During 1960s the need for radiation hardness devices in the devices in the defence and space industries leads the innovation of SOI devices. Due to lackness of proper fabrication process use of expensive material made it unpopular in the primary stage. However it has the characteristic to be an alternating technology due to the drawback of traditional bulk technology; its use in the prior stage become impractical due to technological deficiency and its expensive fabrication cost. The performance of bulk Si MOSFET is limited by the fundamental physical limits such as reduction in carrier mobility due to impurity, as the gate oxide thickness decreases the gate tunneling effect increases and the junction become more and more shallow by increasing p-n junction leakage current. According to the Moore law which states that the performances of processors are doubled every 18 month. Increasing the number of device count means decreasing the space and hence increasing the switching speed of the device. Two most important criteria used for measuring the performance of a circuit is speed and area. However due to increased transistor density and the need of portable devices most important cost measure in VLSI design is power consumption. SOI technology utilizes the low power technique. Most of the early SOI devices were fabricated with SOS (Silicon On Sapphire) wafers. The unique feature of today's SOI wafer is that they have a buried silicon oxide or BOX layer extending across the entire wafer. Introducing a BOX structure in traditional MOS structure brings a lot of improved characteristic such as excellent isolation, reduced short channel effects, reduced leakage current, improved latch up free operation, radiation hardness, and improved switching speed due to reduction in the drain body capacitance. SOI CMOS technology is likely to be an alternative for deep sub-micron CMOS [2]. It appears to be the best option for low-power electronics.

This paper is organized as follow: historical perspective of the SOI devices & technology, have been discussed under section II, operation on SOI MOSFET has been discussed under section III. SOI characteristics and its challenges have been discussed under section IV & V. And finally the paper is concluded and the research area to improve the efficiency has been discussed.

II. HISTORICAL PERSPECTIVE OF SOI MOSFET

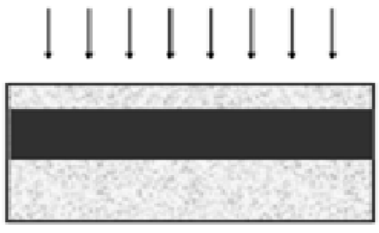
SOI technologies can be in general divided into two groups. In the first one, a thin insulating layer is used to separate the active semiconductor layer from the semiconductor substrate. These include zone melting recrystallization (ZMR), Separation by implantation of oxygen (SIMOX), full isolation by porous oxidized silicon (FIPOS), and wafer bonding (WB). In the second group, the semiconductor film is deposited directly onto an insulating substrate. This happens in Silicon On Sapphire (SOS) and Silicon on zirconia (SOZ).

A. *Separation by implantation of oxygen (SIMOX) :*

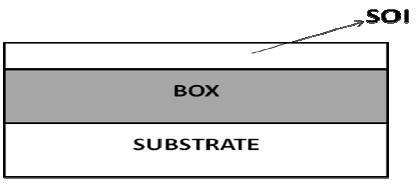
In 1966, Watanabe and Tooi [1] observed that if oxygen ions are implanted into silicon using a RF gas discharge then the resulting SiO2 has the characteristics identical to those of thermally grown SiO2. In 1978, it was discovered that if energy and dose of oxygen being implanted is kept 150 KeV and 12 x 10^{18} cm^2 and the sample is annealed at a temperature of 1150ºC, then the resulting buried oxide layer exhibits excellent electrical characteristics and the top Si layer is crystalline. This method is known as SIMOX process, illustrated in figure 1.1.

The silicon layer above the BOX is where the device is fabricated, and the silicon below the BOX, called the handle, is un-doped silicon that is only used for handling the wafer during the fabrication process, and does not affect device performance. The BOX, greatly affects the parameters of device, and lead to the development of new structure types.

(Oxygen implanted at: energy 120-200KeV DOSE~ 0.3-1.8e18 **Cm^2**)



Anneal in inert ambient above 1300ºC, 3-6 hours



- BOX thickness: 100, 200, 400 nm
- SOI film thickness varies from 50-240 nm

Fig :1.1 SIMOX process

The BOX gave rise to some new structure types not available through the bulk silicon technology. One of the more unusual is the double-gate device, or volume inversion MOSFETs (VI-MOSFET). These devices have a second gate located in the buried oxide layer, which may be grounded. By using second voltage this gate can be turned on and off. Another arrangement is stacked devices, which makes SOI devices in a 3-Dimensional structure. This can be used for parallel processing, and lead to faster processing times. The BOX helps insulate the devices from one another so they do not interfere with each other. A third type of device is the nano-SOI device which is too thin, which have a silicon thickness of less than 10nm [4]. This is possible due to the noise-reducing capabilities of the BOX.

During 1980s, the recrystallization of Si layer with laser or e-beam was studied extensively and also formed a part of Japanese R & D project aimed at developing 3D ICs. This project also included fabrication and evaluation of SOI substrates, design and simulation of SOI devices, and circuit design technology for 3Dimensional ICs [2]. In the same tenure, there was an important improvement in SIMOX technology. It was discovered that if the annealing temperature is raised to above 1300ºC , then the dislocation density is reduced from 10^9 cm-2 to 10^6 cm^2 [3].

During 90s, SIMOX process was further improved with the discovery of "dose window"[4] which resulted in drastic reduction in dislocation density and buried oxide thickness was increased by high temperature oxidation (ITOX technology) [2]. The resulting SIMOX technology led the throughput to increase by a factor of 5 and dislocation density as low as 10^2 cm^2 to 10^3 cm^2.

B. *Zone Melting Recrystallization (ZMR):*

ZMR [5] technology produces SOI structures by recrystallization of polysilicon films, deposited on oxidized silicon wafers. In the ZMR process, a thermal oxide (1-2 µm thick) is first grown on a bulk silicon substrate, followed by polycrystalline silicon film (0.5-1.0 µm thick) on the thermal oxide. The whole structure is capped with a 2 µm thick layer of deposited thermal oxide covered by a thin Si_3N_4 layer. A melting zone is scanned across the entire silicon wafer. Hence as a result, full liquid phase recrystallization of silicon wafer can be carried out in a single pass.

C. *Full Isolation by Porous Oxidation Of Silicon (FIPOS):*

FIPOS [6] involves the use of oxidized porous silicon. This technique is more complicated than the SIMOX and ZMR, but offers the potential for essentially defect-free active silicon layers. Hence this process is relatively clean. The Oxidation of the porous silicon layer leads to the standard thermal oxide and does not disturb the high quality of the original silicon film. The key aspect in FIPOS technique is the formation of porous silicon, which is controlled by the type and concentration of doping as well as by the current density and HF solution.

D. *Wafer Bonding (WB):*

The WB [7] technique provides undamaged crystal quality and more flexibility than SIMOX for both the Si film and the buried oxide layer. There are three basic steps required for the WB process: (1) mating two silicon wafers at room temperature, (2) annealing the bonded wafers at temperatures above 800ºC for several hours to increase bonding strength, and (3) thinning down the wafers to a proper thickness by grinding and polishing and/or etching.

One prominent example of a wafer bonding process is the Smart Cut method which was developed at CEA-LETI, one of the world's premier microelectronics research laboratories. Smart Cut is a revolutionary technique used to transfer ultra thin single crystal layers of wafer substrate material (such as silicon) onto another surface. Differing from traditional layer-transfer techniques uses a thermal activation process as an "atomic scalpel". It literally slices the wafer horizontally from the donor substrate by lifting off a thin layer and placing it onto a new substrate. Inherently, this process offers better control, and a single donor substrate can be reused many times for further layer transfers.

The transferred layer thickness is pre-determined by the cleavage zone created via ion implantation (of hydrogen, helium, argon, etc.). After the layer transfer and bonding, the cleaved surface of the thin film is treated, polished and annealed to ensure a silicon film (in the case of SOI) and surface quality comparable to silicon prime wafers. Smart Cut is Soitec's patented process technology for creating "engineered" wafers. Engineered wafers (such as Silicon-On-Insulator or SOI) consist of multiple layers of substrate materials.

The main drawback of the wafer bonding technique is its difficulty in producing very thin, uniform Si film through the conventional polishing technique. Therefore, the third step is becoming more and more important for manufacturing ultrathin Si films with good uniformity.

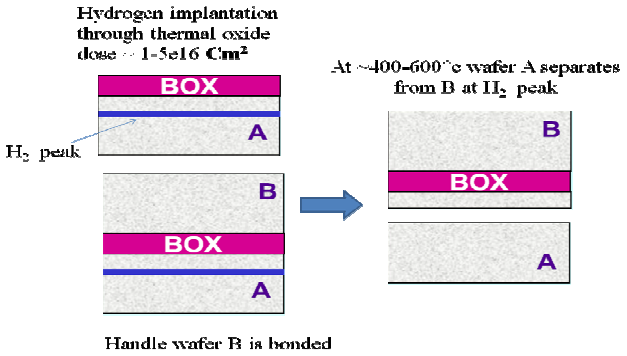


Fig: 1.2 smart cut processes

E. *Silicon On Zirconia (SOZ) & Silicon On Sapphire (SOS):*

The sapphire (alpha-Al203) crystals [8] are produced using either the flame-fusion growth technique, edge-defined film-fed growth or Czochralski growth. The first two of these techniques provide sapphire boules which have to be sliced before polishing and the third technique provides thin rectangular sapphire ribbons, which have to be cut into circular wafers later on. After chemical and mechanical polishing the sapphire wafers receive a final hydrogen etching at 1150ºC in an epitaxial reactor and a silicon film is deposited using pyrolysis of silane at a temperature between 900 and 1000ºC. Due to thermal mismatch and lattice, defect in density in films is quite high, especially in very thin films. The main defects present in the as grown SOS films are: aluminum auto doping from the Al_2o substrate and stacking faults. These all account for the low values of resistivity, mobility and lifetime near the interface.

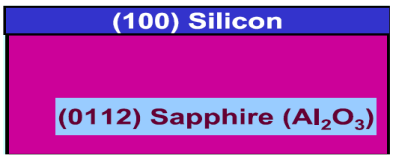
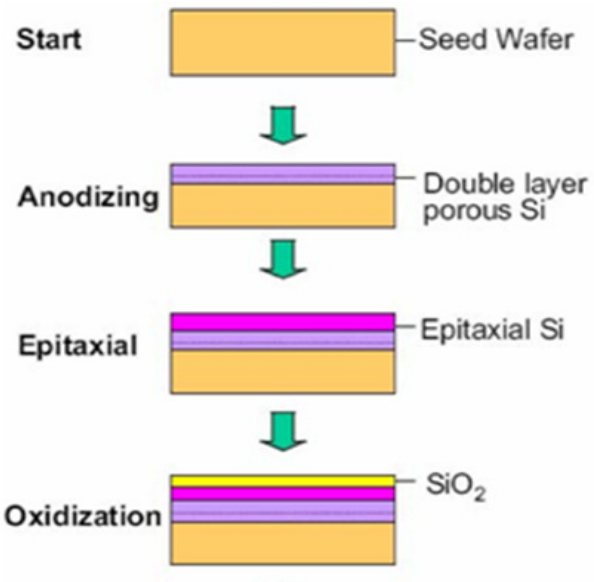


Fig: 1.3 silicon on sapphire

Since, the scaling of device dimension requires thinner and thinner top Si layer, considerable research efforts were made to develop SOI wafers with top Si layer having small but highly uniform thickness (thickness variation < 10%). As a result, plasma assisted chemical etching (PACE) process [9] and ELTRAN process [10] were developed in 1992 and 1994 respectively.



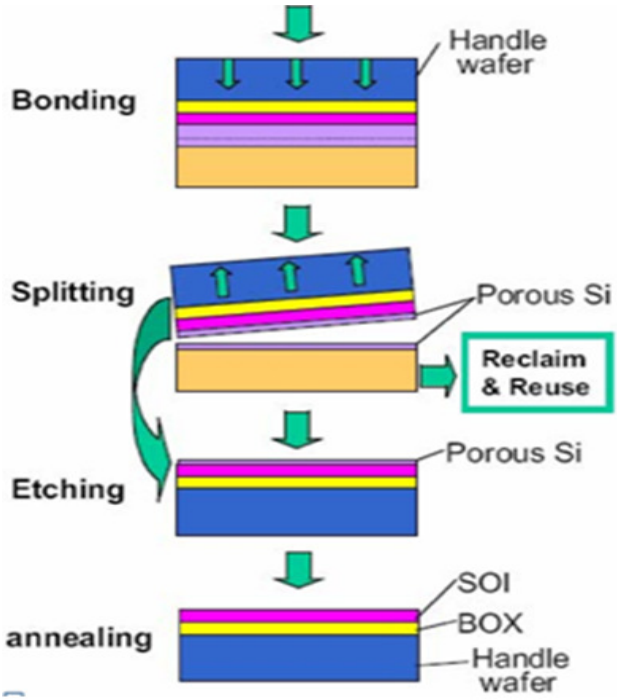


Fig: 1.4 ELTRAN Process

III OPERATION ON SOI MOSFET

The structure of an SOI MOSFET, as shown in figure 1.5 is similar to the conventional bulk MOSFET with the exception that the active silicon layer is separated from the bulk silicon substrate by a thick buried oxide layer.

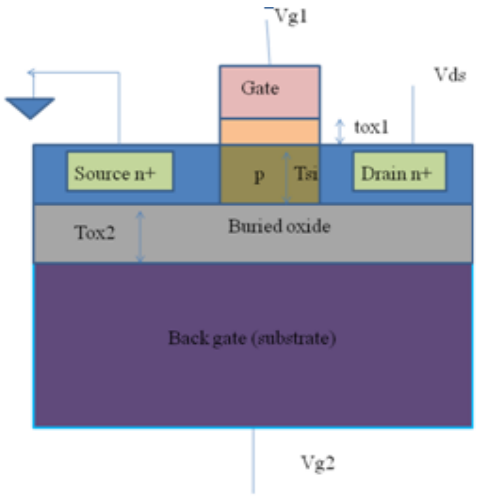


Fig: 1.5 Structure of an SOI nMOSFET

Depending on the silicon film thickness and the channel doping concentration, two types of SOI MOSFETs can be distinguished

a) Thick film SOI
b) Thin film SOI

In a thick-film SOI device the silicon film thickness is larger than twice the maximum depletion width, $X_{d\,max.}$

$$x_{d\,\max} = \sqrt{\frac{4\varepsilon_{Si}\Phi_F}{qN_A}}$$

where
Φ_F is the fermi potential as given below:

$$\Phi_F = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)$$

As a result, there is no interaction between the depletion zones arising from the back and front interfaces, and a neutral body of silicon piece exists beneath the front depletion zone. If we connected it to ground through a body contact, the device operation will same as of a bulk device. When the body is left electrically floating, it will behave as a bulk device, excepting the floating body effects.

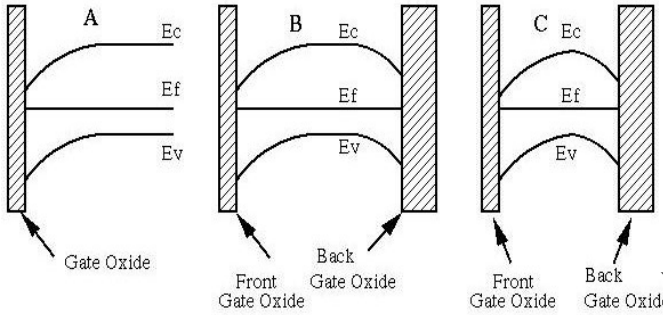


Fig: 1.6 Band Diagram in a bulk (A), a thick-film SOI (B), and a thin-film SOI Device (C)

In a thin-film SOI device the silicon film thickness is smaller than $X_{d\,max}$. The silicon film is fully depleted at threshold, irrespective of the back-gate bias (with the exception of a possible presence of thin accumulation or inversion layers at back interface, if a large negative or positive bias is applied at the back gate, respectively). Among all SOI MOSFETs, fully depleted SOI devices having back interface depleted, which exhibit the most attractive properties, such as low electric fields, excellent short channel behavior, a quasi-ideal subthreshold slope and high trans-conductance.

Medium thickness SOI device is an intermediate case between thin and thick film device, and is obtained when $X_{d\,max} < t_{si} < 2\,X_{d\,max}$, t_{si} being the film thickness. If the back gate bias causes the front and back depletion zones to coalesce, the device behaves like a thin film device; otherwise it behaves as a thick-film device.

In PD MOSFET, a part of the body region remains undepleted or neutral while in FD MOSFET, whole of the body, the depletion region extends right up-to the body and BOX interface. Thus in FD SOI MOSFET, the complete body region is depleted off majority carriers.

A. *Threshold Voltage*

For a thick-film SOI device, which essentially behaves like a bulk device due to absence of interaction between the front and back depletion regions, the threshold voltage is same as in a bulk device and is given as:

$$V_{th} = V_{FB} + 2\Phi_F + \frac{qN_a x_{d\,\max}}{C_{ox}}$$

Where
V_{FB} is the flatband voltage,
Φ_F is the fermi potential, and
x_{dmax} is the maximum depletion width.

For a thin-film SOI device, the expressions for threshold voltage as a function of the different possible steady-state charge conditions at the back interface are given as [18]:

$$V_{th1,inv2} = \Phi_{MS1} - \frac{Q_{ox1}}{C_{ox1}} + 2\Phi_F - \frac{Q_{depl}}{2C_{ox1}}$$

$$V_{th1,depl2} = V_{th1,acc2} - \frac{C_{Si}C_{ox2}}{C_{ox1}(C_{Si}+C_{ox2})}(V_{G2} - V_{G2,acc})$$

$$V_{th1,acc2} = \Phi_{MS1} - \frac{Q_{ox1}}{C_{ox1}} + (1+\frac{C_{Si}}{C_{ox1}})2\Phi_F - \frac{Q_{depl}}{2C_{ox1}}$$

Where
Q_{s2} is the charge in possible back inversion or accumulation layer,
ϕ_{s1} and ϕ_{s2} being the potentials of front and back silicon/oxide interfaces,
ϕ_{s1} and ϕ_{s2} being front and back work functions respectively.

B. *Output Characteristics*

The expression of the current characteristics I_D (V_{G1} , V_{G2} , V_{DS}) of a thick-film SOI MOS transistor is identical to that of a bulk MOSFET, with some modifications due to the parasitic bipolar effects coming up due to the presence of an electrically floating body. The derivation of the current characteristics of a thin film, fully depleted SOI device can be done [18] using assumptions of the classical gradual channel approximation [11]. The saturation current in an SOI MOSFET is given as:

$$I_{Dsat} \cong \frac{1}{2}\frac{W}{L}\frac{\mu_n C_{ox1}}{(1+\alpha)}(V_{G1} - V_{th})^2$$

Where:

$$\alpha = \frac{C_{Si}}{C_{ox1}}$$

(for fully depleted device in accumulation)

$$\alpha = \frac{C_{Si}C_{ox2}}{C_{ox1}(C_{Si} + C_{ox2})}$$

(for fully depleted device in depletion)

$$\alpha = \frac{\varepsilon_{Si}}{x_{d\max}C_{ox}}$$

(for partially depleted and bulk devices)

Since, α fully depleted SOI < α bulk < α back accum SOI, the drain saturation current is highest in the fully depleted device than bulk device, and the device with back accumulation. The high saturation current in a thin-film, fully depleted SOI MOSFETs brings about an increase in current drive, which contributes to excellent speed of fully depleted SOI CMOS circuits.

IV SOI CHARECTERISTICS

In a bulk MOS transistor, only the top region of the silicon wafer is relevant for electron transport. SOI structures emerged from the idea of isolating the active device overlay from the detrimental influence of the underlying silicon substrate by a buried oxide layer.

A. *Dielectric Isolation*

SOI circuits consist of single device, dielectrically isolated from each other and from the substrate. Each device sits alone on the top of the insulator, there are no leakage paths to the substrate or to the adjacent devices. This allows both analog and digital devices to be used on the same chip. The inter-device distance is much more shrinkable in SOI than in bulk. This critical limitation of bulk technology for VLSI circuits is due to unavoidable proximity of diffused regions that belong to adjacent components. Sophisticated techniques of trench isolation are necessary to avoid latch-up in bulk silicon technology. Latch-up refers to unintentional activation of parasitic devices. In figure 1.7 the superposition of PNP and NPN transistors, which have the common diffused regions, is a thyristor which causes uncontrollable high currents and leads to circuit failure when turn on. while, SOI is naturally free from latchup problem.

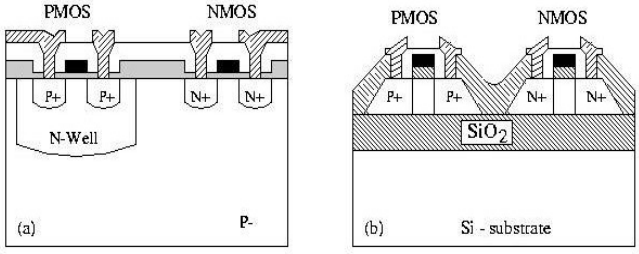


Fig: 1.7 Schematic configurations of CMOS transistors in bulk and SOI wafers

B. *Vertical Junctions*

In regular SOI films, the source and drain regions extend to the insulator, and only their lateral sides serve as junctions The surface of junction is much smaller than in bulk silicon. The smaller surface brings a substantial reduction in parasitic capacitances, and in propagation delays and dynamic power consumption. In short, for predefined power consumption, faster and much denser circuits can be integrated on SOI wafers.

C. *Short Channel Effects*

In small geometry MOS transistors, the source and drain junction induced depletion zone become relatively significant and impede the gate control over the whole space charge region they impede the gate control. A number of small channel effects like threshold voltage roll-off, degradation of subthreshold slope, punch-through drain induced barrier lowering etc. originate due to the "charge sharing" between gate and junctions. SOI devices are more immune to short-channel effects [12]. Basically, the extension of source/drain depletion regions is restricted by the junction size and the dual gate control (via front-gate and silicon substrate) of the surface potential.

D. *Reliability*

The primary motivation for developing SOI technologies was their excellent tolerance of transient radiation effects. The incoming particles generate electron-hole pairs in proportion to the volume of device. This photocurrents acts as leakage currents, causing charge collection and soft errors. It dramatically reduced in SOI as the volume exposed to carrier generation is 2-3 orders of magnitude smaller than in bulk Si, due to the presence of buried oxide layer in these devices. when ionizing radiation flows through a transistor, it creates a tail of mobile charge particles on its wake which increase with the path length of the radiation. since mobile charges can't be created there hence the buried insulator layer lessens the amount of mobile charge that is generated.

E. *High integration density and simplified process*

SOI CMOS offers a higher integration density than bulk CMOS. This high density results mainly from the absence of wells in SOI technology. SOI CMOS devices can be isolated by oxidation, on the other hand bulk devices normally use junction isolation.

F. *Reduced parasitic capacitances*

SOI CMOS devices are isolated from each other dielectrically. Such isolation reduces the parasitic junction capacitance. In a bulk CMOS device the parasitic junction capacitance consists of two components: the channel stop implant under the field oxide and the capacitance between the drain and the substrate when the device is scaled down to small dimensions, high substrate doping must be used to rninimize short channel effects. This increases the parasitic junction capacitance. In SOI CMOS devices there is only one cornponent of parasitic

capacitance between junction and the substrate. As the thick BOX layer (> 300nm) is taken in SOI, capacitance is much smaller than its corresponding counterpart in a bulk device. This reduction of parasitic junction capacitance contributes to the excellent speed performance observed in SOI CMOS circuits.

The presence of the buried oxide not only reduces the junction capacitance, it reduces other parasitic capacitances as well (it means all the parasitic capacitances between the silicon substrate and the various terminals [13].

G. *Subthreshold performance*

Inverse subthreshold dope can be related by equation:

$$S = \frac{\partial V_G}{\partial \log I_{Ls}} = 2.3\frac{kT}{q}\left(1 + \frac{C_{depletion}}{C_{ox}}\right)$$

It is a function of the ratio of $C_{depletion}$ to C_{ox} in a bulk Si CMOS technology, while scaling down the channel length results in a roll-off of the threshold voltage, which is called short channel effect. This causes due to the loss of control by the gate to part of the depletion zone below it. To rninimize the short channel effect, one should increase the doping level in channel region. It increases C_d and hence an increase in Inverse subthreshold slope. In a PD SOI structure, short channel effects are not so serious as in bulk Si CMOS. Therefore optimization of channel doping profile to achieve better inverse subthreshold dope with minimum channel effects. In a thin film SOI device, the channel region is fully depleted. It results as an inverse subthreshold slope in FD SOI MOSFET. For low-power low-voltage applications the lower inverse subthreshold slope is highly desirable because it allows the use of devices with a smaller value of threshold voltage without an increase in leakage current. This reduces the static power consurnption significantly.

V CHALANGES IN SOI TECHNOLOGY

It is generally acknowledged that SOI CMOS provides better device performance than its bulk counterpart. However, the presence of the BOX layer also results in self heating, floating body effects etc.

A. *Self Heating Effects*

Due to thermal isolation of substrate by the buried insulator in an SOI transistor, removal of excess heat generated by the Joule effect within the device is less efficient than in bulk, which leads to substantial elevation of device temperature[14]. The excess heat mainly diffuses vertically through the buried oxide and laterally through the silicon into the contacts and metallization. The device heats up to 50 to 150ºC due to the relatively low thermal conductivity of the buried oxide. This increase in device temperature leads to a reduction in mobility and current drive, thus degrading the device performance over a period of time[15][16].

B. *Floating Body and Parasitic Bipolar Effects*

The presence of a floating volume of silicon beneath the gate is at the origin of several effects related to SOI, generally referred to as floating body effects [17]. There exists a parasitic bipolar transistor in the MOS structure. If we consider an n-channel device, the N+ source, the P-type body and the N+ drain indeed form the emitter, the base, and the collector of an NPN bipolar transistor, respectively. The base of the bipolar transistor is usually grounded by means of a substrate contact in a bulk device. But, due to the floating body in an SOI MOSFET, base of the bipolar transistors is electrically floating. This parasitic bipolar transistor is origin of several undesirable effects in SOI devices.

C. *Kink Effect*

As V_{ds} increases, electron-hole pairs are generated due to impact ionization. Electrons can easily move into the drain region while holes migrate to the floating body, at the place where the potential is low. Because of the existence of the buried oxide layer Holes cannot be extracted through the substrate and are trapped in the neutral region. The accumulation of holes increases the potential in the bulk and decreases in the threshold voltage. Resulting a kink is observed in saturation region.

The injection of holes into the floating body forward biases the source-body diode. The floating body reaches a positive potential, as given by the following equation [18]:

$$I_{holes,gen} = I_{SO}\left(\exp\left(\frac{qV_{BS}}{nkT}\right) - 1\right)$$

Where:

$I_{holes,gen}$ is the hole current generated near the drain,

I_{so} is the saturation current of the source-body diode,

V_{BS} is the potential of the floating body,

n- is the ideality factor of the diode.

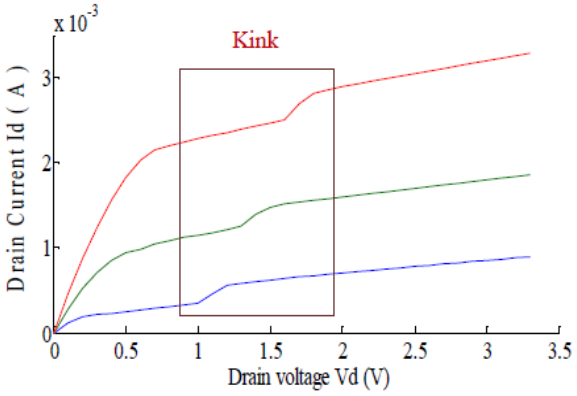


Fig:1.8 Kink effect in SOI MOSFET structure

D. *Single transistor latch-up*

Due to the floating body existence. lateral bipolar action become more frequent in SOI MOSFET. Due to impact

ionization near channel-drain junction the base current in the parasitic bipolar is formed. In NMOSFET the parasitic BJT effects are more serious than that in PMOSFET, the reason behind this is the impact ionization which is more pronounced in NMOSFET than in PMOSFET.

In bulk NMOSFET, the holes generated by impact ionization flow as substrate current. By the way, holes generated by impact ionization are trapped in the neutral region in the SOI structure. when the rninority carrier lifetime in the silicon film is high enough, the parasitic NPN BJT presented in the NMOSFET device can amplify the base current(i.e. the hole current generated by impact ionization near the drain). It results in an increase of drain current. As a result, when the current is higher than certain Ievel, the parasitic BJT will be dominant.. The gate may even lose the control to source drain current. The phenomenon is referred as the single transistor latchup [19] . generally it may cause malfunction of the circuit. Notice that such effect only happens when V_{DS} is larger than $V_{GS} - V_{th}$, since the impact ionization only occurs when the device operates in saturation region.

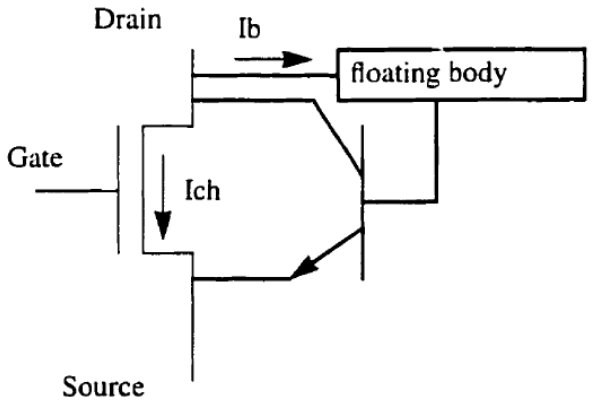


Fig: 1.9 Parasitic NPN bipolar junction transistor in SOI NMOSFET structure.

E. *Reduced drain breakdown voltage*

Because of the existence of parasitic NPN BJT structure in SOI NMOSFET, The current generated by the impact ionization is amplified. This results in the reduced breakdown voltage of SOI NMOSFET. Normally larger the beta value of parasitic BJT, the smaller the breakdown voltage. Such reduction of breakdown voltage is more significant in short channel devices and when the good lifetime SOI materiais are used, since the beta in such kind of devices is much larger than unity [20].

VI CONCLUSION

As the silicon on insulator technology becomes mainstream technology it becomes more important to compensate and handle for the challenging issues like kink effect, self heating effect, short channel effect etc using SOI. Although various method has been already presented to reduce the kink effect like SELBOX structure but it need to be more precise for the better frequency response. In comparison with traditional bulk technology SOI technology need to be more suited for the nanometer and low supply voltage technology. It is also expected that the power consumption should decrease.

REFERENCES

[1] M. Watanabe and A. Tooi, “Formation of SiO2 Films by Oxygen-Ion Bombardment”, Japan J. Appl. Phys., Vol. 5, pp. 737-738, 1966.

[2] S. Nakashima, T. Katayama, Y. Miyamura, A. Matsuzawa, M. Imai, K. Izumi and N. Ohwada, “Thickness Increment of Buried Oxide in a SIMOX wafer by High Temperature Oxidation”, Proceedings 1994 IEEE International SOI Conference, pp. 71-72, 1994.

[3] C. Jaussaud, J. Margail, J. Stoemenos and M. Bruel, “High Temperature Annealing of SIMOX Layers, Physical Mechanism of Oxygen Segregation”, Proceedings of Mat. Res. Soc. Symp., Vol. 107, pp. 17, 1988.

[4] J. Stoemonos, “Microstructure of SIMOX buried oxide, mechanisms of defect formation and related reliability issues,” Microelectron. Eng., vol. 22, p. 307, 1993.

[5] B.Y. Tsaur, “Zone-melting-recrystallization silicon-on-insulator technology,” IEEE Circuits Devices, vol. 3, p. 13, 1987.

[6] G. Bomchil, A. Halimaoui, and R. Herino, “Porous Silicon: The Material and Its Applications to SOI technologies,” *Microelectron. Eng*., vol. 8, p. 293, 1988.

[7] K. Mitani and U.M. Gosele, “Wafer Bonding Technology for Silicon-On-Insulator applications: A Review,” J. Electron. Materials, vol. 21, p. 669, 1992.

[8] S. Cristoloveanu, “Silicon films on sapphire,” Rep. Prog. in Phys., vol. 50, p. 327, 1987.

[9] P.B. Mumola, G.J. Gardopee, P.J. Clapis, C.B. Zarowin, L. D. Bollinger and A.M. Ledger, “Plasma Thinned SOI Bonded Wafers”, Proceedings 1992 IEEE International SOI Conference, pp. 152-153, 1992.

[10] T. Yonehara, K. Sakaguchi and N. Sato, “Epitaxial Layer Transfer by Bond and Etch Back of Porous Si”, Appl. Phys. Lett., Vol. 64, pp. 2108-2110, 1994.

[11] S.M. Sze, “Physics of Semiconductor Devices,” 2nd Ed., New York, J. Wiley & Sons, 1981.

[12] S. Veeraraghavan, and J.G. Fossum, “Short channel effects in SOI MOSFET’s,” IEEE Trans. on Electron Devices, vol. 45, p. 522-528, 1999.

[13] A. J. Auberton-Herve, "SIMOX-SOI technologies for high speed and radiation hard technologies: status and trends in VLSI and ULSI applications" Proc. of the 4th International Symposium on SOI technology and Devices, Ed. by O. Schmidt, Electrocliemical Society, Vol. 90, pp. 455 - 478. 1990

[14] T.-L. Hsu, D.D.-L. Tang , J. Gong, Low-frequency noise properties of dynamic-threshold (DT) MOSFET’s, IEEE Electron Device Lett,Vol. No. 20, (1999), pp. 532–534.

[15] F. Dieudonné, S. Haendler, J. Jomaah , F. Balestra, “ Low frequency noise in 0.12 μm partially and fully depleted SOI technology”, Microelectronic Reliab,Vol. No. 43, (2003), pp. 243–248.

[16] M. Bruel, “ Silicon-on-insulator material technology, Electron Lett” ,Vol No. 31, (1995), pp. 1201–1202

[17] J.-Y. Choi, and J.G. Fossum, “Analysis and Control of Floating-body Bipolar Effects in Fully Depleted

Submicrometer SOI MOSFET's," IEEE Trans. Electron Devices, vol. 38, p. 1384-1391, 1991.

[18] B. Cheng, V. Ramgopal Rao, and J.C.S. Woo, "Sub 0.18 um SOI MOSFETs Using Lateral Asymmetric Channel Profile and Ge Pre-amorphization Salicide Technology," Proceedings of the IEEE SOI Conference, October 5-8, Stuart, Florida, USA, 1998.

[19] C. E. D. Chen. M. Matloubian, B. Y. Mao, C. C. Wei and G. P. Pollack, "Single transistor latch in SOI MOSFETs" IEEE Electron Device Letters, vol. 9, pp. 636 - 638, 1988.

[20] M. Haond and J. P. Colinge, b6Analysios f drain breakdown voltage in SOI n-channel MOSFETs", Electronics Letters, Vol. 25, pp. 1640 - 164 1, 1989.