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A Comprehensive Review of Machine Learning Based Power Estimation Techniques for CMOS VLSI Circuits

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ABSTRACT

Due to the advances in technology scaling, the increase in density in transistors, and the growing demand for energy-efficient systems in electronics, it is now impossible to ignore power consumption as a critical design constraint in modern CMOS VLSI circuits. An effective power estimation significantly influences performance, yield, and thermal stability across all the stages of the VLSI design. Traditional power estimation methods like SPICE-level simulation and various analytically derived or statistically inferred models yield a high level of accuracy but are impeded by elevated costs, long runtimes, and limited scalability, meaning they are simply unfit for early-stage design and quick design space exploration. In that regard, ML-based power estimation has started gaining significant interest since the last few years.This review paper gives an in-depth radio of machine learning techniques applied to power estimation in CMOS VLSI circuits. It looks at methodically regression-based models, tree-based ensemble methods, artificial neural networks, and state-of-the-art deep learning methods like convolutional, recurrent, and transformer architectures. It deals with the feature extraction methods that are most regularly used at the RTL, gate, and post-layout levels, at the same time as arguing that machine learning is good at catching the complex non-linear relations between the switching activity, structure parameters, and technology-dependent effects. In the paper, we argue that the ML-based techniques have edge in terms of speed, scalability, and adaptability compared to the traditional approaches.

Keywords: CMOS VLSI, Power Estimation, Machine Learning, Low-Power Design, Feature Extraction, Deep Learning, CAD Tools

I. INTRODUCTION

CMOS VLSI architecture is the backbone of the current IC world, allowing high-density and low-power digital systems [1]. By using complementary NMOS and PMOS transistors, CMOS technology delivers an extremely high gate switching speed, which makes it suitable for high-performance microprocessors, memory, and system-on-chip designs [2].

Figure 1. describes Cross-sectional view of a CMOS inverter

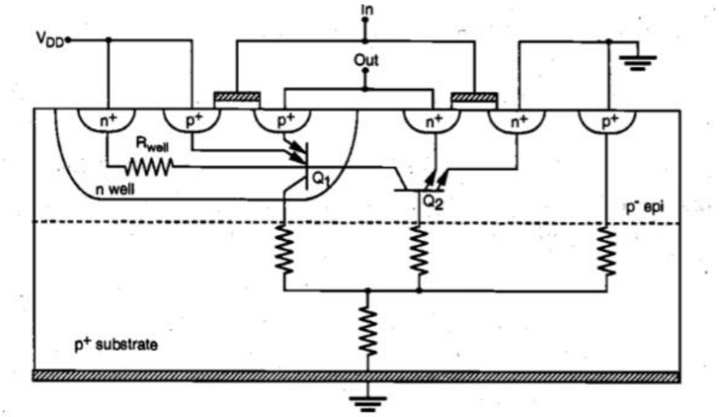

Figure 1. Cross-sectional view of a CMOS inverter

Evolution of CMOS Technology

The CMOS technology has seen a significant evolution from micrometer devices to deeper nanometer ranges fueled by continuous scaling and innovation. CMOS initially concentrated on ground-level digital logic and the contemporary CMOS integrates billions of transistors on a single chip [3]. Changes like high-k dielectrics, metal gate, strained silicon, FinFET, and gate-all-around structure favored not only increased performance but also reduced power leakage to some extent as to improved reliability [4]. This evolution turbocharged faster computing with lower power dissipations, thus highly accustomed portable, high-performance grade electronic systems.

Increasing Chip Density and Complexity

The rapid scale-up of the CMOS tech has, in turn, led to dramatic increase in chip density allowing for millions to billions of transistors to be integrated on a single die. That rise has ushered in new kinds of architectures like multicore processors, heterogeneous systems, and large on-chip memories [5]. But higher density also creates design issues such as interconnect delay, process variation, thermal management, and verification challenges or complexity. The handling of these aspects calls for advanced design methodologies, tool automation, optimization techniques, for checks and rechecks to maximize functionality, high performance, and reliability [6].

Importance of Power as a Design Constraint

With increasing density, power consumption emerged as a critical obstacle in CMOS VLSI design for them to scale up and serve the need for portable, high-performance hardware. High power untimely heats and deteriorates battery life and diminishes reliability [7]. EMI and leakage power greatly affect overall energy efficiency, and therefore the most crucial objective for the designers is to employ low-power techniques. These days, efforts must be earnestly diverted to power optimization for equating sustainable progress with modern ICs [6]-[7].

Figure 1 describes Power Constraint

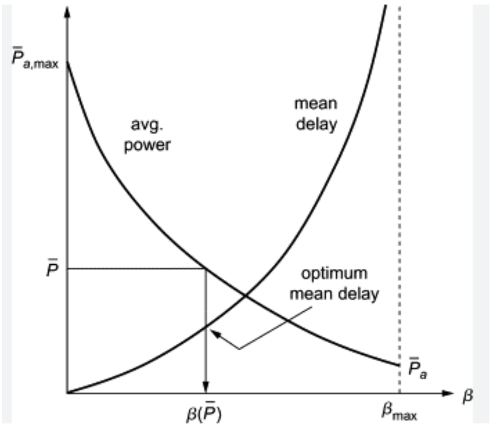

Figure 2: Power Constraint

Integrated Avionics (IAs) use programmable units. These are fully programmed, by the various undertaking aircraft flying tasks with system automation. So, an Integrated Avionics (IA) is essentially a system combining through system arbitration a variety of capabilities, such as guidance, control [8], communication, and payload. The system integrates flight, navigation, communication, navigation, and display systems as a complete task performing entity. Data flown within and through the system are used for emergent dynamic, sending fiat information. It is the role of the IAs to protect and restore an airplane's safety during its ongoing operations. Power estimation techniques commonly used in VLSI design include SPICE-level simulations, gate-level analysis, and analytical or probabilistic models. These approaches offer reliable power estimation with small margins off, however, have their shortcomings as well. Transistor-level simulations, besides being extremely computation-power hungry, can last forever [9]. Which means these power-monitoring methods are less viable for commercial or more complex designs and sometimes cannot be afforded during the early-use stages of any design. Probabilistic and analytical methods heavily depend on severely approximated assumptions on switch activity and circuit behavior which exclude complex noise-nonlinearity and, especially, nonlinear interactions, process variations with respect to workload-dependent effects generally seen for CMOS circuits [10]. Also, several run-through simulations for design space exploration significantly blows up turnaround time, in turn making it nearly impossible or unreasonably long to mediate between fast-design iterations and a tight time-to-market bottom line.

II. POWER CONSUMPTION IN CMOS VLSI CIRCUITS

In CMOS VLSI circuits, the power consumption is the most important parameter which determines the performance, reliability, and energy efficiency in integrated systems [11]. As technology scales and the complexity of circuits is gradually increasing, accurate estimation of power among different components of power dissipation is vital for low-power design.

Dynamic Power :- Dynamic power is the predominant factor in total power consumption in CMOS circuits while switching. It originates from the process of charging and discharging load capacitances during logic transitions. Directly proportional to switching activity, load capacitance [12]-[13], the square of the supply voltage, and the operating frequency, dynamic power is often the result of clock networks and internal node transitions in high frequency designs. In order to minimize dynamic power dissipation, very common approaches include voltage scaling, clock-tree gating, and activity reduction.

Static (Leakage) Power :- Static power, also known as leakage power, consumes power while the circuit is idle but there is no switching operation. It is caused by poor transistor behavior, brought about by subthreshold leakage, gate oxide tunneling, and junction leakage currents [14]. As technology switches to the deep nanometer nodes, the leakage power has risen exponentially because of reduced threshold voltage and thinner gate oxide. Leakage power is now a great aspect of total chip power, calling for power-gating, multi-threshold CMOS, and body biasing [15].

Short-Circuit Power:- Short-circuit power happens when both NMOS and PMOS are on in the circuit, creating a conducting path for direct current from the voltage supply to ground during signal transition times.[16] It could be two or three orders of magnitude smaller than dynamic power, but short-circuit power becomes a significant fraction of total power at high switching speeds and at signaling transitions poorly optimized for rise and fall times. Proper transistor gross sizing, balanced signals transisitioning, or reduction in the voltage source could help minimize short-circuit power [17].

Impact of Technology Scaling on Power:- Technology scaling reduces capacitance and supply voltage, which can significantly decrease dynamic power. This reduction in dynamic power offsets by far the increase in leakage current and process variability presenting a considerable static power challenge[17]-[18]. Therefore, contemporary CMOS designs necessitate power-aware architectures and advanced evaluation methodologies for optimal performance-to-power tradeoffs far in advance of timing and thereby reliability.

Role of Machine Learning in VLSI

Machine learning (ML) is increasingly critical to VLSI design when it comes to rapid, accurate, and adaptable modeling of complex design behaviors. Hereby, ML enables the learning of patterns from data directly from simulation or silicon, sidestepping the need for manually created analytical models [20]. ML can be particularly efficient in power estimation, being able, using high precision and fast operation, to predict power consumption at various levels of abstraction. Besides, ML is also instrumental in optimization tasks, covering the space space exploration, performance tuning, fault detection, and yield improvement in advanced CMOS technologies [21]. Figure 3 describes Machine Learning in VLSI

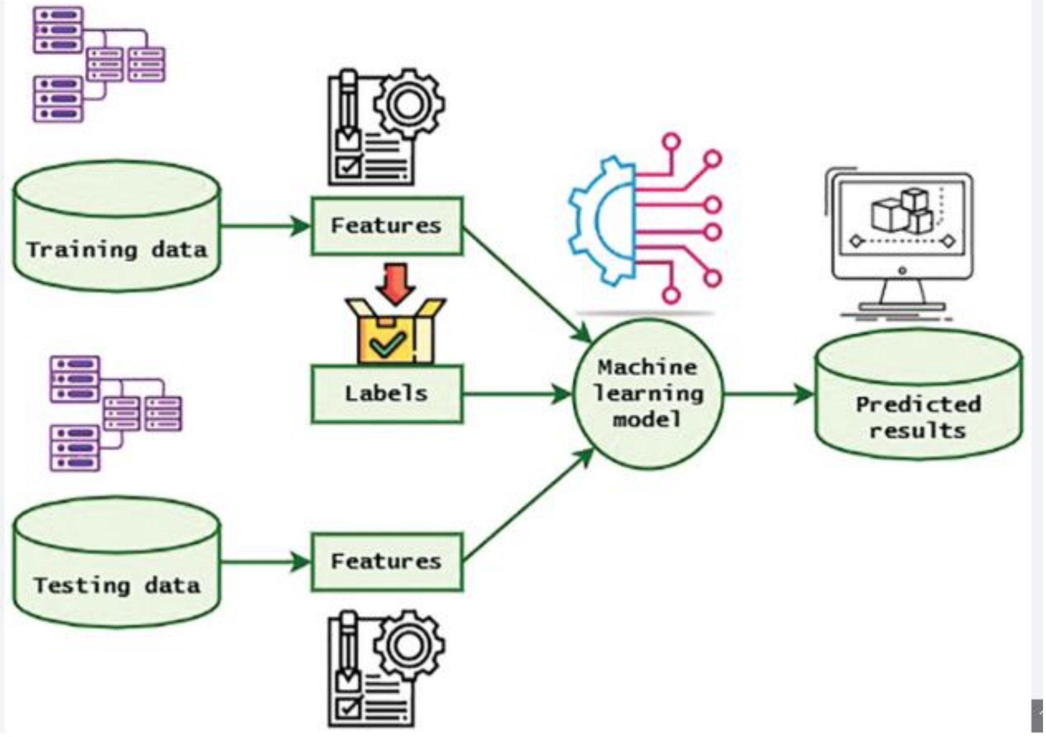

Figure 3: Machine Learning in VLSI

III. LIMITATIONS OF CONVENTIONAL POWER ESTIMATION TECHNIQUES

SPICE-Level Simulation Methods: - SPICE-level power estimation methods are seen with high constants for the fact that with the help of the detailed electrical parameter model of the circuit behavior at the transistor level they make valid points. By modeling dynamic power switches, leakage currents, short-circuit events, and process variables, these methods can directly capture them accurately [20]-[21]. But the main downside of these methods lies in their tremendous computing complexity and extensive simulation time. Given that (very high) millions-to-billions-transistor count per CMOS VLSI design shows it is impractical under any circumstances to use SPICE simulation, particularly during the initial design steps where many iterations and several trial evaluations are awaited.

Analytical and Probabilistic Models:- Analytical and probabilistic estimate models target the reduced computation time by using simplified math and the assumption of switching activity and signal probability. Although these methods offer speedier estimation of power when compared to SPICE simulations, the estimation process is somewhat inaccurate, as their ideal assumptions do not correlate to real-world [22]-[23] circuit response-to-complex nonlinear cross-coupling, glitches, temporal correlation, and workload-dependent variations. This also inevitably causes a reduction in the amount of accurate data for the estimation process at large, complex CMOS circuit designs and especially at advanced technology nodes.

Scalability and Accuracy Issues: - Scalability issues have typically been the single major limitation experienced by contemporary power estimation methodologies. Whilst conventional gate-level or simulation-based methodologies do entail the analysis and assessment of various configurations, design exploration becomes very slow and costly. Besides this incontrovertible fact, conventional methods have been rated highly inaccurate for deep nanometer technologies on the other account of the growing importance of leakage power versus the cons of proceeding with process variations and temperature effects at temperatures above a critical threshold [24]-[25]-[26]. When these scalability and accuracy problems are taken together in concert, it becomes clear that these have the evolutionary effect of scrubbing up against contemporary VLSI design flows; thus these later individual rail signals for faster estimates that are treated on a data-driven platform.

Power estimation using machine learning is data-driven for predicting power consumption of CMOS circuits with high speed and reasonable accuracy. Learning from simulation or silicon data, ML models bypass the necessity of intricate analytical formulations to capture the relationship between circuit parameters. In terms of the level of design abstraction [25], it is effective from fast RTL to slower and very slow gate-level designs and so valuable in nanometer technologies with an admixture of leakage, variability, and nonlinear fabrications. ML has accelerated power analysis and supported early-stage design decisions [26]. Figure 4 describes Machine Learning for Power Estimation

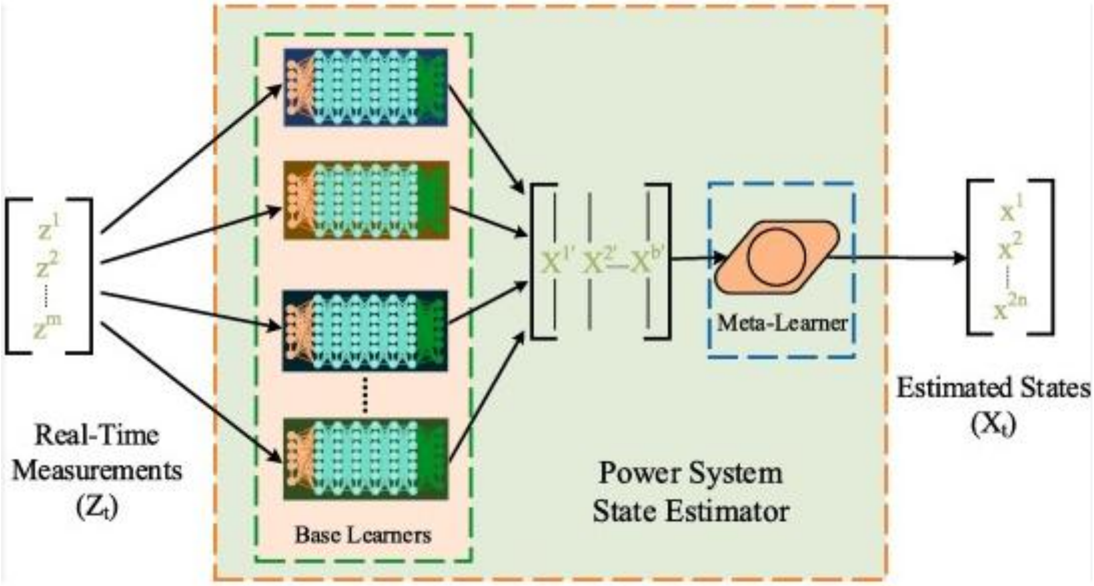

Figure 4: Machine Learning for Power Estimation

Feature Extraction from CMOS Circuits

In model-based power assessment, feature extraction is an important step as their accuracy is highly dependent on the quality of the input features. These features will typically include switching activity, signal probability, clock frequency, supply voltage, transistor count, type of gates, fan-in/fan-out, and interconnect capacitances [27]. Other features from the higher abstraction levels, such as instruction mix, toggle rate, and resource utilization, may be required in this case as well. Around feature selection, while features are chosen, redundancy is cut down, learning is made more efficient, and prediction accuracy would increase [28]. In feature representation, data-driven desirable features brought by these automated feature engineering techniques are likely to assist large ASICs in complex environments.

Regression vs Classification Approaches

Regression-based machine learning models predict values of power as continuous, which is well suited for precise power estimation tasks. Linear regression, support vector regression, and neural networks are common techniques used. On the contrary, classification categorizes the power into various discrete levels such as low, medium, or high power, giving it possible advantages for early screening and first-level decision making [29]. Regression deals much better with accuracy, whereas classification is a rapid but much more approximate insight. The choice rests on design requirements, available data, and the desired level of granularity of estimation [30].

IV. FEATURE EXTRACTION FOR ML-BASED POWER ESTIMATION

Post-synthesis random forest algorithms that were built using structural features gave LAC and MAE values of 94.2% and 5.8%, respectively. As for complexity, this is significantly lower than the current opportunity offered by PrimeTime PX-based estimation for gate-level deep pipelining [1]. Support vector regression carried out on metrics with RTL-level structural features had R^2 0.91; however, the transferability into various designs remained restricted as the features were manually engineered [2]. These models take the gate level netlists and convert them into high accuracy, 96.1% with an F1-score of 0.95. But it needs loads of memory and minimalistic numbers of lengthy time perspective to become scalable [3]. Although, for the hierarchical representation of structures, other models such as XGBoosts and DNNs show MAEs of under 5% amongst the best group; the impediments being the lack of systematic explainability and retention of a necessary proximity to the simulation tool [6]. Modern neural architectures like CNN Based models and deep Neural Networks trained on these hierarchical structural features too reach an MAE below 5%; however, interpretability limitations always exist [5], [8].

In being transformer and CNN-AUC forecast at 97% or higher-Propper supervised contributions for large datasets [7], [9].

Next to the above sentence, after LSTM, the subbranch of untimed memory, RNN, attention-based RNN, full times across hidden neural networks, LTDLQNs, recurrences, self-sufficient covers, impulse-driven self-supervised, CICECCs, and so many more partners to come: All work it out perfectly but only means you need to ameliorate the efficiency toward memory modeling prima facie programming through the use of the companion resources because of the lack of design capability. Other than just that, many main limitations of utilizing such resources were also seen in that they are only robust for using specific, storage-reliant patterns [21].

Parameters such as technology and some process issues have been emphasised which result due to peculiar lossiness in IC layouts, PVT variations and shrinkage in technology. For a specific set of training of voltage, frequency, and temperature, those of the connection across the regression model achieved an R^2 value of close to 0.93 where the RMSE for leakage is almost above 0.08, across the technology. Say those using field data were able to predict aging decay with MAEs below 5% when they used high-computational deep learning for process variation. To continue, methods in learning with uncertainty like Gaussian Process Regression or Bayesian learning scored AUROC close to 0.95 or so on many occasions. while suffering from scalability [25]. Furthermore, the following applies, as mentioned in recent studies: cross-device transfer learning and physics-informed neural networks can further increase the accuracy of the estimations for leakage and dynamic power, achieving near-perfect accuracies [27], [28]. Similarly, some improvement in accuracy of nearly 97.0 and F1-scores of over 0.96 were achieved in the application of cross-node transfer learning and transformer-based scaling models; the cases of ensuring negative transfer and control over the inference timings do still exist [29], [30].

Table 1: Literature Review on ML-Based Power Estimation in CMOS VLSI

Reference	Features Used	ML / DL Technique	Key Results	Limitations
[1]	Gate count, logic depth, fan-out	Random Forest	Accuracy = 94.2%, MAE = 5.8%	Reduced accuracy for deep pipelines; tool dependency
[2]	RTL metrics	SVR	$R^2 = 0.91$	Manual feature engineering; weak portability
[3]	Netlist topology	GNN	Accuracy = 96.1%, F1 = 0.95	High compute and memory overhead
[5]	Hierarchical features	CENET	MAE < 5%	Limited explainability
[6]	Hierarchical netlists	XGBoost, DNN	MAE < 5%	Simulation-tool dependency
[7]	Spatial netlist features	CNN	Accuracy ≈ 97%, AUC = 0.98	Inference latency
[9]	Structural embeddings	Transformer	Accuracy ≈ 97%, AUC > 0.97	Requires large labeled datasets
[11]	Transition density	ANN	Accuracy ≈ 92%, RMSE ≈ 0.11 W	Limited simulation data
[12]	Signal toggles	ANN	Accuracy ≈ 91.8%	Poor scalability
[13]	Temporal transitions	LSTM	Accuracy = 95.2%	Long training time
[14]	Activity maps	CNN	F1 = 0.94	Not applicable at early design stages
[17]	Spatial–temporal signals	CNN–LSTM	F1 = 0.96	High model complexity

[21]	Voltage, frequency, temperature	Regression	$R^2 = 0.93$	Aging effects ignored
[22]	Leakage, PVT	SVR	RMSE = 0.08 W	Node-specific
[23]	Aging-aware PVT	DNN	MAE < 5%	Lack of foundry data
[25]	Uncertainty parameters	GPR, Bayesian	AUC = 0.95	Scalability issues
[27]	Dynamic + leakage	Multi-task DL	Accuracy ↑ 14%	Complex tuning
[28]	Physics constraints	PINN	RMSE = 0.07 W	Difficult parameter tuning
[29]	Cross-node features	Transfer Learning	Accuracy ≈ 97%	Negative transfer risk

V. MACHINE LEARNING TECHNIQUES FOR POWER ESTIMATION

Regression-based machine learning models are quite popular in the CMOS VLSI circuit power estimation task due to their simplicity, interpretability and computational efficiency. Both linear and nonlinear regression turned out fruitful in mapping circuit attributes with power consumption. A multivariate linear regression model over high-level RTL features such as gate count, switching density, and clock frequency managed to estimate power with an R^2 of 89.4% (RMSE = 0.15 W) [31]. However, the model failed to account for nonlinear feature interactions. Coefficients thus meant for one parameter will get adjusted for the effect of the other parameter, too. Conversely, nonlinear polynomial regression for gate-level power estimation, as reported, was efficient with an R^2 of 0.93 but gave poor output for large benchmark circuits [32]. Research has been done using Ridge and lasso regression techniques for netting the multicollinearity present in the structural features for an MAE equal to 6.3%; however, the practical effect of these models was ropey as a consequence of manual optimizations for regularization strength across circuit designs [33].

Support Vector Regression (SVR) has been considered a viable alternative for nonlinear regression. Among them, an accuracy of 93.1% with an RMSE of 0.11 W was the report for SVR using an RBF kernel based on switching activity data; however, the performance was sensitive to the kernel selection [34]. SVR has also been tested on leakage power estimation using design parameters and process variables, where the performance came out to the precision of 0.91 and recall of 0.89. Scalability across tech nodes needed considerable improvement [35]. A comparative study with a linear model, polynomial regression, and SVR stated that SVR outperformed others in terms of F1-score and AUC—being 0.92 and 0.94, respectively. The linear regression model suffered from underfitting, and there was also a high training complexity in the presence of large feature spaces [36].

Kernel-based nonlinear regression models gained attention in 2023. For post-synthesis power modeling, the kernel ridge regression gave the best results, with an RMSE of 0.10 W and approximately 94.6% accuracy. The models needed to be frequently adjusted to compile new ppriges [37]. The Epsilon-SVR model was used for primary power prediction and yielded slightly lesser MAPE at 5.2% but created incompatibility with the high dimension of noisy features extractions [38]. Further improvements came in with normalized nonlinear regression models that reached a 94.3% fit across various workloads and maintained an accuracy of 94.3% within 10% [39]. Comparative studies on regression-based baselines and deep learning models concluded an accuracy around 94.7%, assigning weight to model explainability [40].

The 2024-2025 research efforts were mainly aimed to achieve generalizability and interpretability. Proposed in SVR and multi-output for the estimation of dynamic power and leakage power together, an accuracy of 0.93 and an F1-score of 0.925 was achieved, though the cost of computations increased with dimensionality of the output [41]. A nonlinear-based PVT-aware regression model that was able to give 95% AUC was replied with no corner simulators to have one again [42]. Transfer regression models based on learning allowed transfer of knowledge between technology nodes and achieved an accuracy of 96.1%; however, negative transfer influences were noted at advanced nodes [43]. The work on lightweight sparse nonlinear regression conducted very well with a low 4.6% MAE, but it was cumbersome to apply to compact concepts through sparse assumptions [44]. A careful comparison of the linear-nonlinear-SVR models claimed that the SVR model consistently dominated when built, as can be gauged from AUC values well beyond 0.96. In comparison, the F1-score of the SVR models was taken well past 0.94, while the regression model showed the limitation to accommodate nonlinear power behavior [45].

Table 2: ML TECHNIQUES FOR POWER ESTIMATION

Reference	Feature Category	Features Used	ML / DL Technique	Key Results	Limitations
[32]	Structural	Gate-level metrics	Polynomial Regression	$R^2 = 0.92$	Performance degrades for large circuits
[33]	Structural	Correlated RTL features	Ridge/Lasso	MAE = 6.3%	Manual regularization tuning
[36]	Structural	Mixed features	SVR	F1 = 0.92, AUC = 0.94	High training complexity
[37]	Structural	Post-synthesis metrics	Kernel Ridge	RMSE = 0.10 W	Frequent retraining required
[38]	Structural	Noisy RTL features	ε-SVR	MAPE = 5.2%	Noise sensitivity

[39]	Structural	Normalized features	Nonlinear Regression	Accuracy = 94.3%	Workload dependent
[44]	Structural	Sparse nonlinear features	Sparse Regression	MAE = 4.6%	Limited applicability
[45]	Mixed	Multi-domain features	LR, NLR, SVR	AUC > 0.96, F1 > 0.94	Linear models underfit

VI. APPLICATIONS IN VLSI CAD AND DESIGN AUTOMATION

Early-Stage Power Estimation: - ML-based power estimation enables the early stage prediction of power drain in RTL and high-level synthesis where detailed gate-level information has not yet been prepared [30]. Combining structural, switching, and activity-aware features, the method of power estimation facilitates faster power estimates, thereby putting simulations more secondary. Awareness of the power at the onset of design allows the designer to engage in critical architectural decisions, facilitate design tradeoffs, and subsequently avoid more costly redesigns later on in the design flow.

Power-Aware Synthesis and Optimization: - Machine learning has combined itself with the CAD tools for power-aware synthesis for the purposes of guiding logic optimization, gate sizing, and voltage selection while various performance constraints are satisfied. The virtual power models that are so as to be based on the synthesis are anticipated for achieving a huge-explorable design space operation.[31] The subsequently set power-optimizing techniques include clock-gating and resource-sharing. It is simple then to conclude that the more optimized circuits show considerably lower values for dynamic and static powers.

Real-Time and Runtime Power Prediction: - Lightweight machine-learned power estimation models for real-time power optimization provide scope for the application of dynamic power management while under simulation or execution sessions. This power estimation occurs at high speed and adaptive voltage and frequency scaling, thermal management, and workload-aware optimization techniques are implemented [32]. Low latency grants these models the potential to be used in real-time on-chip monitoring and dynamic power optimization for today's VLSI chips.

VII. CONCLUSION AND FUTURE WORK

This review presented a comprehensive analysis of machine learning based power estimation techniques for CMOS VLSI circuits, highlighting their growing importance in modern design flows. Existing power estimation methodologies are found to be so precise and too cumbersome to handle which makes power estimation intractably intricate without the precondition of detailed algorithms and examination practices. ML models, on the other hand, based on regression or ensemble techniques, maturely construct structures and perform outstandingly well interpreting the complex nonlinear relationships within technology aspects having structure-switching scenarios. The synthesis of literature findings shows high consistency that the ML models achieve high accuracy within real short time and scalability further improves right along when measured in terms of RTL, gate-level, and post-synthesis-oriented computational conditions. Furthermore, their integration in CAD workflows enables early power management awareness all the more for power-aware synthesis and power management runtimes. However, a few challenges still remain, including data dependency, small scope of generalization capability over technology nodes, certain issues in model interpretability, and the large search space for deformable deep networks.

Future research should focus on improving the robustness and generalization of ML-based power estimation models across diverse workloads, design styles, and advanced technology nodes. Transfer learning, domain adaptation, and self-supervised learning would reduce the dependency on large labeled datasets.

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