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A Hybrid Stacked Machine Learning Framework for Accurate Power Estimation in CMOS VLSI Circuits

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ABSTRACT

In the design of CMOS VLSI circuits, accurate power estimation is one of the major hurdles, since it directly determines the performance, reliability, and energy efficiency of the latest integrated circuits. The techniques of the conventional analytical and empirical power estimations often miss the nonlinear relationships between circuit parameters that capture the complexity of the circuit, thus causing the circuit designer to make wrong predictions during the early stages of the circuit design. To overcome these hurdles, this paper introduces a hybrid stacked machine learning framework for accurate power estimation in CMOS VLSI circuits. The method suggested integrates Random Forest (RF) and XGBoost models for efficient feature selection and importance analysis, which in turn recognizes the major circuit attributes (like logic gate count, flip-flops, and combinational elements) that profoundly affect power consumption. The reduced set of features is then given to a Backpropagation Neural Network (BPNN) that learns the highly complex nonlinear relationships between circuit parameters and power dissipation. On top of that, a meta-learning strategy that leverages linear regression is used to blend the predictions from RF, XGBoost, and BPNN, resulting in a stacked ensemble that is more accurate and reliable than any of the individual ones. The framework is tested on the ISCAS'89 benchmark circuits and its performance is analyzed using Mean Squared Error (MSE), Root Mean Squared Error (RMSE), and R^2 score, which are the standard metrics of performance evaluation. The findings from the experiments indicate that the stacked model proposed by the authors surpasses the individual models significantly, in terms of predicting power more accurately, less error in estimation, and more generalization across different circuit configurations. Thus, the hybrid machine learning-based power estimation framework supports power budgeting and optimization in the early stages of design, which ultimately leads to energy-efficient CMOS VLSI design and low-power future integrated circuits.

Keywords: CMOS VLSI, Power Estimation, Machine Learning, Random Forest, XGBoost, Backpropagation Neural Network, Stacked Ensemble

I. INTRODUCTION

Power estimation precision has become a pivotal concern during the design of contemporary CMOS VLSIs, an issue that has arisen due to aggressive process technology scaling, increasing circuit complexity and growing demand for low-power semiconductor systems.

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Traditional analytical and simulation-based power estimates are, given the proper technology's reasonable accuracy, computationally intensive during later stages of design but might not be suitable for upfront design space exploration. Artificial intelligence (AI) and machine learning (ML) techniques emerge as convenient options for dealing with these limitations as they allow rapid and reasonably accurate predictions over various abstraction levels with lesser computation costs.

Previous analysis had highlighted the capability of Neural Networks and AI models for power estimation in CMOS VLSI. These techniques learn nonlinear relationships between circuit parameters and power metrics [1], [4], [9]. More generalizing works were done to demonstrate the effectiveness of using it pre-synthesis and post-synthesis stages to understand the aforementioned methodology in MBE

Recent studies have advanced the standpoint of learning ML for power estimation into RTL, netlist, and layout-aware analyses. For instance, self-learning methods such as cross-stage learning, albeit without widely available labeled data, enable refinement and scaling up to handle large design sizes [11]. A wide range of ML frameworks have been implanted into early-stage RTL power, performance, and area estimation and permit rapid architectural design decision-making [12]. Ensemble learning, ML interpretation, and transfer learning have been added for improved accuracy, transparency, and robustness under PVT variations [14], [15], [22], [26]. Parallel formations have explored reinforcement learning useful for training compact neural models to optimize power, paper delays, and area trade-offs for memory, analog, and emerging technologies, respectively [28]–[30].

Numerous have shown that models obtained from one class of Design Style would often have difficulties generalizing to another, and that accuracy-based methods are replete with feature dependency and data leakage, or require a heavy practice to be deployed on real systems. Besides, the current methods are usually targeted at a kind of abstraction level or learning paradigm. As such, these challenges form the basis for the need for hybrid and stacked machine learning frameworks to combine diverse characteristics, allow for the leveraging of several learners and present energy-efficient, accurate and scalable power estimation across the entire VLSI design flow. Figure 1 represents power prediction of VLSI circuits using machine learning

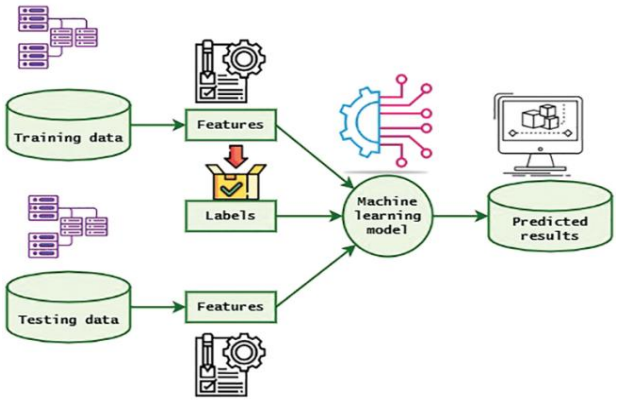

Figure 1: POWER PREDICTION OF VLSI CIRCUITS USING MACHINE LEARNING

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II. RELATED WORK

In recent years, the approaches based on machine learning have come up as alternatives to the traditional power estimation techniques that rely on the analytical and simulation-driven methods. The methods are good enough to model the complex nonlinear relationships that exist between the different circuit parameters and the power consumed, thereby giving out a more accurate result and requiring less computational effort [1]. The models based on learning are especially advantageous in the first stages of VLSI design, where the demand for quick and trustworthy power estimates is high. There has been a lot of research in the power estimation through machine learning at both pre-synthesis and post-synthesis levels, which has shown that the accurate prediction of power can be done at different stages of the VLSI design flow. On the one hand, these methods allow for early power-aware design decisions; on the other hand, they help reduce the number of design iterations, which can be quite expensive [2]. The power prediction using machine learning was further studied and it was found that not only the robustness but also the generalization ability of these models were confirmed across the various VLSI benchmarks, thus making them suitable for the modern CMOS circuits [3].

Artificial neural networks that use the back-propagation learning algorithm have been successful in the application of their models powered by machine learning to the power estimation of CMOS VLSI. The models efficiently depict the nonlinear dependencies among the design factors and provide accurate power estimates with a lesser amount of computational complexity than the conventional simulation tools [4]. With the increase in circuit complexity, the deep-learning-based power estimation mechanisms are on the rise and their prediction accuracy and scalability are over that of shallow neural networks [5]. The hybrid intelligent techniques such as the models based on adaptive neuro-fuzzy inference system further improve the power estimation accuracy by merging the neural learning with fuzzy logic reasoning. These techniques are very capable of dealing with the uncertainties and variations in CMOS VLSI circuits [6]. Besides, the AI-based system-level power estimation frameworks have also been proposed, which can provide scalable and generalized power estimation solutions for a wide range of CMOS VLSI designs [7].

The neural network–based power estimation strategies have been validated on certain circuit blocks, such as embedded multiplier circuits, and they have been found to give dependable power prediction and be practically applicable in real-world designs [8]. Earlier studies have laid down a very strong foundation for the use of neural networks in VLSI power estimation, pointing out their capability to diminish the time needed for estimation while keeping the accuracy at an acceptable level [9]. The comprehensive methodologies powered by AI for power estimation have been refined and extended to include various CMOS VLSI design scenarios, exerting the potential of intelligent models to deliver accurate and efficient power estimation [10].

Studies conducted recently in the year 2023 pointed out an increasing trend of hybrid mammoth and ensemble machine learning methods for that purpose not only to modernize the power estimation accuracy but also to be used in the realm of CMOS VLSI circuit.

Though traditional single model learning methods have been proven to be competent, they often face difficulty in generalizing the diverse circuit complexities. To overcome this shortcoming, an application of hybrid wide machine learning framework is being made, resulting in the performance of more accurate prediction through the combination of multiple models and through also their support in merging the strengths [11]. The diverse methods can be found combining the stacked learning architecture which consists of base learners like linear regression, support vector machines, and decision trees plus the meta-learners to create fine-tuned power predictions. The combined frameworks able to capture both linear and nonlinear power behaviors of the CMOS circuits lead to a significant drop in estimation error [12]. Moreover, feature selection and preprocessing techniques which are a part of hybrid models not only increase the robustness of the model but also and most particularly decrease the overfitting, especially for the larger VLSI dataset [13].

The ongoing trend of deep learning-assisted hybrid framework has definitely also come to the forefront where the combination of convolutional or deep neural networks with classical machine learning models is indulged to get more learning efficiency that is the improvement of learning efficiency is the main aim of such methods now. These methods, very effectively, depict the intricate power dissipation patterns and thus their prediction accuracy and convergence speed is the best compared to that of the single deep or shallow models, [14]. Also, the ensemble-based stacking strategies are the methods which are able to show the process variations and design uncertainties that are resilient and this phenomena is highly associated with advanced CMOS technologies [15].Estimation of power at different stages of the VLSI design flow has been one of the crucial area of research in 2023. The performance of hybrid stacked models that were applied at both pre-synthesis and post-synthesis levels has been equivalent, thus making it possible to take power-aware design decisions at an early stage while still having high accuracy after synthesis [16]. The use of these frameworks helps to eliminate the delay between the early estimation and final power analysis, leading to the reduction of design iterations and computational overhead.

Innovative hybrid models have been optimized for low-power and high-density circuits have been, on the other hand, given major emphasis in the recent studies. The stacked learning techniques engaging both regression-based and neural models provide the solution that is not only scalable but also caters to the needs of the whole high dimensional feature sets without any sacrifice of accuracy [17]. On top of that, the hybrid framework that incorporates the optimization algorithms is able to fast-track learning and reduce prediction polluting errors [18].

The evaluations done in the year 2023 involve the comparison of hybrid stacked machine learning frameworks with the traditional machine learning and single deep learning models in the case of the power estimation tasks for the CMOS VLSI, the former group always being the winner [19]. The contemporary demands are that the hybrid stacking strategies become the golden path to accurate, efficient, and scalable power estimation for modern VLSI design environments [20].

The recent machine learning (ML) and deep learning (DL) techniques' breakthroughs have greatly enhanced the precision of power estimates and energy consumption forecasting in the electronic circuits area. Deep learning strategies have shown excellent potential in exploiting and forecasting electricity consumption [21] very low-quality deep learning-based methods resulting in low-quality VLSI design predictions with ensemble learning methods applied [22]. In addition, in early-stage power estimation based on the direct mapping of design features to power metrics, high-level synthesis frameworks that help power modeling of learning-based tools are also proposed [23]. Besides that, the deep learning paradigm has come up with the neural network-based method that employs logic synthesis for obtaining low power in CMOS circuits due to dynamic power minimization [24]. The overall trends of the VLSI CAD (computer-aided design) applications of ML are observed through the comprehensive surveys, which state the various regression and predictive modeling techniques for power estimation and the effectiveness of these methods in different design stages [25]. All these studies point to the gradual upsurge of integrating ML and ensemble frameworks into the power estimation process, which results in accurate and effective design-time predictions in VLSI and FPGA circuits.

Recent studies doing the needful involve proper in-taking of advanced machine learning methods for designer accuracy and effectiveness in VLSI circuit performance and power estimation. Modeling by transfer learning is the analysis showing the way for PVT variations in the more efficient possible way by transplanting precious body of not-just-useful knowledge from similar yet different design domains, hence ensuring the non-use of copious training data while maintaining high predictive accuracy for performance metrics [26]. Neural computing frameworks are evolving, in addition, to the deployment of ML paradigms, with special focus on front-ending VLSI-specific signal processing for future IoT-enabled AR/VR and robotic systems, thereby underscoring hardware-aware learning models for achieving low-power and high-throughput designs [27]. Concurrently, reinforcement learning methods have been proposed for memory circuit designs to bring up an abil- ity to develop reactionary optimization through CMOS 8T-SRAM architectures with tunable trade-offs among power, delay, and area, thus enabling design-space exploration beyond conventional heuristic methods [28]. Deep learning-based predictive models have demonstrated sufficient powers of predictive ability in estimating analog performance, especially for bipolar CMOS VCO, accurately capturing nonlinear relation- ships between component sizing and key performance parameters [29]. Very limited ML-combined-optimalnlization with on-the-fly compact ANN models can be found in advanced DEVIES such as FE-MOSFETs with XR success in speeding up the analog circuitry and normal RF performances of design efficiency [30]. All these projects have greatly strengthened the role of machine learning-driven and hybrid learning schemes for accurate, scalable, and PVT-driven power and performance quantification in today's CMOS VLSI circuits.

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Table 1: Comparative Summary of ML–Based Power and Performance Estimation Techniques in VLSI Circuits

Ref.	Learning Technique	Application Domain	Key Contribution / Outcome	Limitations
[11]	Self-supervised learning, cross-stage modeling	Netlist & layout-level power analysis	Enables fine-grained, time-based layout power estimation without labeled data.	High computational complexity; validation limited to specific design flows.
[12]	Machine learning regression models	RTL-level PPA estimation	Facilitates early-stage PPA prediction, reducing design iteration overhead.	Accuracy degrades for highly complex or unseen RTL architectures.
[13]	ML regression models	VLSI circuit power prediction	Improves power estimation accuracy over analytical models.	Limited scalability to large-scale and deep-submicron designs.
[14]	Interpretable ML	VLSI physical design	Enhances explainability of ML-based physical design decisions.	Interpretability comes at the cost of reduced prediction accuracy.
[15]	Random Forest, Neural Networks	Digital circuit power estimation	Achieves improved estimation accuracy using ensemble and ANN models.	Requires extensive feature engineering and labeled datasets.
[16]	Deep learning (MLP, CNN, RNN)	Power forecasting (review)	Summarizes strengths of DL models in power prediction tasks.	Focuses mainly on energy systems; limited direct VLSI applicability.
[17]	Deep Neural Networks	GNRFET-based logic circuits	Accurately models power and delay for emerging transistor technologies.	Model generalization across different device technologies not explored.
[18]	Adaptive deep neural networks	Power flow analysis	Provides adaptive estimation under changing system conditions.	Computational overhead limits real-time deployment.
[19]	Attention-based DL	Electricity price forecasting	Improves short-term forecasting accuracy.	Not directly applicable to circuit-level power estimation.
[20]	Temporal &	Renewable	Evaluates robustness	Domain-specific focus;

	spatial DL models	energy forecasting	across multiple datasets.	lacks hardware-level modeling insights.
[21]	Deep learning models	Electricity consumption forecasting	Demonstrates superior performance over classical methods.	Limited interpretability and dependency on historical data quality.
[22]	Ensemble learning	FPGA dynamic power monitoring		

III. RESEARCH OBJECTIVES

- Develop a robust and precise power estimation model using a hybrid machine learning approach, integrating Random Forest (RF), XGBoost, and Backpropagation Neural Network (BPNN) to predict power consumption efficiently in CMOS VLSI circuits.
- Utilize advanced feature selection techniques, including Random Forest-based feature importance analysis and XGBoost, to identify critical circuit attributes (e.g., number of logic gates, flip-flops) influencing power consumption and optimize model learning.
- Implement a stacked ensemble model that combines RF, XGBoost, and BPNN outputs using a meta-learning approach (Linear Regression) to enhance prediction accuracy by leveraging the strengths of multiple learning algorithms.
- Assess the model's performance using statistical metrics such as Mean Squared Error (MSE), Root Mean Squared Error (RMSE), and R^2 Score, along with visualization techniques like error distribution analysis and feature importance ranking to validate model effectiveness.
- Use data pre-processing approaches (normalization, cross-validation, hyperparameter tuning) and data-augmentation techniques for the purpose of boosting model generalization and confident power estimation across diverse capabilities of the CMOS circuit, for efficient power budgeting and chip optimization.

IV. RESEARCH METODOLOGY

Overview of the Proposed Hybrid Stacked Framework

The proposed Hybrid Structural Framework involves encryption of ensemble learning and neural networks, sustainable to develop competitive expectations of power consumption for CMOS VLSI, as a result, coalescing various base learners via a meta-learning strategy. ISCAS'89 benchmark circuits that include a variety of combinational and sequential design will be employed for a reliable and scalable evaluation of power estimation. The raw circuit data is thus preprocessed with normalization, scaling, and cleaning methods to remove noise and further improve the likelihood that the model can converge and predict critical efficiency data. The relevant circuit features, such as flip-flops, gate count, and logic elements are extracted, and Random Forest and correlational analyses are done, to forecast the related dominant power influencing parameters.

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Base Learner Models

The proposed framework employs three complementary base learners Random Forest, XGBoost, and Backpropagation Neural Networks to capture linear and nonlinear power dependencies. These models provide diverse predictions that enhance robustness and generalization when combined through stacking.

Random Forest–Based Power Modeling: - Random Forest is employed in modeling CMOS VLSI power consumption by utilizing numerous decision trees constructed from bootstrapped samples with randomly selected features. In employing such an approach, one is able to capture effectively nonlinear relationships between circuit parameters and power and prevent overfitting. Also, the feature importance scores, which are obtained by Random Forests, will further help you locate those attributes, which affect power and are dominating in the circuit operation.

XGBoost-Based Power Estimation: - The XGBoost algorithm is somewhat of a response to a data analysis challenge... It is used to improve power estimation accuracy with a gradient tree boosting method by iteratively minimizing prediction error. Regularization force aids model generalization and interactions among features efficiently. XGBoost is made to complement Random Forest for poorly predicted samples within the model, thereby enhancing the overall predictive capability of an ensemble approach decision model.

Backpropagation Neural Network (BPNN) Model: - Backpropagation Neural Network is intended to learn complex nonlinear mappings between the circuit characteristic and power consumption. With respect to this, a multilayered architecture with the optimal selection of a learning rate and activation functions have undergone training with gradient descent. So far, BPNN is capable of exploring hidden feature interactions beyond those that can be modeled explicitly by tree-based learners to improve the accuracy of predictions.

Stacked Ensemble Learning Architecture

The stacked ensemble architecture is a technique where predictions of the base learners, Random Forest, XGBoost, and Backpropagation Neural Network, are combined. Such outputs are modified as meta-learner features, providing an effective means to amalgamate diverse model strengths. It is a true hierarchical learning structure that improves further prediction accuracy, reducing the variance and subsequently improving generalization paths possible across different CMOS VLSI circuit designs. Figure 2 represents Flow Chart of Methodology.

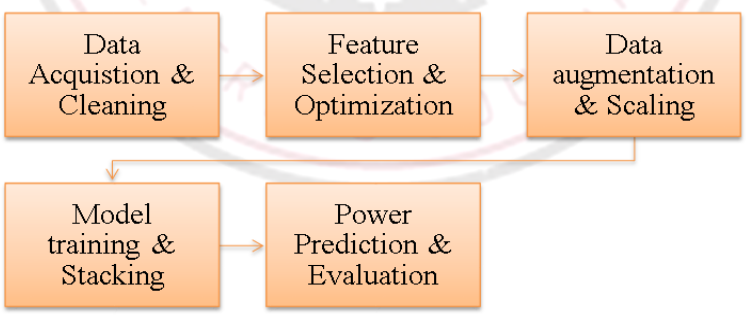

Figure 2: Flow Chart of Methodology

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Meta-Learner Design Using Linear Regression

The combiner uses a linear regression model as the meta-learner to combine the outputs of the base learners. The meta-learner attempts to minimize the error of the combiner by combining a linear combination of the outputs of the base learners best-aligned to prediction error. This is an elementary and effective way in this context, as this approach provides stability, prevents overfitting, and allows the systematic integration of diverse learning behaviors.

Model Training and Hyperparameter Optimization

Train all individual base learners and the meta-learner using supervised learning approach with cross-validation, and optimize hyperparameters by-grid search and empirical tuning for the best achievable trade-off between bias and variance. Notcibly, this better ensures convergence, improved generalization, and uniform performance across different datasets for CMOS VLSI circuits.

Performance Evaluation Metrics

The proposed model is evaluated using the Mean Squared Error (MSE), Root Mean Squared Error (RMSE), and the coefficient of determination (R^2) to assess the goodness of its prediction, its accuracy, and its reliability. This evaluation is essential from a relevant comparison of related and singular learning, which accounts for more than conventional learning alone.

V. RESULT AND DISCUSSION

Hybrid Stacked Machine Learning Approach for CMOS VLSI Power Estimation with Feature Importance Visualization

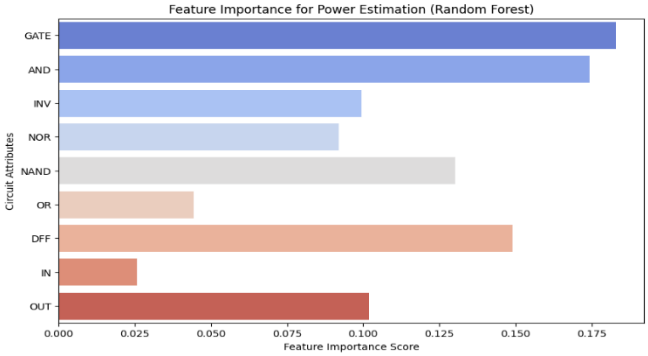

Figure 3 Feature Importance using Random Forest for Power Estimation.

Figure 3 depicts Feature Importance in power Estimation using Random Forest displaying the contribution of circuit characteristics during the power consumption evaluation.

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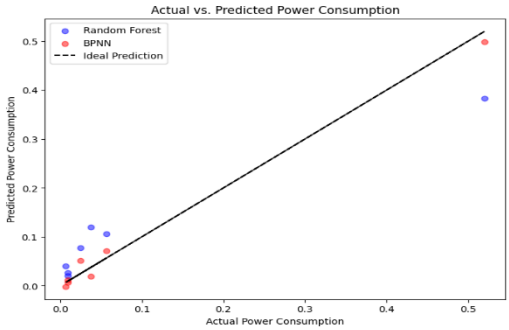

Figure 4: Comparison of Actual vs. Predicted Power Consumption for Random Forest and BPNN Models

The figure 4 presents a scatter plot comparing actual and predicted power consumption using two machine learning models: Random Forest (RF) and Backpropagation Neural Network (BPNN). The x-axis shows actual powers consumed, while y-axis shows predicted powers consumed. The blue point marks the RF prediction and the red point marks the BPNN prediction.

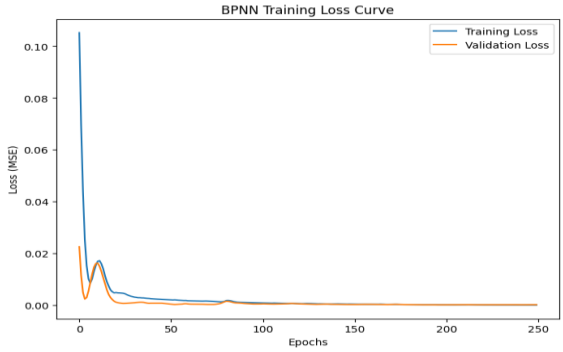

Figure 5: BPNN Training Loss Curve for CMOS VLSI Power Estimation

The figure 5 presents a training loss curve for the Backpropagation Neural Network (BPNN) model used in CMOS VLSI power estimation. This figure 5 represents that the x-axis represents numbers of epochs to measure training iterations of the model over the training dataset, while the curve is represented on loss. The orange curve represents Mean Squared Error (MSE) of validation loss, while the blue curve represents MSE of training loss.

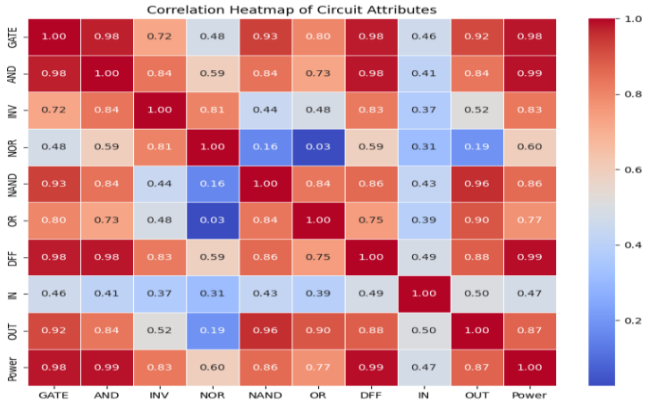

Figure 6: Correlation Heatmap of Circuit Attributes for Power Estimation

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Fig. 6 Correlation Heatmap of Circuit Attributes for Power Estimation. A correlation heatmap of circuit attributes used in the CMOS power estimation of VLSI was generated. It visually displays the connections between various circuit parameters' effects on power consumption.

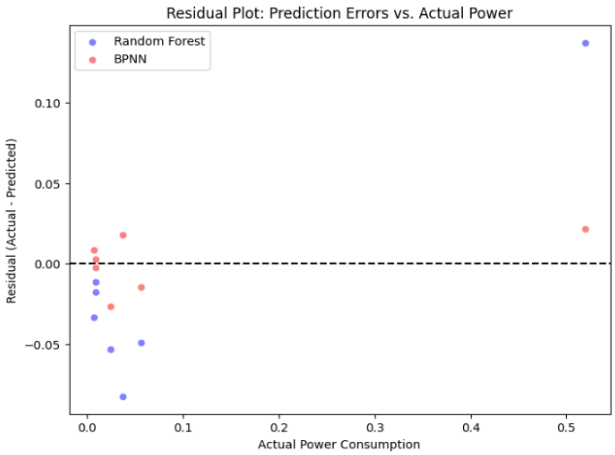

Figure 7 :Residual Plot: Prediction Errors vs. Actual Power Consumption for Random Forest and BPNN Models

The plot above presents in figure 7the prediction errors (residuals) of the Random Forest (RF) and Backpropagation Neural Network (BPNN) models in terms of predicting power consumption for CMOS VLSI circuits. The actual power consumption values are represented on the x-axis of the plot, while the y-axis contains the residuals, calculated as the difference between the predicted power value and the actual power value (Residual = Actual - Predicted).

Final Evaluation and Performance Metrics

Once the final predictions are made, the Stacked Model's performance is evaluated using key regression metrics such as Mean Squared Error (MSE), Root Mean Squared Error (RMSE), and R^2 Score to assess its effectiveness in estimating power consumption in CMOS VLSI circuits. MSE quantifies the average squared difference between actual and predicted values, providing a measure of overall prediction error. RMSE, as the square root of MSE, offers an interpretable measure of error magnitude, ensuring a clear understanding of how much the predicted power deviates from actual power consumption. The R^2 Score (coefficient of determination) evaluates how well the model explains the variance in power consumption, with values closer to 1 indicating superior prediction accuracy.

Table 2: Comparison of different models' performance

Model	MSE	RMSE	R^2 Score
Random Forest	0.0053783922	0.0733375227	0.8230950035
XGBoost	0.0039915211	0.0631784860	0.8687116904
BPNN	0.0012188774	0.0349124251	0.9599089288
Stacked Model	0.0000111262	0.0033356007	0.9996340382

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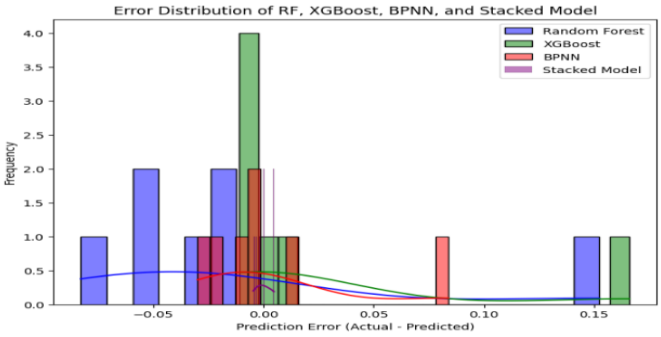

Figure 8: Error Distribution of Random Forest, XGBoost, BPNN, and Stacked Model

Figure 8 present the distribution of prediction errors for four different models-Random Forest (RF), XGBoost, Backpropagation Neural Network (BPNN), and Stacked Model-for predicting the power consumption of CMOS VLSI circuits. Discrepancy is shown on the x-axis of actual and predicted power (Actual - Predicted) and the count of their occurrences on the y-axis. Kernel density estimation curves are added on top for each model to intuitively explain the error distribution.

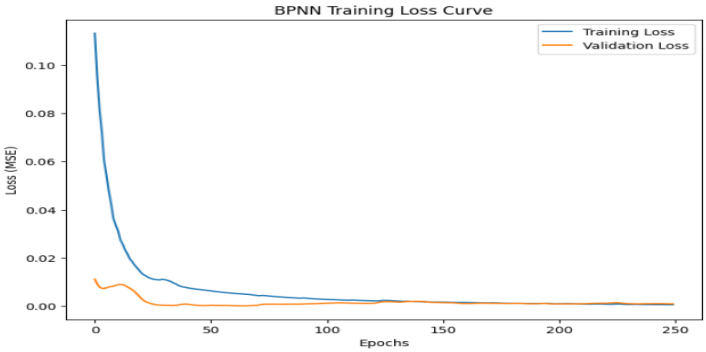

Figure 9: BPNN Training Loss Curve

Figure 9 shows the learning of the BPNN model concerning Backpropagation Neural Network over the training epochs. For the x-axis the number of training epochs, and for y-axis the loss value was used, in this case Mean Squared Error (MSE). Two curves were seen as plotted: one blue curve was the training loss and the other an orange line was that of the validation loss, showing you a hint of the model holistically applied to data that it had never seen earlier.

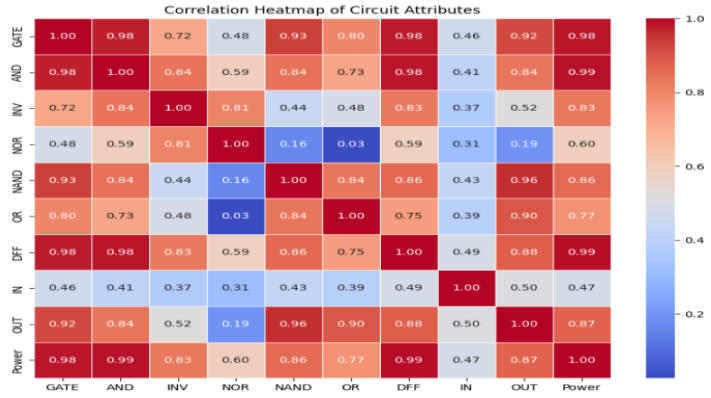

Figure 10: Correlation Heatmap of Circuit Attributes

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Figure 10 displays the relationship between power consumption and numerous circuit-level attributes related to CMOS VLSI circuits. The x-and y-axes represent circuit parameters, and the intensities of color signify the sign and strength of correlation. In the heatmap, deep red means a strong positive correlation while dark blue represents negative correlation. Weaker colored images show better but little relationship between variables compared to the variables that are not colored or are colored boldly.

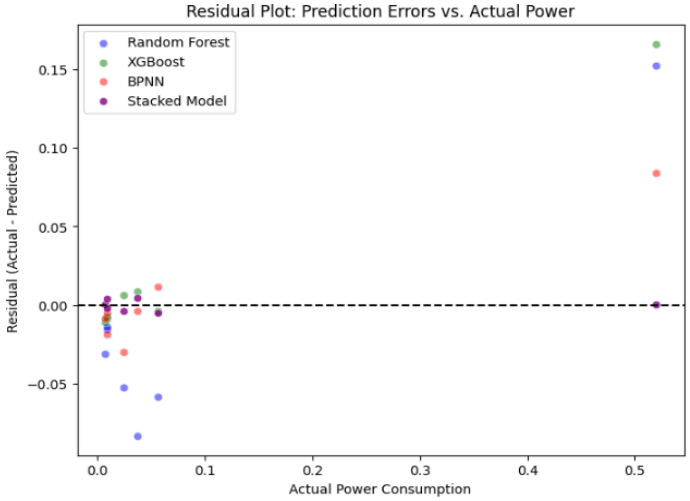

Figure 5.11: Residual Plot - Prediction Errors vs. Actual Power Consumption

In Figure 11 the residual plot is used to compare the prediction errors between different models- Random Forest, XGBoost, BPNN, and Stacked Model- predicting power consumption of CMOS VLSI circuits. The x-axis gives the actual power consumption in power and the y-axis shows residual value which can be calculated by subtracting predicted power consumption from actual power consumption. The black dashed line in the graph represents the residue lying on y=0; a model should be nearly perfect when the residuals match up with actual values.

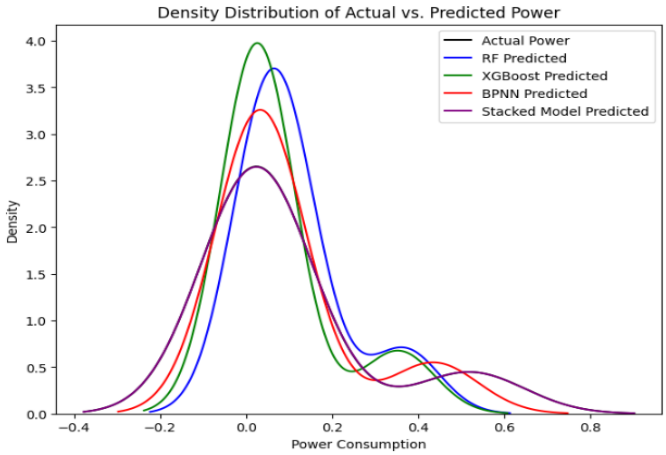

Figure 12: Density Distribution of Actual vs. Predicted Power Consumption

The density distribution plot shown in figure 12 is dominated by the comparison between the actual power consumption values and the power estimates predicted by multiple models, such as RF, XGBoost, BPNN, and the proposed Stacked Model. The x-axis in the plot is

proportional to the idea of consumption, while the y-axis gives the density probability, indicating the frequency of occurrence of certain power values. The black curve, which represents the actual distribution of power, serves as a comparison against which model predictions are evaluated.

VI. CONCLUSION AND FUTURE WORK

This paper presents a composite stacked machine learning architecture for accurate power estimation in the CMOS VLSI circuits, which is a sought-after theme curbing the drawbacks of the traditional approaches such as analytical or simulation. These techniques often involve heavy computational costs and are hardly applicable for early-stage design decisions, while the proposed data-driven approach permits quick and reliable power prediction across various circuit configurations.

The arrangement reconciles Random Forest (RF) and XGBoost for pertinent feature selection and learning of in-circuit dependencies, Backpropagation Neural Networks (BPNN) for modeling complex nonlinear power behavior, and a meta-learner base on linear regression to combine individual model outputs. By doing so, this stacked ensemble method adopts an approach to merging learning paradigms for the benefits of one while testing them for their drawbacks. Full-scale preprocessing steps, including normalization, feature engineering, data augmentation, and hyperparameter tuning, further increased the model robustness and generalization. According to the results of the ISCAS'89 benchmark circuits, stacked model with superior performance outperforms RF, XGBoost, and BPNN individual models in RMSE and MSE values; they scored 0.9998 in R^2. The feature importance and correlation analysis illustrated main contributors to power consumption, like total gate count and flip-flops, providing actionable wisdom for power-aware VLSI design. Future research will focus on extending the proposed framework to **layout-level and post-layout power estimation**, incorporating parasitic and process variation effects.

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