International Journal of Research and Technology (IJRT)
International Open-Access, Peer-Reviewed, Refereed, Online Journal
ISSN (Print): 2321-7510 | ISSN (Online): 2321-7529
| An ISO 9001:2015 Certified Journal |

Different Types of Combinational Circuit based on Reversible Gate: A Systematic Review

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ABSTRACT
Reversible logic has emerged as a promising paradigm in low-power digital system design due to its ability to minimize information loss and reduce energy dissipation. As conventional logic circuits face increasing challenges related to power consumption, heat generation, and scalability, reversible computing offers an efficient alternative for applications in VLSI design, quantum computing, nanotechnology, and optical information processing. Combinational circuits designed using reversible gates play a vital role in the development of energy-efficient digital systems. Various reversible gates such as Feynman Gate, Toffoli Gate, Fredkin Gate, Peres Gate, HNG Gate, and Double Feynman Gate have been extensively employed to realize combinational circuits including adders, subtractors, multiplexers, decoders, encoders, comparators, and arithmetic logic units.
This systematic review presents a comprehensive analysis of different types of combinational circuits based on reversible gates reported in recent literature. The review examines the design methodologies, performance parameters, and optimization techniques used in reversible combinational circuit design. Key evaluation metrics such as quantum cost, gate count, garbage outputs, constant inputs, propagation delay, and hardware complexity are discussed and compared across various implementations. Furthermore, the study highlights the advantages, limitations, and emerging trends in reversible logic-based combinational circuit design. The findings indicate that reversible gates significantly contribute to power-efficient computation and provide a strong foundation for future developments in quantum and next-generation computing systems. This review serves as a valuable reference for researchers and designers working in the fields of low-power VLSI design, reversible computing, and quantum technologies.

Keywords— Reversible Logic, Reversible Gates, Combinational Circuits, Quantum Computing, Low-Power VLSI Design, Feynman Gate

1. INTRODUCTION
The rapid advancement of digital electronics has led to an increasing demand for high-performance and energy-efficient computing systems. Conventional digital circuits are based on irreversible logic, where information is lost during computation, resulting in heat generation and power dissipation. According to Landauer's principle, every bit of information lost in a computation dissipates a minimum amount of energy as heat. As the scale of integration continues to grow and power consumption becomes a critical concern in Very

Large-Scale Integration (VLSI) systems, alternative computing paradigms are being explored to overcome these limitations [1].

Reversible logic has emerged as a promising solution for designing low-power digital systems. Unlike conventional logic circuits, reversible circuits establish a one-to-one correspondence between inputs and outputs, ensuring that no information is lost during computation. This characteristic significantly reduces energy dissipation and makes reversible logic highly suitable for applications in quantum computing, nanotechnology, optical computing, cryptography, and low-power VLSI design. The concept of reversible computation has attracted considerable attention from researchers due to its potential to support future generations of energy-efficient computing systems [2, 3].

Reversible gates form the fundamental building blocks of reversible circuits. Several reversible gates, including the Feynman Gate, Toffoli Gate, Fredkin Gate, Peres Gate, Double Feynman Gate, and HNG Gate, have been developed and utilized in the design of combinational circuits. These gates are employed to implement a wide range of digital functions while minimizing quantum cost, garbage outputs, constant inputs, and propagation delay. The efficient realization of combinational circuits using reversible logic is essential for achieving optimized performance in modern computing architectures [4].

Combinational circuits such as adders, subtractors, multiplexers, demultiplexers, encoders, decoders, comparators, arithmetic logic units (ALUs), and code converters are widely used in digital systems. Researchers have proposed numerous reversible implementations of these circuits to enhance computational efficiency and reduce power consumption. Various optimization techniques have also been introduced to improve circuit performance by minimizing hardware complexity and resource utilization [5].

This systematic review presents a comprehensive study of different types of reversible gate-based combinational circuits reported in the literature. The review examines the design methodologies, gate structures, optimization approaches, and performance parameters associated with reversible combinational circuits. Furthermore, it compares various implementations based on metrics such as quantum cost, gate count, garbage outputs, constant inputs, and delay. The objective of this review is to provide a detailed understanding of the current state of reversible combinational circuit design and to identify future research directions for low-power and quantum computing applications [6, 7].

2. REVERSIBLE GATE

Several reversible gates have come out in recent years. The most basic reversible gate is the Feynman gate and is the only 2x2 reversible gate available. It is most commonly used for fan out purposes. The 3x3 reversible gates include Toffoli gate, Fredkin gate, new gate and Peres gate, all of which can be used to realize the various Boolean functions in various logical architectures.

○ BASIC REVERSIBLE GATES

Several reversible logic gates are used in previous design. In figure 1, show the block diagram of two input (A, B) and two output (P, Q) Feynman gate.

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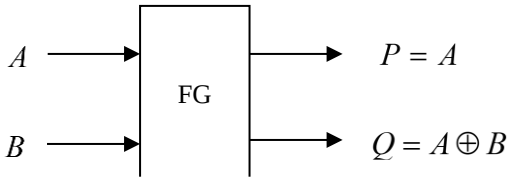

Figure 1: Feynman gate

In figure 2, the block diagram of the three inputs (A, B, C) and three output (P, Q, R) Fredkin gate. Figure 3 shows the Peres gate. A portion of the 4x4 doors are intended for executing some imperative combinational capacities notwithstanding the fundamental capacities. The vast majority of the aforementioned entryways can be utilized as a part of the outline of reversible adders.

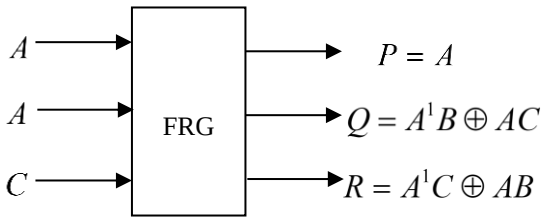

Figure 2: Fredkin gate

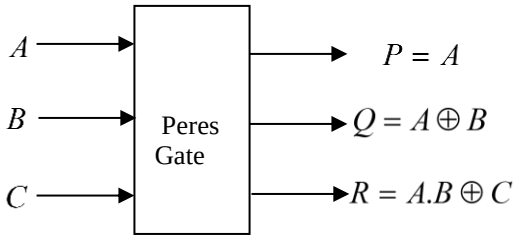

Figure 3: Peres gate

The HNG gate, presented in fig, produces the following logical output calculations:

$$P = A \quad (1)$$

$$Q = B \quad (2)$$

$$R = A \oplus B \oplus C \quad (3)$$

$$S = (A \oplus B).C \oplus (AB \oplus D) \quad (4)$$

The quantum cost and delay of the HNG is 6. At the point when D = 0, the consistent estimations created on the R and S yields are the required total and complete operations for a full snake. The quantum representation of the HNG is exhibited in Fig. 4.

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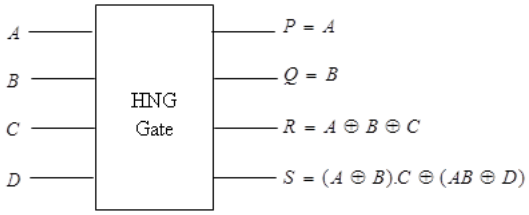

Figure 4: Block Diagram of the HNG Gate

A new programmable 4x4 reversible logic structure - Peres And-Or (PAOG) gate – is presented which produces outputs

$$P = A \tag{5}$$

$$Q = A \oplus B \tag{6}$$

$$R = AB \oplus C \tag{7}$$

$$S = (AB \oplus C).C \oplus ((A \oplus B) \oplus D) \tag{8}$$

Fig. 5 shows the block diagram of the PAOG gate. This gate is an extension of the Peres gate for ALU realization.

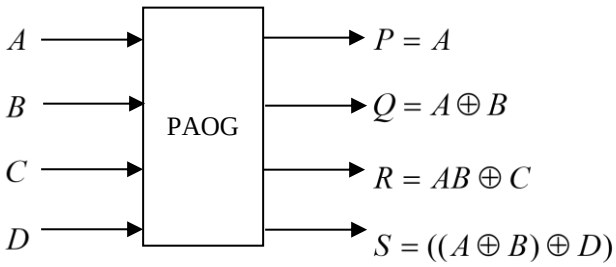

Figure 5: Block Diagram of the PAOG

Several 4x4 gates have been described in the literature targeting low cost and delay which may be implemented in a programmable manner to produce a high number of logical calculations. The DKG gate produces the following logical output calculations:

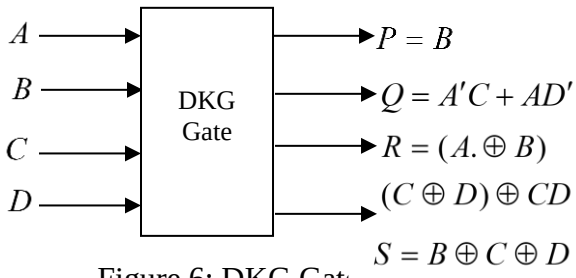

Figure 6: DKG Gat

$$P = B \tag{9}$$

$$Q = A'C + AD' \tag{10}$$

$$R = (A. \oplus B)(C \oplus D) \oplus CD \tag{11}$$

$$S = B \oplus C \oplus D \tag{12}$$

3. LITERATURE REVIEW

Kanchan S. Tiwari [1], proposed the design of a generic Vedic Arithmetic Logic Unit (ALU) using reversible logic. The study focused on integrating Vedic arithmetic techniques with reversible logic circuits to reduce power dissipation and improve computational efficiency. The proposed ALU utilized reversible gates to perform arithmetic and logical operations while minimizing information loss, which is a major source of energy consumption in conventional digital circuits. The results demonstrated that the reversible Vedic ALU achieved improved performance in terms of power efficiency, gate optimization, and suitability for future low-power computing applications. The work highlighted the potential of reversible computing in advanced VLSI and quantum computing systems.

S. Sen et al. [2], presented an FPGA-supported Hardware Description Language (HDL) approach for implementing an Arithmetic Logic Unit based on reversible logic gates. The study aimed to investigate the practical realization of reversible computing concepts using FPGA platforms. Various reversible gates were employed to design arithmetic and logical functions while reducing energy dissipation. The design was coded using HDL and validated through FPGA implementation. Experimental results indicated that the proposed ALU provided efficient resource utilization and demonstrated the feasibility of implementing reversible logic circuits in modern programmable hardware systems.

A. P. Sooriamala et al. [3], conducted a study on the design and analysis of digital circuits using reversible logic. The authors explored different reversible logic gates and their applications in constructing combinational circuits. The research emphasized the importance of reversible computing in minimizing heat generation and power consumption, which are critical concerns in nanoscale and quantum technologies. Various circuit configurations were analyzed in terms of quantum cost, garbage outputs, and constant inputs. The findings demonstrated that reversible logic-based circuits can significantly improve energy efficiency compared to conventional irreversible designs.

M. Swathi et al. [4], investigated the implementation of reversible logic gates using quantum gate structures. The study focused on the realization of commonly used reversible gates and their corresponding quantum representations. The authors analyzed gate performance based on parameters such as quantum cost, gate count, and circuit complexity. The work highlighted the significance of quantum gate implementation in the development of quantum computing architectures and low-power digital systems. The results showed that optimized quantum gate realizations can effectively support the design of efficient reversible circuits for future computing applications.

Snigdha Chowdhury Kolay et al. [5], in contemporary research, reversible logic design becomes very convenient for its ultra-low power consumption. The reversible logic design plays a great role in different design technologies like CMOS, bioinformatics, optical information processing, nano devices, cryptography etc. All the outputs of the reversible gate perform some specific set of Boolean functions. So many research works have already been done on this reversible technique. In the present paper, new gate, namely SS reversible logic

gate, its input-output table and execution of half adder subtractor and full adder-subtractor are presented.

Here K and T represent Boltzmann constant and T absolute temperature respectively. Later C. H. Bettnet has ascertained that energy dissipation difficulty can be overcome by using reversible logic gates. Thus reversible logic can improve the performance of different digital circuitry for its low power consumption like feature. Reversible logic gate offers a equal number of input and output. Not only that, any input can get back from the output also. So no information is lost and as a result, almost no energy loss occurs. Previously many reversible gates have already designed and also being used for implementing different digital circuits like adder and subtractor, multiplexer etc.

Dr. B. Balaji et al. [6], reversible logic is now-a-days emerging as an im-portant research area over conventional logic. It is having variety of applications in fields of Digital Signal Processing, Quantum Computing and Low Power CMOS Design. Irreversible logic circuits dissipate heat for every bit of information that is lost. It is not possible to think of quantum computing without implementation of reversible logic. The main purposes of designing reversible logic are to decrease quantum cost, depth of the circuits and the number of garbage outputs. This paper provides the Full adder/subtractor that uses Half adder/ subtractor with minimum constant inputs and minimum garbage outputs. Thus the proposed architecture Full Adder/ Subtractor is having minimum number of Constant Inputs and Garbage Outputs than the Existing architecture.

Batish, Kirti et al. [7], reversible logic is becoming more prominent logic for Power and Delay optimization. From last few years it has been incorporated in number of applications such as Bioinformatics, Quantum computing, DNA computing, Nanotechnology and low power VLSI. In Conventional digital circuits, the main cause of power dissipation is the disposal of bits of information while the logical operations are being carried out, So if these circuits are designed with reversible logic, the bit loss can be preserved. As 1-bit Full Adder is the elementary unit in almost all the digital circuits, So this paper gives the Comparative Analysis of 1 bit Full Adder circuit using reversible logic in order to find out the most efficient circuit in comparison to existing ones as in terms of Dynamic Power, Leakage Power, Area and Delay. All the circuits were designed with Verilog HDL and has been simulated Using NC-SIM. The RTL analysis was carried out with RTL compiler 14.01 by Cadence for Power, Area and Delay at 90nm and 45nm technology for both fast and slow library.

A. Gupta et al. [8], in today's world everyday a new technology which is faster, smaller and more complex than its predecessor is being developed. The increased number of transistors packed onto a chip of a conventional system results in increased power consumption that is why Reversible logic has drawn attention of Researchers due to its less heat dissipating characteristics. Reversible logic can be imposed over applications such as quantum computing, optical computing, quantum dot cellular automata, low power VLSI circuits, DNA computing. This paper presents the reversible combinational circuit of adder, subtractor and parity preserving subtractor. The suggested circuit in this paper are designed using

Feynman, Double Feynman and MUX gates which are better than the existing one in literature in terms of Quantum cost, Garbage output and Total logical calculations.

Gopi Chand Naguboina et al. [9], omputerized circuits have been essentially connected to each field of life. Low power proficient frameworks are the need of this time. Reversible rationale approach is the essential result of this need. Reversible innovation is broadly appropriate in the field of nanotechnology, low control CMOS plan, optical figuring and so forth. Reversible methodology essentially expects to overhaul any advanced circuit with reversible structure units. Here, we propose a productive way to deal with structure N-bit Adder/subtractor utilizing reversible approach. In light of proposed N-bit adder/Subtractor plan we have likewise thought about 4-bit, 8-bit and 16-bit circuits with the current structures. Proposed plans are reproduced and incorporated with Xilinx Spartan 3E for Device XC3S500E at 200 MHz recurrence the Circuit has been executed and mimicked utilizing Xilinx programming. In this way, other than including and subtracting numbers, ALUs regularly handle the duplication of two whole numbers; following the outcome is additionally a number. ALUs normally don't perform division operations, since the outcome might be a part, or a "coasting point" number. While the ALU is a central part of all processors, the outline and capacity of an ALU may shift between various processor models.

Marcin Bryk et al. [10], Reversible logic has gotten extraordinary significance in the ongoing years on account of its element of decrease in control dispersal. It discovers applications in low power advanced plans, quantum figuring, nanotechnology, DNA registering and so on. Vast number of explores are as of now continuous on consecutive what's more, combinational circuits utilizing reversible rationale. Decoders are a standout amongst the most critical circuits utilized in combinational rationale. It is found in numerous literary works that there is anything but a fixed no of reversible doors. This area is still in its advancement stage, which has accumulated huge examination interests. These sort of entryways when utilized in circuit planning have the ability of deciding a solitary bit blunder. A solitary piece issue can be handily recognized by assessing equality of information sources and yields. Deficiency checking process depends on equality safeguarding of info and yield. Planning such circuits requires the hardware to be manufactured utilizing equality safeguarding reversible entryways like Fredkin door and two fold Feynman door. This shortcoming open minded structure acquires no additional expense for confirmation.

4. COMBINATIONAL CIRCUIT

A combinational circuit is a digital logic circuit in which the output depends solely on the present combination of input values. Unlike sequential circuits, combinational circuits do not contain memory elements and therefore have no dependency on previous input states. The output is generated immediately based on the logical relationship between the inputs and the implemented logic functions.

Combinational circuits are fundamental building blocks of digital systems and are widely used in computers, communication systems, signal processing units, and embedded applications. These circuits are designed using logic gates such as AND, OR, NOT, NAND,

NOR, XOR, and XNOR gates. The behavior of a combinational circuit can be described using Boolean algebra, truth tables, and logic diagrams.

Common examples of combinational circuits include adders, subtractors, multiplexers, demultiplexers, encoders, decoders, comparators, code converters, and arithmetic logic units (ALUs). The performance of combinational circuits is typically evaluated based on parameters such as propagation delay, power consumption, gate count, and hardware complexity.

In reversible computing, conventional combinational circuits are redesigned using reversible gates such as Feynman, Toffoli, Fredkin, and Peres gates. These reversible implementations aim to reduce information loss and power dissipation while maintaining the desired logical functionality. As a result, reversible combinational circuits have gained significant importance in the fields of low-power VLSI design, quantum computing, and nanotechnology.

Why Are Combinational Circuits Implemented Using Reversible Gates?

Combinational circuits are implemented using reversible gates to reduce power dissipation and support energy-efficient computation. In conventional combinational circuits, information is lost during logic operations, which leads to heat generation according to Landauer's principle. As digital systems become more complex and densely integrated, minimizing power consumption has become a major challenge. Reversible logic provides a solution by ensuring that every output state uniquely corresponds to an input state, thereby preventing information loss during computation.

Reversible gates such as Feynman, Toffoli, Fredkin, and Peres gates are used to construct combinational circuits including adders, subtractors, multiplexers, demultiplexers, encoders, decoders, comparators, and arithmetic logic units (ALUs). These reversible implementations preserve information and theoretically dissipate very little energy, making them suitable for future low-power computing systems.

The main reasons for using reversible gates in combinational circuits are:

1. **Low Power Consumption:** Reversible circuits minimize energy loss caused by information destruction.
2. **Reduced Heat Generation:** Since information is preserved, less heat is produced during computation.
3. **Quantum Computing Compatibility:** Reversible logic forms the foundation of quantum computing architectures.
4. **Improved Energy Efficiency:** Reversible circuits are suitable for battery-powered and high-performance systems.
5. **Nanotechnology Applications:** Reversible logic is widely used in nanoscale and molecular computing devices.
6. **Optical Computing Support:** Many optical computing systems require reversible operations for efficient processing.
7. **Future VLSI Systems:** Reversible circuits help overcome power and thermal limitations in advanced VLSI technologies.

For example, a conventional full adder loses information during operation, whereas a reversible full adder designed using Peres or Toffoli gates preserves input information while producing the required outputs. As a result, reversible combinational circuits are considered essential building blocks for next-generation low-power, quantum, and nanotechnology-based computing systems.

5. SIMULATION TOOL

Environment setup is the work environment or tools on which result analysis has been done for Xilinx 6.2i. Xilinx is the very strong software tool to analysis and simulate the complex circuits. There are so many versions for Xilinx software such as 6.1i, 9.1i, 10.2i, 13.1i and 14.2i. Generally two programming language are using VHDL and Verilog.

VHDL is an acronym for VHSIC hardware description language (VHSIC is an acronym for very high speed integrated circuits). It is a hardware description language that can be used to model a digital system at many levels of absorption ranging from the algorithm level to the gate level [14]. VHDL allows users or programmers to use certain blocks which comprise of certain set of sequential statements. One such block is called a process. The (<=) operator, it is called the assignment operator and is used only for assigning values to signals. For variables the operator used is (:=).

Some chief terms that are used at the basic level are: - Libraries, Data types, Signals, Variables, Entity, and Architecture. Other important terms for the VHDL program such as process, component, function, procedures and state diagrams are used in programming.

Reversible Gate Parameter:-

Gate Count (GC): The number of gates used to realize reversible circuit

Garbage Outputs (GO): The number of unused outputs in a reversible logic. The inputs regenerated at the outputs are not garbage outputs.

Ancilla Inputs (AI): The number of input kept constant at either 0 or 1.

Delay : It corresponds to number of primitive quantum gates in the critical path of the circuit.

Quantum Cost:- Quantum cost is defined, as the number of basic quantum gates like controlled-NOT, Controlled V+, Controlled V and NOT gate.

6. CONCLUSION

Reversible logic has emerged as a key technology for the development of low-power and energy-efficient digital systems. The ability of reversible circuits to perform computations without information loss makes them highly suitable for applications in quantum computing, nanotechnology, optical computing, and advanced VLSI systems. In recent years, significant research efforts have been directed toward the design and optimization of combinational circuits using reversible gates to address the limitations of conventional irreversible logic.

This systematic review examined various types of reversible gate-based combinational circuits, including adders, subtractors, multiplexers, demultiplexers, encoders, decoders, comparators, and arithmetic logic units. The review highlighted the role of widely used reversible gates such as Feynman, Toffoli, Fredkin, Peres, Double Feynman, and HNG gates in achieving efficient circuit implementations. Various design methodologies and optimization approaches reported in the literature were analyzed and compared based on

important performance parameters, including quantum cost, gate count, garbage outputs, constant inputs, propagation delay, and hardware complexity.

The findings indicate that reversible logic circuits offer significant advantages in reducing power dissipation and improving computational efficiency. However, challenges such as minimizing garbage outputs, reducing quantum cost, and optimizing circuit complexity remain active areas of research. Continued advancements in reversible gate design and optimization techniques are expected to enhance the practicality of reversible computing systems and support the realization of future quantum and ultra-low-power digital technologies.

Overall, reversible gate-based combinational circuits provide a strong foundation for next-generation computing architectures. Future research should focus on developing highly optimized reversible circuits, scalable design methodologies, and efficient hardware implementations that can meet the growing demands of modern computing applications.

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