DESIGN AND ANALYSIS OF 1-BIT TRANSMISSION GATE ADDERS

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ABSTRACT: Addition is probably the most commonly used arithmetic operation. It also forms the basic for many processing operations from counting to multiplication to filtering. Even for performed to increment the program counter and to calculate addresses. Often it is also the speed limiting element. Therefore careful optimization is of almost importance.

In this paper we have briefly discussed the design of Transmission gate based Adder. We have analyzed its performance based on speed, power and Power Delay Product and having its comparative chart. Transmission gate based Adder consumes approximately 54.7%-66% less power as compare to Conventional Adder

I. INTRODUCTION

Adders have always been by far the most important and very frequently used operation, whether it is application specific for a processor or it is general purpose system. Lot of research and funding has been dedicated to improve the design of one adder over another to make the delay shorter and power consumption lesser.

II. ADDERS TOPOLOGIES

Following types of adders have been implemented to consider for the power, delay, area issue. It is very important to discuss the working of each adders and their comparative performance.

2.1. *Type*

Types of Single bit adder
1) Conventional adder
2) Mirror adder
3) Transmission gate based adder
4) Manchester adder

2.2. *Single Bit Full adder Design*

2.2.1 Conventional CMOS full adder:

A full adder performs the addition of two bits A and B with the Carry (C_{in}) bit generated in the previous stage. Full Adder using CMOS Logic and will be called as "Conventional CMOS design". The block diagram of conventional CMOS Full Adder is shown below

The above Boolean expressions may be rearranged as:

$$sum = c\,(a + b + c) + a \cdot b \cdot c \qquad (5)$$

$$carry = a \cdot b + c \cdot (a + b) \qquad (6)$$

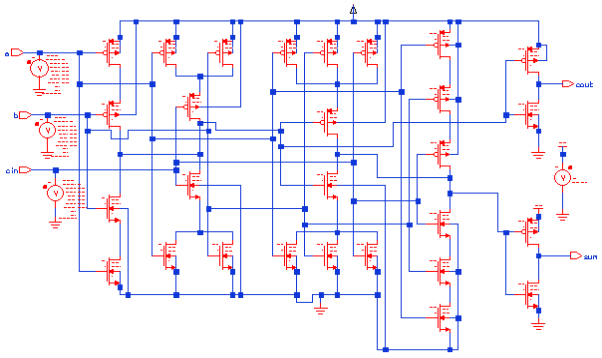

Fig 1. 2-1 Conventional Adder

2.2.2 Transmission gate full adder

The TG full adder, shown in Fig. 2 , is based on transmission gates and introduced for its low power dissipation [14]. As in the case of the LP circuit, cascading full adders leads to an overall propagation delay roughly proportional to n^2, which becomes excessive for long chains of full adders. This drawback is solved in the TG drivcap. Output buffers which interrupt the transmission gate chain when cascading full adders are added.

$$\overline{P} = A \oplus B \qquad (2.3)$$
$$\overline{D} = \overline{A} \,.\, B \qquad (2.4)$$
$$G = A \,.\, B \qquad (2.5)$$

We can write S & C_o as function of P & G,

$$C_o\,(G, P) = G + P \,.\, C_i \qquad (2.6)$$

$$S\,(G, P) = P \oplus C_i \qquad (2.7)$$

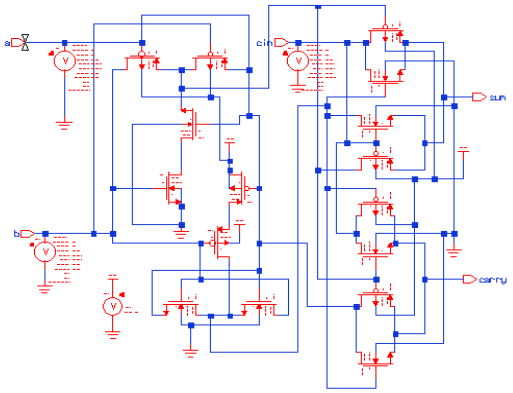

Fig 2. 2-2 Transmission gate based Adder

The carry generation circuitry is worth analyzing. First, the carry-inverting gate is eliminated. Second, the Pull-Up Network and Pull-Down Network of the gate are not dual.

Instead, they form a clever implementation of the Propagate/ Generate/ Delete function – when either D or G is high, Co_Bar is set to V_{dd} or GND respectively. When the condition for propagate is valid (or P is 1), the incoming carry is propagate to Co_Bar (in inverted format). This results in a considerable reduction in both area and delay.

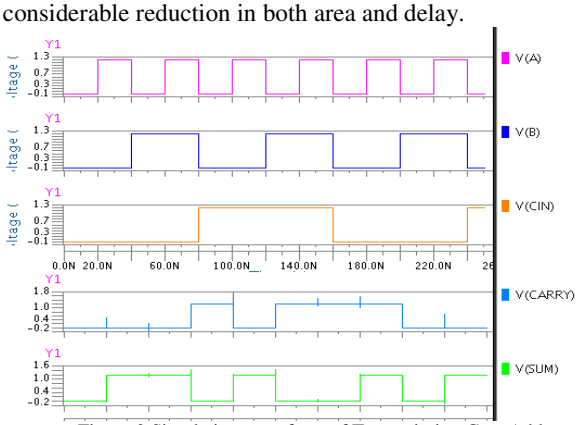

Figure 3 Simulation waveform of Transmission Gate Adder

III OBSERVATIONS

1. This full adder requires only 16 transistors.
2. Transmission gates [7, 8] consists of a PMOS transistor and an NMOS transistor that are connected in parallel.
3. Another Transmission Gate Full-Adder (TGA) presented in [8] contains 20 transistors.
4. TFA and TGA are inherently low- power consuming and they are good for designing XOR or XNOR gates.
5. When laying out the cell, the most critical issue is the minimization of the capacitance at node Co_Bar.

The output of carry stage derives two internal gate capacitance in the connecting adder cell. A clever solution to keep the transistor sizes the same in each stage is to increase the size of the carry stage to about three to four times the size of the sum stage. This maintains the optimal fanout of 2. Where a PMOS/NMOS ratio of 2 is assumed[8].

IV TESTING AND SIMULATION RESULTS

3.1. Testing.

Power Consumption of each cell is obtained from Mentors EDA simulation tool. Here the power consumption is the average power consumption per million transitions at the output. To find out average power consumption of the cell all the possible input transitions are applied at the input and the average is computed. Here input pattern is applied in such a manner that all possible input transitions are covered.

Note down the Average Power Consumed (P_{avg}) from the SPICE output file.

3.2. Simulation Results.

After putting the Schematic design the next step would be performance evaluation. The performance for a particular circuit could be based on the area of the design speed ,power and power delay product. All these three parameters are carefully evaluated for each of these adders and are given in Table 3.2.1 .

Table 3.2.1. Single-bit Adders.

Type of adders	Supply Voltage	Delay	Power Dissipation	Power delay Product
Conventional Adder	1.0v	39.9145ns	136.464 nwatt	5446.89
	1.2v	39.9145 ns	145.524 nwatt	5808.51
	1.5v	39.9145ns	344.714 nwatt	13759.08
Transmission gate based Adder	1.0v	33.2673ns	37.671 nWatt	1253.21
	1.2v	33.2673ns	45.205 nWatt	1503.84
	1.5v	33.2673ns	56.506 nWatt	1879.80

3.1.1. Graphical representation

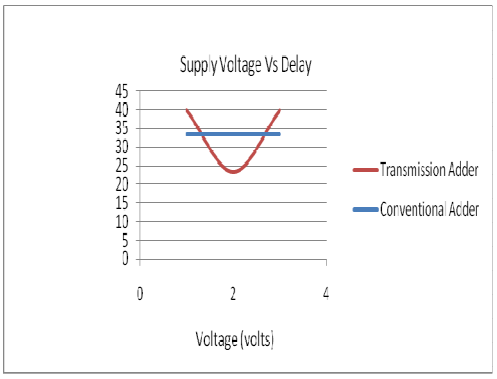

Fig. 3-1 Supply Voltage vs Delay

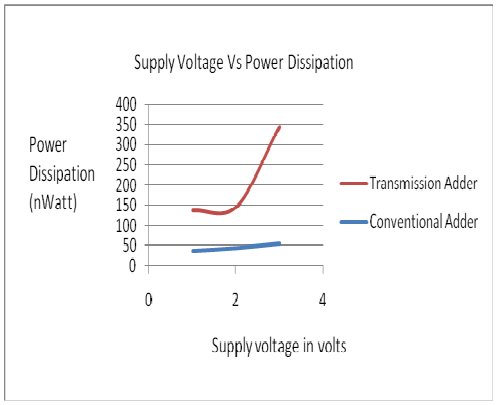

Fig. 3-2 Supply Voltage vs Power Dissipation

The graph shows comparative study for Conventional and Transmission Gate Adders. The comparisons are done on the basis of applied voltage and propagation delay, and supply voltage Vs power dissipation of adders.

As seen from the Fig. 3-1, when the supply voltage varies between 1.0V to 1.5V, the best results are obtained as on 1.2V for delay. If the supply voltage is increased or decreases above 1.2V, the Conventional adder Delay time should be increased and thus speed decreases.

Fig. 3-2 shows the comparison is done on the basis of power dissipation with respect to supply voltage. As shown in the graph, power dissipation should increases with increase in supply voltage and the Transmission adder has the least power dissipation at lowest voltage i.e at 1.0V.

So, from these graphs it can be seen that, if speed factor is considered, then power dissipation factor has to be sacrificed and vice-versa.

V CONCLUSION

In this paper basic Transmission Gate adder-cell characteristics have been compared. The adders were design using 0.18µm technology on Mentor Graphics.

The advantage of Transmission gate based adder is it have less power dissipation comparably to other basic 1 bit adder and Transmission gate based Adder consumes smaller area than other adders while it have a disadvantage that it has problem of full voltage swing. Transmission gate based Adder power dissipation is reduced in an abrupt amount if we go towards less power supply voltage.

REFERENCES

[1] Mary Jane Irwin and Robert Michael Owens. "*A Comparison of two Digit Serial VLSI Adders*". IEEE Transactions on Computers: 277-229, October 1998.

[2] Belle W. Y. Wei, member, IEEE, and Clark D. Thompson, "*Area-Time Optimal Adder Design*", IEEE Transactions on Computers, Vol. 39, No. 5, May 1990.

[3] Chien-In Henry Chen and Anup Kumar, "*Area-Time Optimal Adder Design*", IEEE Transactions on Computers, Vol. 43, No. 4, April 1994.

[4] R. P. Brent, and H. T. Kung, "*A regular layout for parallel adders*", IEEE Transactions on Computers, C–31(1982), 260–264.

[5] Taewhan Kim, William Jao, and Steve Tjiang, "*Circuit Optimization Using Carry–Save–Adder Cells*", IEEE Transactions on Computers – Aided design of integrated circuits and systems, Vol. 17, No. 10, October 1998.

[6] H. Ling, "*High speed binary parallel adder*", IEEE Transactions on Computers, EC-15(5):799-802, October 1966.

[7] A.Shams, T.Darwish, M.Bayoumi, Performance an alysis of low power1-bit CMOS full-adder cells, IEEE Transactions on Very Large Scale Integration (VLSI)Systems10(1)(2002February)20–29.

[8]Keivan Navi Mohammad Reza Saatchi and Omid desai A High-Speed Hybrid Full. European Journal of Scientific Research ISSN 1450-216X Vol.26 No.1 (2009), pp.29-33

[9]E. Boyce, "*CMOS Circuit Design, Layout and Simulation*", IEEE Press, PHI.

[10]Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, "*Digital Integrated Circuits – A Design Perspective*", Second edition, Pearson Education (Singapore) Pte. Ltd., Prentice Hall Electronics and VLSI Series.