IMPLIMENATION OF FM0/MANCHESTER ENCODING USING SOLS TECHNIQUES-A Review

ROHINI

Department of ECE, Bhabha University ,Bhopal, M.P, India
Email id: rohinidps@gmail.com

Abstract--**Intelligent transportation system is the next generation of transportation that ensures a greener, safer, and a much more convenient method of transportation across all modes of transport. The dedicated short-range communication (DSRC) is a transpiring technology which can be utilised to implement the intelligent transportation system into our everyday life. The DSRC protocols generally adopt FM0 and; Manchester; codes to enhance the signal reliability and achieve dc-balance.**

The disadvantages of using the conventional FM0 and Manchester techniques individually is that area utilization is less. Another disadvantage that we face with FM0 and Manchester is that the output that we get is an unbalanced dc logic. Different families have their specifications that lead us to find out the most suitable implementation out of all in varied circumstances.

Keywords—**Standard,Wireless communication,V2V communication**

I. INTRODUCTION

Intelligent transportation system ensures a greener, safer, and a much more convenient method of transportation across all modes of transport.

For instance, a car becomes another extension of our digital life such as when battery of the car becomes lower, it automatically searches for gas stations around.It aims at connected intelligence among vehicles and also will extend beyond vehicles. This includes communication between traffic lights & surveillance cameras to maintain real time automated systems of transportation. For instance, strategically positioned safety cameras will identify congestion or accidents automatically alerting safety personnel & rerouting traffic by notifying ongoing vehicles and frequently updating nearby roadside signs.

Intelligent traffic lights will become smarter than today detecting real time traffic flow from each direction & automatically updating; signals to improve traffic level.This system is implemented by DSRC.

DSRC is a standard used for; communication for a short limit range of distance, for instance hundred meters through the provided channel. Intelligent transportation system is introduced into our everyday life using this technology. The DSRC helps in vehicle to vehicle communication and vehicle to infrastructure communication. The vehicle to vehicle communication generally handles hard break warnings, collision alarms etc. Similarly, the vehicle to infrastructure communication comprises of the in vehicle signing, ETC, highway-rail intersection warning etc. Although the primary inspiration of the DSRC channel is vehicular safety and collision detection. Additionally, smooth traffic control is possible because of this communication. The DSRC equipment generally comprises of three modules: RF front end, base band processors and the microprocessors. The microprocessors are; accountable for the arrangement of the tasks; of base band processing and RF; front end and intercept- the instructions. The RF front end takes care- of the transmission and reception- of data. Finally main function of the base band processing- includes error correction, modulation, clock synchronization, and encoding. In order to encode data, generally an FM0 or Manchester encoding are used in order to reduce the likelihood of occurrence of noise in the channel whenever it is left solitary. When a system; that can be-reused between both the-FM0 and the Manchester encoding is observed, the hardware utilization rate is reasonably reduced thus, dropping the effectiveness. This ultimately affects the output results of the system. Thus a new technique of scheming a reusable VLSI architecture is brought to notice. This new design technique is called SOLS which helps in improving the hardware usage pace of the reusable design which ultimately enhances the area footage and performance.

II. BACKGROUND

A. FM0/Manchester Encoding Based on SOLS

DSRC (Dedicated-Short-Range-communication) is a one way or two-way communication standard that allows for very high rate of data transmissions. It is crucial in safety applications that rely on communications. DSRC standards employ either Manchester or FM0 code as an encoding technique to amplify signal reliability, to maintain DC balance. The primary limitation with the existing systems is,

the code word organisation of FM0 and Manchester are different, thus vastly impacting the DSRC hardware potential.

SOLS techniques merge hardware architectures of both FM0 and Manchester, and an integrated architecture accounts for a better hardware utilization rate (HUR). The SOLS techniques allowed for the circuits to be simplified such that hardware utilization rate (HUR) reached nearly 100%.

The Manchester encoding is vastly adopted as it is self-clocking, level sensitive and widely used to encode data and clock of a synchronous bit stream. Manchester encoding is a basic XOR operation between CLK and input data X.

$$Manchester\ Encoding = X \oplus CLK$$

Thus its hardware architecture can be designed with the use of an XOR gate.

The hardware design of FM0 encoder is drawn from the FSM of FM0 encoding. Without SOLS technique HUR is 57.14%, and almost half of the components get wasted. This drop in HUR drastically affects the effectiveness of the design.

SOLS technique uses two core methods to plan a fully reused VLSI architecture of FM0 and Manchester encoding:

Area compact retiming technique repositions the hardware resources to reduce transistor count. Area compact retiming technique minimizes the use of transistors by eliminating the use of a DFF in the primary circuit of the FM0 code. One amongst the two DFFs is removed from the circuit, and the other is relocated after the MUX to avoid and logic faults. Area compact timing technique lessens transistor count by 22 transistors.Balance Logic Operation Sharing combines FM0 code logic design and Manchester codelogic design to design a fully reused VLSI architecture. By comparing the equations of both the circuits, the primary stages are merged into a single MUX run by a single CLK signal, and this eliminates one additional MUX from the circuit. Similar concepts are applied to integrate additional signals. Also, the multiplexer is functionally integrated into relocated DFF from area compact retiming technique.

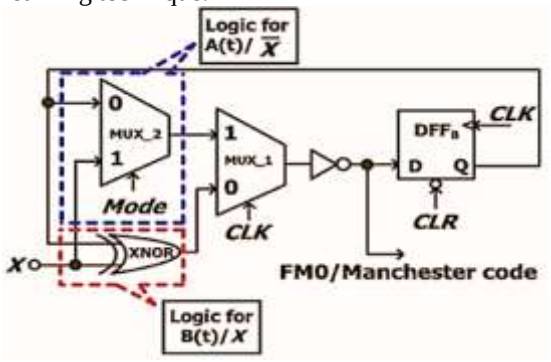


Fig.1 VLSI architecture of FM0 and Manchester encodings using SOLS technique

Combining the hardware architectures of both area compact retiming and balance logic operation sharing, the VLSI architecture of FM0/Manchester encoding is shown that achieves full reusability.

HUR with SOLS design: for VLSI architecture of FM0/Manchester encoding using SOLS technique, the number of components is reduced from 7 to 5 by using area compact retiming and balance logic operation sharing techniques of SOLS. Further, there is independence achieved in the application of any encoding technique due to all the components being fully reused.HUR is improved from 57.14% to 100% with all the hardware components fully reused with each other for both FM0 and Manchester encoding.

B. Manchester Code Generator (90nm)

Aim: A Manchester code generator is presented which is designed at a transistor level by adopting nMOS switches. The generator is constructed using 26 transistors while preserving the complexity as that of a standard D flip-flop. Manchester Code generators are designed for DRSC systems, which require high-speed communication. The primary benefit of this design is the usage of a clock signal running at an equal frequency as that of the data. The rising and falling edge of the clock are when the output of the generator changes. The circuit was designed in a UMC CMOS technology(90nm) to evaluate the effectiveness of the proposed approach. Experimental results demonstrate the correct behaviour up to 5 Gbit/s data rate.

Manchester code is an extremely prevalent code as it is self-clocking, level insensitive and can also detect the absence of signal as the coded signal always undergoes at least one transition per bit.

CMOS wideband switches are primarily designed to suit the necessities of devices communicating at ISM (industrial, scientific, and medical) band frequencies. Many high frequency applications that work on low power and has the ability to handle the transmitted power can use these devices, this is primarily due to a very small amount of insertion loss between the ports, low distortion, high isolation between the ports and their low current consumption.

Wideband switches use simply NMOSs in the signal path to increase their bandwidth. A switch with only NMOS, has practically twofold the bandwidth performance of a standard switch, one with NMOS and PMOS transistors in parallel. This is a consequence of the greatly diminished parasitic capacitance owing to the elimination of the PMOS and the reduced switch size. N-channel MOSFETs behave fundamentally as voltage controlled resistors.

The use of Manchester codes can aid the structure of photo receiver amplifiers in the context of optical interconnections. The novelty in this implementation is the use of RF switches. Classical CMOS inverter is used as a basis for the design. The transistor size of each inverter has to be optimized to ensure correct behaviour. Decreasing the size of the transistor would lead to an increase in the propagation time of the inverters whereas an increase in their size would increase the capacitance of preceding ones and thus their propagation delay would increase.
A Manchester code generator was designed with only 26 transistors and 6 NMOS switches running at 2.4 GHz and 5 GHz without changing the size of transistors.

C. Manchester Encoder for UHF RFID Tag Emulator

Aim: Radio Frequency Identification (RFID) is the most widespread wireless identification technology. The UHF RFID tag is designed for testing the RFID systems it operates at 860 MHz to 960 MHz, further it acts as a general purpose data transport device for other RFID systems. This paper discusses the Finite State Machine and RTL executions of a Manchester Encoder with particular focus on RFID emulator as a data transport device. In this paper the presented Manchester Encoder is implemented using Finite state machine (FSM) and Register Transistor Logic (RTL).

RFID are contactless data capture systems. The power necessary to run these devices is supplied by the reader by induction coupling. Thus, RFID is a system in which the information is carried by the Radio Waves. The components that are essential for implementing any RFID system are RFID Tag, RFID reader, RFID antenna, Controller, Sensor and the software system holding everything all together. Tag emulator is used to generate tag data in EPC format, it is also a part of the testing and debugging tools. A Tag emulator is used for mimicking the RFID Tag. A Tag emulator captures multiple tags and permits their access only to the authorized reader. Manchester Encoding is a digital phase modulation encoding method. It is special as a separate clock is not required at receiver, there are no DC components either. Manchester Codes also eliminate long strings of logic 1 or logic 0. However, the decoding technique is rather complex and the modulation bandwidth needed is double that of NRZ. It is a technique of merging a serial data stream with a synchronized clock signal to create Manchester encoded signal. In this technique a transition in the output data state at the middle of the data bit is observed. Manchester encoding is also called as Bi-Phase code, due to the fact that each bit is encoded by a positive 90 degree phase transition or a negative 90 degree phase transition. The instantaneous transition between logic 1 and logic 0 is the reason behind the zero DC power of the Manchester encoded data.
Thus the FSM of the Manchester encoder was designed and thus used to realize the design using Verilog HDL.

The obtained schematic demonstrates the efficient use of hardware, minimizing the number of components used, thus minimizing the area used on a FPGA.

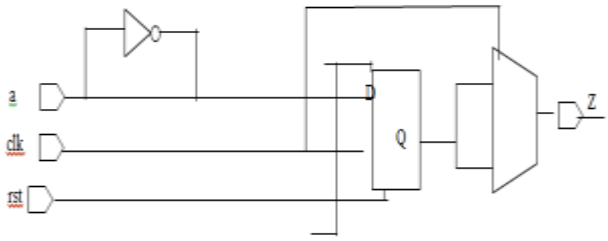


Fig.2 Schematic of FSM based Manchester Encoder

The maximum frequency of operation achieved in the FSM based design is 256.54 MHz whereas that of RTL based implementation achieves 247.64 MHz. The maximum path delay for the FSM based design is also lesser at 9.622ns while for the RTL design is 9.764ns. Further analysis also shows that the FSM approach is the more efficient approach. However, extracting the clock from the encoded data is a difficult task, since Manchester decoder doesn't need a clock at the receiver end since the data is self-clocking. The two approaches for implanting a Manchester decoder are with the use of a phase-locked loop (PLL) or by the use of the over-sampling technique.

Thus the presented work in this paper exploits the Manchester encoder's design strategies, this is done as a plan for eventual integration in the UHF RFID tag emulator. The Finite State Machine based Manchester encoder displays higher efficiency amongst the two approaches.

D. CMOS Chip Design for Manchester and Miller Encoder

A modified Manchester and Miller encoder is proposed in this paper that operates at high frequencies without complex circuit structure. Also, the model of parallel operation is applied enhance throughput and the technique of hardware sharing is implemented to reduce transistor count. The circuit is also integrated into Radio Frequency Identification (RFID) tag emulators.
In RFID systems, in order to improve efficiency and reduce error rate, the data is encoded before

modulation. This data, through modulation is transmitted between the tag and the reader. Manchester and Miller codes are the most prevalent techniques used for RFID systems. The Miller code has been studied for efficient circuit realization, since it has better performance against noise interference and delay errors.

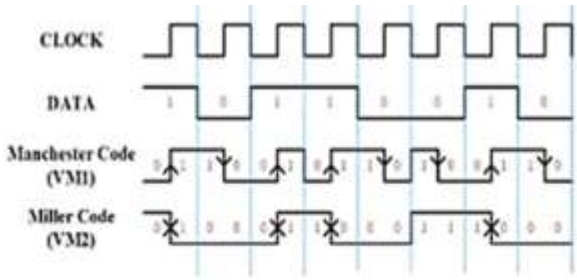


Figure 3: Waveform samples for various coding

RFID systems uses one of the three most popular encoding methods: Non Return to Zero code (NRZ), Manchester code and Miller Code. NRZ code being the simplest amongst the lot. Since NRZ has no timing information, i.e. when a series of '1' bits or '0' bits are transmitted from receiver to sender, the synchronous information for high speed transmissions are lost. Thus the error rate for NRZ is increased for high speed operations. Manchester code is called split-phase coding or dual phase coding. This is due to the fact that it uses the transition from a high-to-low level transition to represent a logic 0 and the positive rising edge of a low-to-high level transition to represent a logic 1. Manchester code is a self-clocking code.

Miller code represents a logic '1' by either the positive or negative edge of the half cycle. Logic '1' in Miller code is either represented as '01' or '10', depending on the preceding bit status.

In order to generate Miller code, the output from a Manchester encoder is fed into a T- Flip Flop (TFF). To improve the speed of the encoder, two identical encoders operate in interlaced fashion this improves the overall speed. We also have the benefit of double speed enhancement, however at the cost of increased hardware. To optimize the hardware cost and power consumption, some circuit blocks are further simplified.

The action of the modified Manchester and Miller encoder is described as, the data is first switched rapidly in turn into 2 individual DFFs by the de-multiplier stage. The data is sequentially processed by top and bottom data path. After DFF, the processed data is combined as Manchester code, this data is then passed through a single TFF and finally Miller codes are obtained after recombination from top and bottom data path.

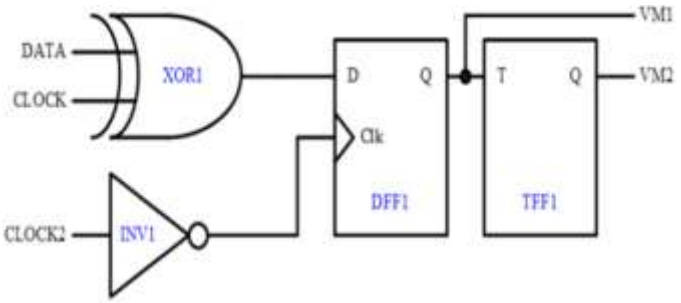


Fig.4: High-speed Manchester and Miller encoder circuit structure

HSPICE simulation results shows that the operation frequency of the proposed circuit stretches to 200 MHz while under the operational voltage of 3.3 V. This paper successfully designed a modified Miller and Manchester CMOS encoder by using hardware sharing and parallel operation techniques. Under room temperature, the average power consumption of the circuit is 549 μW. It employs 94 transistors and the total layout area of the circuit is 70.7 μm × 72.2 μm. The authors expect the proposed design to be integrated into the RFID design with ease. Further, the circuit speed may be improved by using Dynamic Logic.

E. DSRC Applications in Intelligent Transportation System using SOLS Technique for fully reused VLSI Architecture

Aim: Dedicated Short Range Communication (DSRC) is a technique that employs high speed short distance communication. The most pressing issue with the implementation of DSRC is the inability to implement both Manchester and FM0 codes. To tackle this SOLS technique is used,it helps achieve 100% HUR and reduces system area covered.

Manchester encoding is realized using an XOR gate, the encoded signal is the XOR function
implemented on the clock signal and the data signal.

FM0 Is implemented using two flip flops and multiplexers. The FM0 encoding is implemented as shown. A(t) and B(t) indicates the two states.

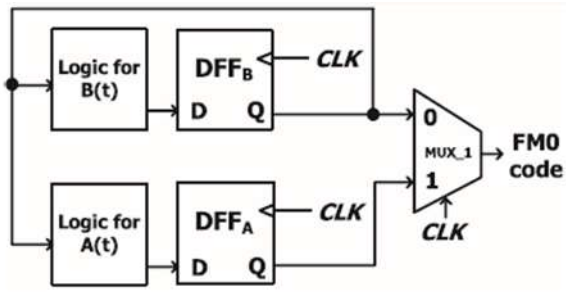


Fig.5 FM0 encoder

The SOLS technique is primarily implemented by two methods, area compact retiming and the logic simplification.

Area compact retiming technique minimizes the use of transistors by eliminating the use of a DFF in the primary circuit of the FM0 code. One amongst the two DFFs is removed from the circuit, and the other is relocated after the MUX to avoid and logic faults. Area compact timing technique reduces transistor count by 22 transistors. Balance Logic Operation Sharing combines the logic of both FM0 and Manchester codes to design a fully reused VLSI architecture. By comparing the equations of the 2 circuits, the primary stages are amalgamated into a sole MUX run by a single CLK signal, and this eliminates one additional MUX from the circuit.

However, although the SOLS technique enables the VLSI architecture to be fully shared for FM0 and Manchester encoders, their critical paths are not identical. For Manchester encoding, the delay time is represented by $TMan$ and given as

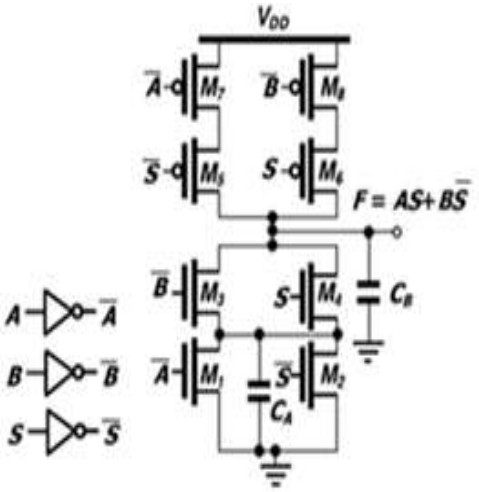
$$TMan = \{TMUX, TXNOR\} + TMUX + TINV$$

For Manchester encoding, the DFFB is always kept at a logic-0, however in FM0 encoding, DFFB stores the state code and thereby the delay time becomes

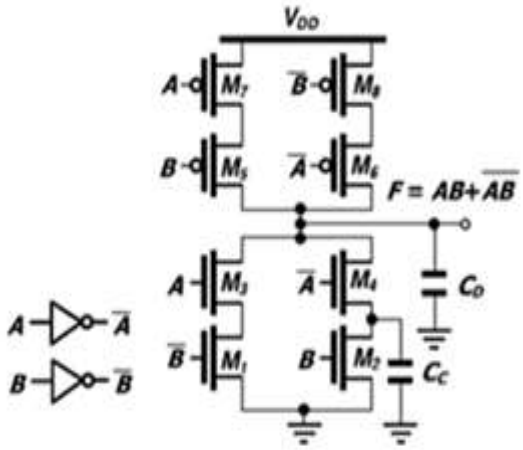
$$TFM0 = TMan + TDFF$$

For the static CMOS, the series of the two multiplexers used dominate the Manchester encoding path and lead to a total propagation delay as

$$2T_{MUX\text{-}SC} = 2(T_{INV} + C_A R + C_B 2R)$$



(a)



(b)

Figure 6.: Static CMOS topologies of:
(a) Two-input multiplexer
(b) Two-input XNOR

III. CONCLUSION

The vast differences between FM0 and Manchester encodings result in various limitations on HUR of the VLSI architecture. This paper proposes the SOLS technique to tackle this issue. The SOLS technique achieves an HUR of 100% from 57.14% which is a significant jump.

The vehicle to vehicle communication which is known to help road safety includes 2 types of protocols for its implementation.

1. Dedicated short range communication (currently in use)
2. Cellular V2X (recent development in the field):

The wireless communication technology keeps on improving with time and the advancement which have come in the cellular communication (4G LTE and 5G) can be used for the vehicle to vehicle communication also.

The major challenges which are faced by vehicular communication includes:

1. Assisting high speed because due to the very high speed of the cars as much as 250kmph, the Doppler spread is around 2700 Hz which makes the estimation of the channel bandwidth even more challenging. (for DSRC to overcome this problem ,advanced algorithms have to be used which are practically not possible to implement because of their high implementation complexity, whereas in the case of V2X ,high speeds cab be supported by adding a reference symbol per 2 OFDM channels)
2. Supporting long range communication another problem is the range of the vehicular communication. This is very important to understand about the blind spots kind of applications. In the case of DSRC, no optimization has been done to improve the range,

whereas long communication range is a known prime advantage of the cellular communication.

IV. ACKNOWLEDGMENT

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V. REFERENCES

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