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Review Paper on VLSI Architecture for 2-D Discrete Wavelet Transform using Multiplier-less Technique

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Abstract: This review paper presents a comprehensive analysis of VLSI architectures for implementing the 2-D Discrete Wavelet Transform (DWT) using multiplier-less techniques. The 2-D DWT is a fundamental tool in image processing applications such as compression, denoising, and feature extraction, especially in standards like JPEG2000. However, conventional hardware implementations rely heavily on multipliers, which increase design complexity, area, and power consumption. To overcome these limitations, recent research has focused on multiplier-less approaches that replace complex multipliers with efficient shift-and-add operations, distributed arithmetic, and coefficient approximation methods.

The paper critically examines various existing architectures, including lifting scheme-based designs, distributed arithmetic (DA)-based implementations, and pipeline and parallel processing techniques. These methods significantly reduce hardware utilization while maintaining computational accuracy. The use of efficient adders and memory-based computations further enhances performance by minimizing critical path delay and improving throughput. Additionally, the review highlights trade-offs between area, speed, and power consumption across different design approaches.

Overall, multiplier-less VLSI architectures demonstrate considerable potential for achieving high-speed and low-power 2-D DWT implementations. The study concludes that such techniques are highly suitable for real-time and resource-constrained applications, including embedded and portable image processing systems. Future research directions include the integration of advanced adder architectures and optimization techniques to further improve performance and scalability.

Keywords: 2-D Discrete Wavelet Transform (DWT), VLSI Architecture, Multiplier-less Technique, Distributed Arithmetic (DA)

1. INTRODUCTION

The rapid advancement in digital signal and image processing has significantly increased the demand for efficient hardware implementations of complex mathematical transforms. Among these, the 2-D Discrete Wavelet Transform (DWT) has emerged as a powerful tool due to its excellent time-frequency localization properties and multi-resolution analysis capability. It is widely used in applications such as image compression, denoising, feature extraction, and video processing. In particular, standards like JPEG2000 rely heavily on 2-D DWT for achieving high compression efficiency while preserving image quality. However, implementing 2-D DWT in hardware, especially using conventional approaches, poses

several challenges in terms of computational complexity, hardware resource utilization, power consumption, and processing speed [1, 2].

Traditional VLSI architectures for 2-D DWT primarily depend on multipliers for performing convolution operations. Although multipliers provide accurate results, they are resource-intensive components that occupy a large silicon area and consume significant power. This makes them less suitable for real-time and portable applications where energy efficiency and compact design are critical requirements. As a result, there has been a growing interest in developing multiplier-less techniques that can reduce hardware complexity without compromising performance. These techniques typically replace multiplication operations with shift-and-add methods, coefficient approximations, or memory-based computations such as Distributed Arithmetic (DA) [3, 4].

The lifting scheme is another important approach widely adopted in modern DWT implementations. It decomposes the wavelet transform into a sequence of simpler filtering steps, enabling in-place computation and reducing memory requirements. When combined with multiplier-less techniques, the lifting scheme further enhances hardware efficiency by minimizing arithmetic operations. Additionally, advanced architectural strategies such as pipelining and parallel processing are employed to improve throughput and reduce critical path delay, thereby increasing the overall speed of the system [5].

In recent years, researchers have proposed various optimized VLSI architectures for 2-D DWT that focus on achieving a balance between area, speed, and power consumption. These designs often incorporate efficient adder structures, memory optimization techniques, and resource-sharing mechanisms to further enhance performance. The use of Field Programmable Gate Arrays (FPGAs) has also gained popularity due to their flexibility, reconfigurability, and suitability for rapid prototyping. FPGA-based implementations allow designers to evaluate different architectural choices and optimize designs for specific applications [6, 7].

This review paper aims to provide a detailed analysis of existing multiplier-less VLSI architectures for 2-D DWT. It highlights the key design methodologies, compares their performance metrics, and discusses the advantages and limitations of each approach. By examining recent developments in this field, the paper identifies emerging trends and potential research directions for further improvement. The study emphasizes the importance of designing efficient, high-speed, and low-power architectures to meet the growing demands of modern image processing systems, particularly in embedded and real-time applications [8].

2. LITERATURE REVIEW

Qitao Li et al. [1], a brand new QRS complex detection algorithm based on the DWT is presented in this paper on a very large-scale integration chip. The first step in many aspects of electrocardiogram (ECG) analysis is to detect the QRS complex. Since the RR interval is used to evaluate heart rate variability (HRV), for instance, an effective QRS detection algorithm would have a significant impact on the subsequent HRV analysis steps. On the other hand, this study proposes a simple, dependable, low-power, and cost effective QRS detection method and its VLSI implementation because wireless monitoring is still

prohibitively expensive and reducing its cost and power consumption requires reducing the complexity of the algorithm. The quadratic spline wavelet-transform-based wavelet packet decomposition is utilized-in-this instance to carry out the task of QRS complex detection. A novel noise level detection is carried out following a four-level DWT decomposition in order to improve the QRS complex. The proposed noise level detector would first-determine-the-product-of-two of the four wavelet coefficients. Consequently, the processing stage also includes the execution of decision rules, the adaptive thresholding scheme, and the-product-of-the two chosen wavelet coefficients. Manufactured on a 0.18-µm integral metal oxide semiconductor, the 1-KHz processor draws just 4.2 µW of force, and the chip region is just 0.83 mm^2. Additionally, 48 recordings from the MIT-BIH arrhythmia database are used to confirm the proposed method's detection accuracy (Se = 99.57%, +P=99.59%), indicating-that-the proposed QRS detector may-be-able to detect QRS complexes with high accuracy and low cost.

A. Cardozo et al. [2], for the one-dimensional (1-D) and two-dimensional (2-D) DWT, a comprehensive analysis of VLSI architectures is presented in this paper. Additionally, three related architectures are proposed. There are three types of 1-D DWT and inverse DWT (IDWT) architectures: B-spline, lifting, and convolutional models. They are talked about with regards to equipment intricacy, basic way, and registers. Concerning the 2-D DWT, the most pressing issues are the substantial amount of frame memory access and die area occupied by the embedded internal buffer. Different external memory scan techniques are used to classify and examine the two-dimensional DWT architectures. The internal buffer's implementation issues are also discussed, and some real-world experiments demonstrate that the internal buffer's area and power are highly correlated with memory technology and working frequency rather than just the required memory size. The overlapped stripe based scan method and the B-spline based IDWT architecture are also suggested in addition to the analysis. Last but not least, we suggest a one-level 2-D DWT architecture that takes full advantage of the analysis's many advantages and is both adaptable and effective.

Raja Arslan Naseera et al. [3], a more accurate and resource efficient "QRS" detector is what we propose in this paper. We used a pipeline-scheduled, reconfigurable time-sharing computation unit inspired by the folded architecture's approach. We developed the position calibration unit (PCU) on the basis of the data compression method in order to more precisely locate the position of the "R" peak and to reduce the need for additional hardware. Using the Verilog programming language, the proposed architecture was implemented on the Xilinx Zynq-7000. On the MIT-BIH database, the proposed architecture has the best performance when compared to current designs, with a sensitivity of 99.76 percent, a precision of 99.85 percent, and a detection error rate of 0.40 percent. Additionally, the proposed architecture reduces power consumption, storage memory, and computing resources by 13.35 percent, 1.28 percent, and 4.35 percent, respectivel

G. D. Mahesh et al. [4], a real-time QRS-detection algorithm and a dynamic tracking-based 12-bit successive approximation register (SAR) ADC are proposed. There are two tracking windows in the dynamic tracking algorithm that are right next to the prediction interval. The

prediction code is updated, and the subrange interval is automatically adjusted by this algorithm, which is able to locate the variation range of the input signal. Real-time QRS-detector and synchronous time sequential ADC are incorporated into the QRS-complex detection algorithm. The chip is made using a 0.6 V supply and the standard 0.13 m CMOS process. At 10k Hz sample rate and 41.5 Hz sinusoid input, measurements reveal that the proposed ADC has an effective number of bits (ENOB) of 10.72 and a spur-free dynamic range (SFDR) of 79.63 dB. The limits of the DNL and INL are -0.67/1.43 LSB and -0.62/0.62. In the ideal scenario, the ADC achieves a FoM of 48 fJ/conversion step. Additionally, the prototype successfully extracts the heartbeat signal when subjected to ECG signal input.

Yuan-Ho Chen et al. [5], this paper introduces power reduction strategies and considerations at the system level of design, where we have the greatest potential to influence power, with the goal of lowering the power consumption of wearable healthcare devices based on electrocardiography. It focuses on algorithm design and implementation, data acquisition, and transmission with limited resources. Based on metrics like sensitivity, positive predictivity, power consumption, parameter selection, and time delay, nine existing algorithms are thoroughly examined for their suitability for on-sensor QRS feature detection. A direct memory access (DMA) list approach and low-level register manipulations for task delegation are used to optimize data acquisition on CPU-based IoT systems and reduce current consumption by a factor of three. Additionally, the batch size, buffer size, sampling rate, and acquisition data rate are all optimized. The impact of on-sensor versus off-sensor processing is investigated in order to cut down on the amount of power required for data transmission. While the experiments in this work were carried out on a generic low-power wearable platform and focused on CPU-based systems, the design optimization and considerations suggested in this work could be extended to custom designs, which would make it possible to conduct additional research into optimizing the QRS detection algorithm for wearable devices.

Jhilam Jana et al. [6], the vital data contained in an electrocardiogram (ECG) signal can be used to identify a variety of arrhythmia conditions. In this work, we have fostered a calculation to identify the R pinnacles of the ECG signal in light of the Skillet Tompkins Calculation. The work has also been improved to a first-level approximation for the purpose of identifying various arrhythmia conditions. The Q and S points that are based on the R-peaks are also found in order to compute the QRS complex. The MIT/BIH arrhythmia database is used as a reference for R peak annotations and as a source for ECG signals in order to verify that the proposed algorithm works. The metric of False Detection Rate (FDR) of 1.289%, Sensitivity of 99.492%, and Positive Predictivity of 99.293% is provided by the algorithm. In order to extract the P and T waves from the signal, the entire QRS complex is reset to zero after it has been detected. As a result, this work offers a unique strategy for real-time P, Q, R, S, and T wave detection of an ECG signal. To demonstrate the approach's efficacy, the algorithm is further ported to a low-cost ECG monitoring patch.

W. Yan et al. [7], have wireless body sensor networks, compressive sensing (CS) has recently been used as a low-complexity compression framework for long-term electrocardiogram (ECG) signal monitoring. ECG signals can be recorded over a long period of time for diagnostic purposes and to track the progression of a number of common diseases. By calculating the distance between QRS complexes (R-peaks) in the ECG signal, beat-to-beat intervals, in particular, can be derived from the signal and provide important clinical information. For uncompressed ECG, a variety of R-peak detection techniques are available. However, with relatively complex optimization algorithms and possibly a significant amount of energy consumption, signal reconstruction can be carried out with compressed sensed data. Without reconstructing the entire signal, this paper addresses the issue of estimating heart rate from CS ECG recordings. Methods: We consider a framework in which CS linear measurements are used to represent the ECG signals. The correlation between the compressed ECG and a known QRS template is used to estimate the QRS locations in the compressed domain. The proposed method proves to be very convenient for low-power real-time applications because it does not require reconstruction.

Z. Zhang et al. [8], Internet of Things (IoT) medical wearable devices require an ultra-low power electrocardiogram (ECG) processing architecture that is accurate enough. An innovative real-time QRS detector and an ECG compression architecture for IoT healthcare devices are presented in this paper. An A-CLT, or absolute-value curve length transform, is proposed to effectively improve QRS complex detection while using as few hardware resources as possible. Only adders, shifters, and comparators are required in the proposed architecture, which eliminates multipliers altogether. QRS recognition was achieved by involving versatile limits in the A-CLT changed ECG signal and accomplished a responsiveness of 99.37% and the predictivity of 99.38% while approved utilizing Physionet ECG data set. The proposed architecture also includes a lossless compression method that makes use of entropy encoding and the ECG signal's first derivative. Utilizing the MIT-BIH database, the evaluation produced an average compression ratio of 2.05. With minimal hardware resources, the proposed QRS detection architecture addresses nearly all ECG signal artifacts, including baseline drift, low-frequency noise, and high-frequency interference.

3. METHODOLOGY

The proposed methodology for implementing a 2-D Discrete Wavelet Transform (DWT) using a multiplier-less technique focuses on reducing hardware complexity while improving speed and power efficiency. The design is mainly based on the lifting scheme and Distributed Arithmetic (DA), which eliminate the need for conventional multipliers.

Initially, the input image is fed into the system and processed row-wise followed by column-wise to achieve 2-D transformation. The first stage performs 1-D DWT on each row of the image. This is achieved using lifting steps, which consist of split, predict, and update operations. In the split stage, the input signal is divided into even and odd samples. The predict stage estimates the odd samples using even samples, while the update stage refines the even samples based on the predicted values.

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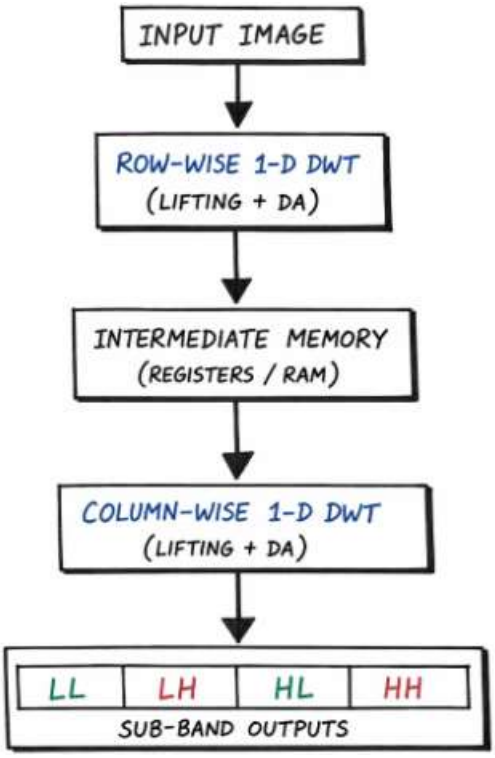

Figure 1: Methodology

To avoid multipliers, the design uses shift-and-add operations and precomputed coefficients stored in Look-Up Tables (LUTs). Distributed Arithmetic (DA) is applied to perform inner product computations efficiently using memory-based techniques. This significantly reduces hardware usage and improves speed.

After completing row-wise transformation, the intermediate output is stored in memory (usually RAM or registers). Then, column-wise 1-D DWT is applied to the stored data, producing four sub-bands: LL (approximation), LH (horizontal details), HL (vertical details), and HH (diagonal details). These sub-bands represent different frequency components of the image.

To further enhance performance, pipelining and parallel processing techniques are incorporated. Efficient adder structures such as Carry Select Adder or Kogge-Stone Adder (KSA) are used to reduce delay and improve throughput. The entire architecture is implemented on FPGA for validation and performance analysis.

Multiplier-less Technique

The multiplier-less technique is an efficient design approach used in VLSI architectures to eliminate the need for hardware multipliers, which are typically the most area- and power-consuming components in digital systems. In applications like the 2-D Discrete Wavelet Transform (DWT), frequent multiplication operations are required for filtering and convolution. Replacing these multipliers with simpler operations significantly improves hardware efficiency, making the system more suitable for real-time and low-power applications.

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In this technique, multiplication operations are replaced by shift-and-add operations, Distributed Arithmetic (DA), or coefficient approximation methods. Since shifting operations can be implemented using simple wiring and adders require less hardware compared to multipliers, the overall circuit complexity is greatly reduced. For example, multiplication by constants can be achieved using combinations of left shifts and additions, avoiding the need for full multipliers.

One of the most widely used multiplier-less approaches is Distributed Arithmetic (DA). In DA, precomputed values of coefficients are stored in Look-Up Tables (LUTs), and the multiplication results are obtained through memory access and accumulation. This method is highly efficient for fixed-coefficient systems like DWT filters, as it trades off memory usage for reduced computational complexity and faster execution.

Another important approach is the lifting scheme, which restructures the wavelet transform into a sequence of simple steps such as split, predict, and update. These steps involve fewer arithmetic operations and can be efficiently implemented using adders and shifters. When combined with multiplier-less techniques, the lifting scheme further reduces hardware requirements and improves performance.

4. CONCLUSION

In conclusion, this review paper highlights the significant advancements in VLSI architectures for 2-D Discrete Wavelet Transform (DWT) using multiplier-less techniques. The study demonstrates that replacing conventional multipliers with efficient approaches such as distributed arithmetic, shift-and-add operations, and lifting schemes leads to substantial reductions in hardware complexity, area, and power consumption. These optimizations make multiplier-less architectures highly suitable for modern applications that պահանջ high-speed processing and energy efficiency.

Furthermore, the analysis of various architectures reveals that the integration of pipelining, parallel processing, and optimized adder designs plays a crucial role in improving system performance by reducing critical path delay and increasing throughput. The use of FPGA platforms has also enabled flexible and cost-effective implementation, facilitating rapid prototyping and design validation.

Overall, multiplier-less VLSI architectures for 2-D DWT offer an effective balance between performance and resource utilization. They are particularly beneficial for real-time image processing, embedded systems, and portable devices. Future research can focus on further enhancing power efficiency, exploring advanced adder structures, and extending these techniques to more complex wavelet transforms to meet the growing demands of next-generation digital systems.

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